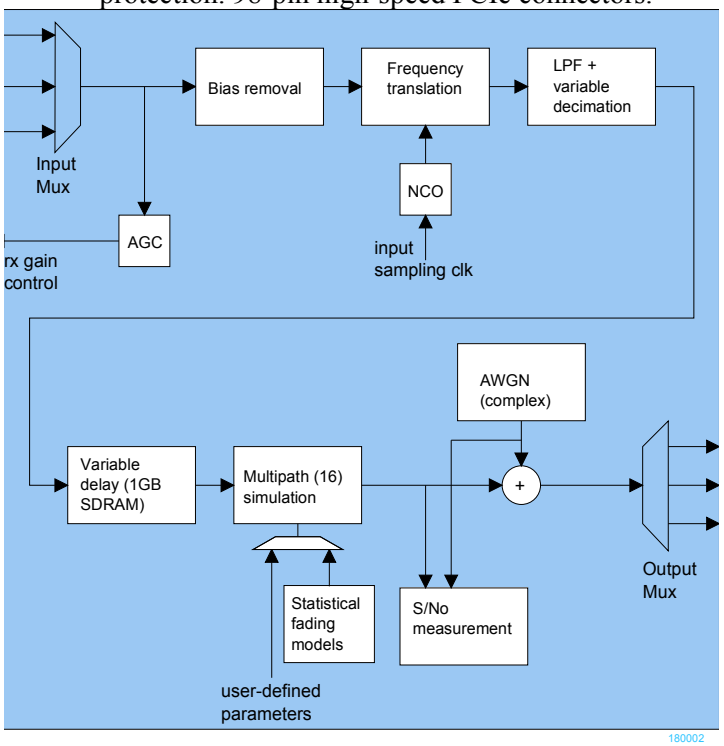
COM-1824 Channel Emulator

Key Features

- Real-time digital channel simulator, featuring multipath fading, white Gaussian noise, frequency translation and long propagation delay (satellite link).
- Multipath fading parameters are either user controlled (via USB or LAN/TCP) or adjusted dynamically by supplied statistical simulation models:
    - Rician (some line of sight)
    - Rayleigh (no line of sight)
    - Lognormal shadowing.
- Precise additive White Gaussian Noise (AWGN)
- Long programmable delay up to 256 Msamples (1GB) for satellite link simulation.
- Maximum input sampling rate: 120 Msamples/s, complex, 16-bit precision. Support for complex baseband inputs and IF undersampling.
- Multi-path:
    - 16 complex baseband paths (one direct, 15 scattered or reflected paths)
    - Each indirect path is modeled as
        - A delay (0 to 511 samples)
        - An initial phase offset
        - A Doppler frequency offset
        - An amplitude scaling coefficient
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.
- Connectorized 3”x 3” module. Single 5V supply with reverse voltage and overvoltage protection. 98-pin high-speed PCIe connectors.



COM-1824

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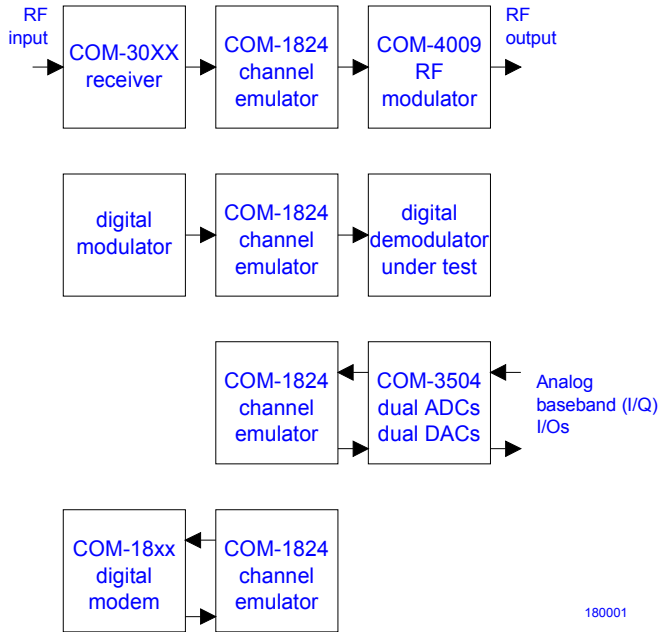
For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/com1824.html. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.html

Typical Configurations

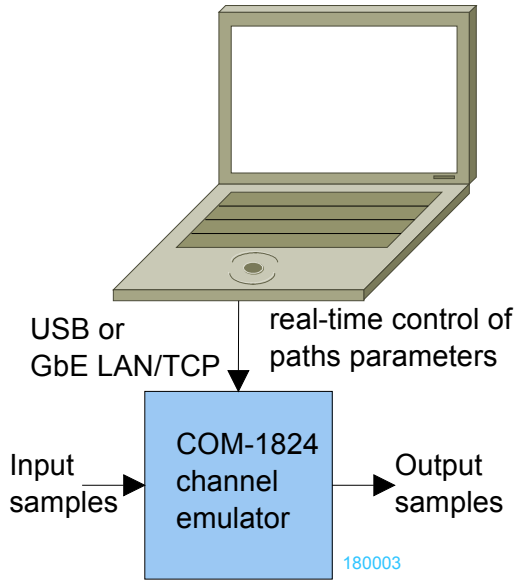


Multi-path simulator

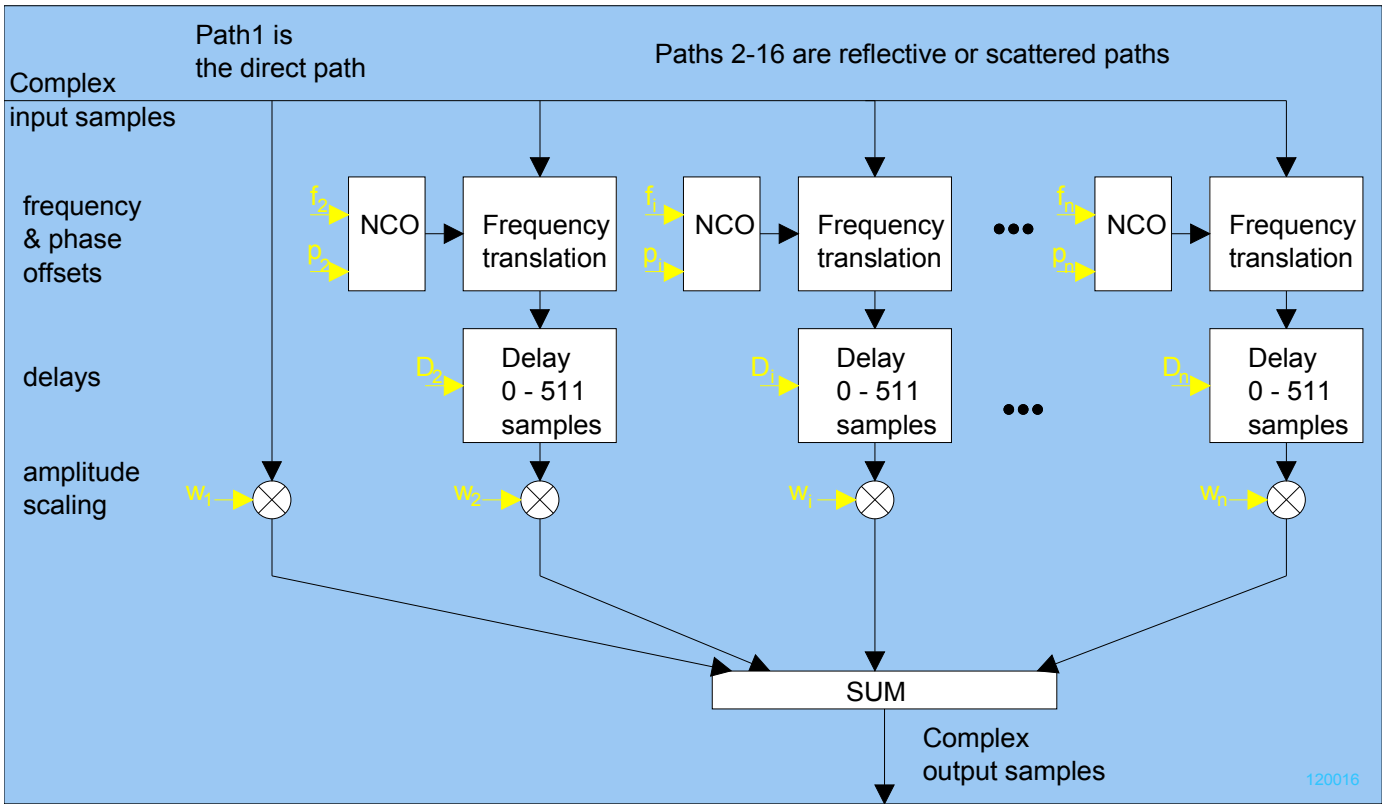
The multipath section of the simulator can be operated in either **auto** or **manual** mode.

In auto mode, the multi-path parameters are statistical variables generated automatically (as a one-time or periodic random draws) by the ComBlock Control Center. The random variables are drawn on the basis of user-supplied system-level parameters such as maximum Doppler, delay spread, indirect path mean amplitude, etc.

In manual mode, users can program each path parameter (delay, phase rotation, frequency offset, amplitude scaling coefficient) by running a custom program on the host computer and communicating in real-time over a USB or LAN/TCP connection. (see the code template in CD-ROM).



Multi-path simulator



Path 1 is the direct path, and as such represents the reference against which the other paths are described in terms of relative delay and relative frequency offset. The path 1 gain can be set to zero to simulate the absence of line of sight.

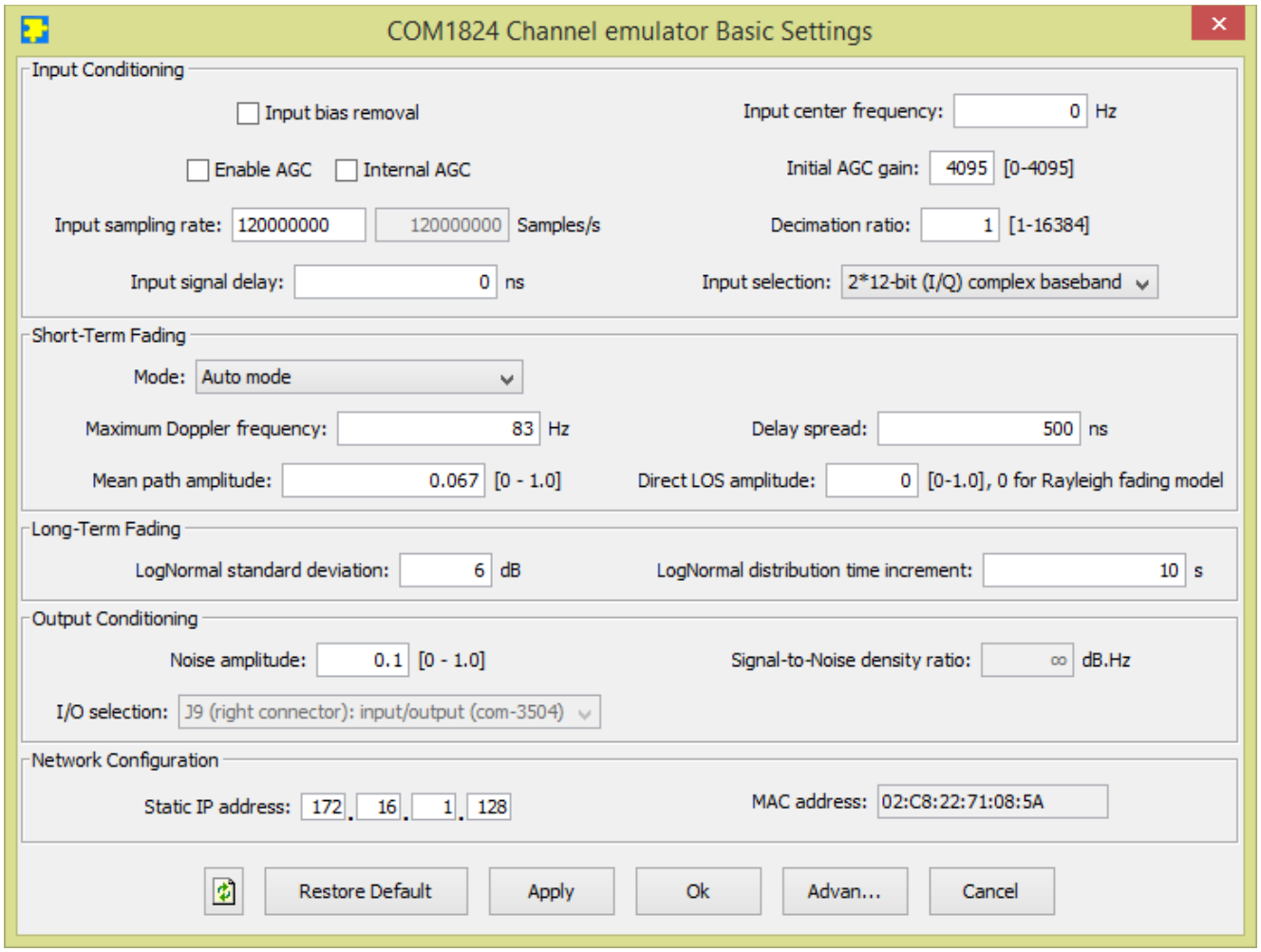
Configuration

Complete assemblies can be monitored and controlled centrally over a single built-in USB or Gigabit Ethernet LAN, or, when available, through adjacent ComBlocks connections.

The module configuration is stored in non-volatile memory.

Configuration (Basic)

The easiest way to configure the COM-1824 is to use the **ComBlock Control Center** software supplied with the module on CD. In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-1824 module to be configured, next click the *Settings* button to display the *Settings* window shown below.



This configuration is for Rayleigh fading, 1 GHz RF frequency, 25m/s speed, delay spread 0.5us (suburban area). LogNormal shadowing enabled, 6 dB attenuation standard deviation, updated once every 10 seconds. SNR = 10 dB within the 100 MHz bandwidth.

Maximum Doppler = 25/3E8*1GHz = 83 Hz
Mean path amplitude = 1/15 for each of the 15 indirect paths.

Total output signal power = (15 paths)*(1/15)^2*input power

Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center "Advanced" configuration or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

In the specific case of the COM-1824, each path delay, phase rotation, amplitude scaling coefficient can be controlled dynamically through a user-developed custom application program. A C-language code template is provided to help developers in this task.

All control registers are read/write.

Definitions for the Control registers are provided below.

Control Registers

The module configuration parameters are stored in volatile (SRT command) or non-volatile memory (SRG command). It is automatically loaded up at power up. All control registers are read/write.

Control registers REG0 through REG39 are fairly static and can thus be stored in non-volatile memory. The other control registers are dynamic in nature and should be written to volatile memory using the SRT command (because of the limit on Flash memory write cycles).

Undefined control registers or register bits are for backward software compatibility and/or future use. They are ignored in the current firmware version.

Parameters	Configuration
Input selection / format, test modes	Select the channel simulator input: 1 = 2*12-bit baseband complex samples 2 = 12-bit real samples on I-channel input. Q-channel input is zeroed. Use in the case of IF input. 7 = test mode, fixed input (turns into sinewave after subsequent frequency translation) REG0(2:0)
Receive sampling clock frequency f_{clk_adc}	ADC sampling clock. Expressed as as f_{clk_adc} = 20 MHz * M / (D * O)) where D is an integer divider in the range 1 - 106 M is a multiplier in the range 2.0 to 64.0 by steps of 1.0. Fixed point format 7.3 O is a divider in the range 2.0 to 128.0 by steps of 1.0. Fixed point format 7.3 Note: the graphical use interface computes the best values for M, D and O. Maximum value: 120 MHz REG13(6:0) = D REG14 = M(7:0) REG15(1:0) = M(9:8) REG16 = O(7:0) REG17(2:0) = O(10:8)

Bias removal enable	The bias removal circuit removes any spurious DC bias that may be introduced by an external A/D convert. Disable this function if the input signal includes a legitimate DC offset. 0 = disable 1 = enable REG0(7)
Spectrum inversion after center frequency translation	0 = no spectrum inversion 1 = spectrum inversion REG0(6)
Nominal Center frequency ($\mathbf{f}_{c\_rx}$)	The digital signal processing is implemented at baseband (near-zero center frequency). Therefore, the input signal must first be translated in frequency. Enter the expected center frequency of the input signal. 32-bit integer expressed as $\mathbf{f}_{c\_rx} * 2^{32} / \mathbf{f}_{clk\_rx}$. where $\mathbf{f}_{clk\_rx}$ is the input sampling rate. In the case of IF undersampling, the residual intermediate frequency can be removed here. For example, in the case of a 125 MHz IF signal sampled at 100 Msamples/s, the 25 MHz residual frequency is removed here by entering 0x40000000. REG1 = bit 7-0 (LSB) REG2 = bit 15 – 8 REG3 = bit 23 – 16 REG4 = bit 31 – 23 (MSB) Any change is enacted upon (re-)writing REG4

Internal AGC enable	Enable or disable the input automatic gain control 0 = disabled (unit gain) 1 = enabled REG5(0)
External AGC enable	0 = gain control fixed at a preset level (see below) 1 = enabled The analog gain control output is on pin J4.B13 REG5(1)
External AGC gain	Gain settings for an external variable gain amplifier. This setting is used when the external AGC is disabled. It is also the initial gain value before the AGC takes over. Unsigned 12-bit number. 4095 represents the minimum gain, 0 the maximum gain. REG5(7:4): LSB REG6: MSB
CIC decimation ratio **R**	Combined low-pass filter /.decimation. The decimation ratio R is set here. Valid range 1 to 16384. 0 is illegal. Usage: be careful not to decimate too much as the CIC decimation filter is not very sharp and thus can distort the modulation signal. For most applications, select R = 1. REG7: LSB[1] REG8(6:0): MSB
DDR3 SDRAM variable delay	The input signal can be delayed through the 1GB DDR3 SDRAM. The maximum delay is 256M complex samples. The delay is expressed as number of complex samples (after decimation by **R**). It must be an integer multiple of 8 complex samples. REG9 LSB REG10 REG11 REG12(3:0) MSB Any change is enacted upon (re-)writing REG4
AWGN noise amplitude N	Unsigned (positive) 16-bit precision amplitude scaling coefficient, expressed as a numerical value in 0.16 fractional binary format REG38 = N(7:0) REG39 = N(15:8)

[1] LSB = Least Significant Byte
MSB = Most Significant Byte

Multi-Path Fading Configuration (Auto mode)	
Mode	1 = clears all paths parameters such as amplitude scaling coefficients, delays, phase offsets, frequency offsets. Only the direct path amplitude is left unchanged. 2 = manual mode. User is responsible for defining the multi-path parameters. 3 = auto mode, single draw: multi-path random parameters are generated automatically for all paths. 4 = auto mode. Multi-path random parameters are periodically updated automatically for all paths. The update rate is approximately 20ms. REG20(2:0)
Maximum Doppler f_m	Maximum Doppler frequency in Hz. REG21 = bits 7 – 0 (LSB) REG22 = bits 15 – 8 REG23 = bits 23 – 16 (MSB)
Delay spread standard deviation Δ_τ	Expressed in ns. Note that, because of the exponential distribution, the mean equals the standard deviation. REG24 = bits 7 – 0 (LSB) REG25 = bits 15 – 8 REG26 = bits 23 – 16 (MSB)
Multipath amplitude mean.	Format 0.16 REG27 = bits 7 – 0 (LSB) REG28 = bits 15 – 8 (MSB)
Direct Path (line-of-sight) amplitude k_d	k_d is the direct, line-of-sight, component amplitude. The Rician Fading is disabled when k_d is set to zero. Format 0.16 REG30 = LSB REG31 = MSB
LogNormal distribution standard deviation σ_L	Standard deviation of the received power long-term fluctuation. Expressed in dB. The long-term power attenuation (in dBs) is a zero-mean Gaussian random variable. Set to 0 to disable the Lognormal shadowing. Format 8.8. (For example: 8.5 dB is represented as REG34/33 = 0x08 / 0x80) REG33 LSB REG34 MSB
LogNormal distribution Time increment T_L	Independent random values for the lognormal shadowing are computed once every T_L seconds. The actual attenuation is interpolated between two random draws. REG36

Multi-Path Fading Configuration (Manual mode)

Because of the dynamic (frequently changing) nature of these parameters, storing values in non-volatile registers is not recommended. Instead API users should use the "SRT" Set Register Temporary command.

Any change is enacted upon (re-)writing REG4

Parameters	Configuration
Coefficient W_i	Unsigned (positive) 16-bit precision coefficient. 16 coefficients are referred to by their path index i in the range 0 to 15. The amplitude scaling coefficient W_i are expressed as a numerical value in 0.16 fractional binary format (meaning 16 bits following the decimal point). Near unit gain is 0xFFFF. $REG_{40+8*i} = W_i (7:0)$ $REG_{41+8*i} = W_i (15:8)$
Delay D_i	Delay expressed as number of input samples. Valid range 0 – 511 samples. Path index i is in the range 0 to 15. $REG_{42+8*i} = D_i (7:0)$ $REG_{43+8*i} (0) = D_i (8)$
Phase Rotation φi	Phase rotation at the start of the simulation. As this is an initial condition, changes to the phase rotation are only enacted upon software reset. Unsigned 12-bit number representing a phase rotation in the range 0 (inclusive) to 360 degrees (exclusive) by steps of approximately 0.1 deg. Path index i is in the range 0 to 15. $REG_{43+8*i} (7:4) = φi (3:0)$
	$REG_{44+8*i} = φi (11:4)$
Frequency offset f_i	Signed 24-bit number. Computed as f_i /decimated sampling rate $*2^{32}$ For example, if the decimated sampling rate is 120 MHz, the frequency offset step size is 7.1 Hz. Path index i is in the range 0 to 15. $REG_{45+8*i} = f_i (7:0)$ $REG_{46+8*i} = f_i (15:8)$ $REG_{47+8*i} = f_i (23:16)$
Network Interface	
IP address	4-byte IPv4 address. Example : 0x AC 10 01 80 designates the default address 172.16.1.128 REG224 (MSB) – REG227(LSB)
Subnet mask	REG228 (MSB) – REG231(LSB)
Gateway IP address	REG232 (MSB) – REG235(LSB)
MAC addresses LSB	In order to ensure the uniqueness of MAC addresses, users can define bits 7:0 through REG236. The MAC addresses upper bits are automatically tied to the nearly unique FPGA DNA_ID. REG236(7:0).

Monitoring

Status Registers

Parameters	Monitoring
Hardware self-check	At power-up, the hardware platform performs a quick self check. The result is stored in status registers SREG0-7 Properly operating hardware will result in the following sequence being displayed: SREG0-SREG7 = 01 F1 1D xx 1F 93 10 22
Internal clocks	When the internal clocks and related PLLs are operating properly SREG21 = 1F
Input sampling rate	The input sampling rate is measured and displayed here. The frequency measurement accuracy is a function of the internal clock stability. The measurement is expressed in Hz. SREG8 = bit 7-0 (LSB) SREG9 = bit 15 – 8 SREG10 = bit 23 – 16 SREG11(2:0) = bit 26 – 24 (MSB)
AGC	SREG12 (LSB) SREG13(3:0) (MSB)
SNR calibration	
Received signal measured power	Power measurement of the received signal, after the multi-path channel. Averaged over 1K samples. SREG14(LSB) SREG15 SREG16(MSB)
Measured AWGN power (Noise bandwidth is the input sampling rate after decimation)	Power measurement of the AWGN, after applying the noise scaling factor specified in control registers REG28/REG29. Averaged over 1K samples. SREG17(LSB) SREG18 SREG19(MSB)
Saturation detection	'1' for saturation in any 1s window at the following test points: Bit 0: before SDRAM Bit 1: I-channel after multi-path Bit 2: Q-channel after multi-path Bit 3: AWGN I-channel Bit 4: AWGN Q-channel Bit 5: I-channel S+N Bit 6: Q-channel S+N SREG20
DDR3 SDRAM Monitoring	
Memory status	SDRAM memory ready SREG22(0)
SDRAM write pointer address	Current SDRAM write pointer address. Used to monitor the upload progress. When finished, the write pointer will point to the last address written to. Unit: number of SDRAM 64-bit words. SREG23 (LSB) – SREG26 (MSB)
SDRAM read pointer address	Current SDRAM read pointer address. Used to monitor the download progress. When finished, the read pointer will point to the last address read. Unit: number of SDRAM 64-bit words. SREG27 (LSB) – SREG30 (MSB)
TCP-IP Connection Monitoring	
MAC address	Unique 48-bit hardware address (802.3). In the form SREG31:SREG32:…:SREG36
TCP-IP server connection status	Bit 0 = port 1028 (M&C) connected SREG37(0)

Note: reading status register SREG7 latches multi-byte status words.

ComScope Monitoring

Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center.

Note: ComScope is not available when running a custom fading model on the PC as it would create conflicts on the monitoring and control link.

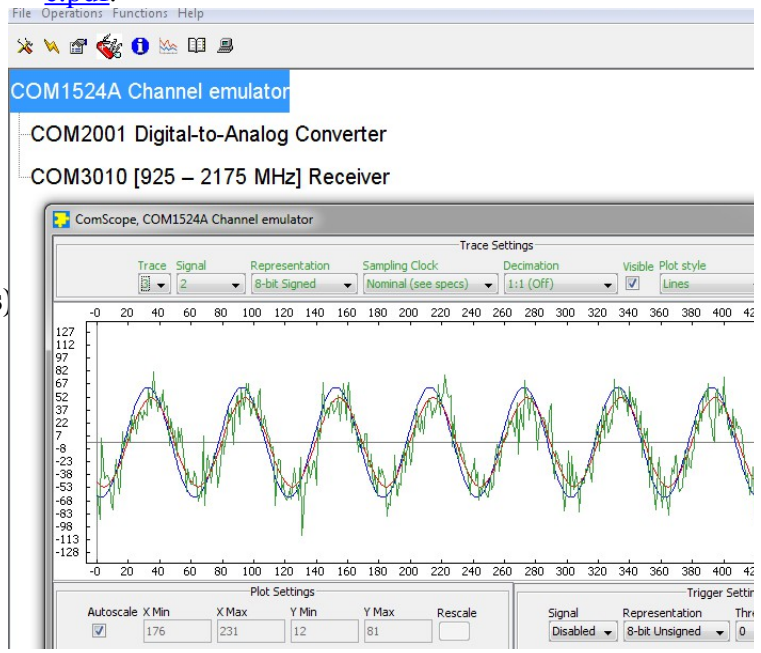
The COM-1824 signal traces and trigger are defined as follows:

Trace 1 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: Input signal I-channel	8-bit signed (8MSB/14)	Input sampling rate	512
2: Input signal (I-channel) after AGC, frequency translation, decimation	8-bit signed (8MSB/14)	Input sampling rate/R	512
3: Input signal (I-channel) after SDRAM delay	8-bit signed (8MSB/14)	Input sampling rate/R	512
4: I-channel after multi-path fading	8-bit signed (8MSB/18)	Input sampling rate/R	512
Trace 2 signals	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: Input signal Q-channel	8-bit signed (8MSB/14)	Input sampling rate	512
2: Input signal (Q-channel) after AGC, frequency translation, decimation	8-bit signed (8MSB/14)	Input sampling rate/R	512
3: Input signal (Q-channel) after SDRAM delay	8-bit signed (8MSB/14)	Input sampling rate/R	512
4: I-channel after multi-path fading	8-bit signed (8MSB/18)	Input sampling rate/R	512
Trace 3 signals	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: I-channel output	8-bit signed (8MSB/18)	Input sampling rate/R	512
2: Q-channel I-channel output	8-bit signed (8MSB/18)	Input sampling rate/R	512

Signals sampling rates can be changed under software control by adjusting the decimation factor and/or selecting the $\mathbf{f_{clk}}$ processing clock as real-time sampling clock.

In particular, selecting the $\mathbf{f_{clk}}$ processing clock as real-time sampling clock allows one to have the same time-scale for all signals.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.

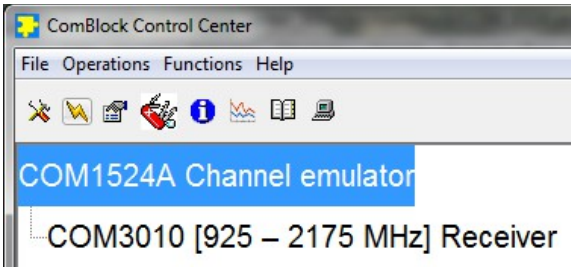


ComScope Window Sample

Getting Started

Software / Driver Installation

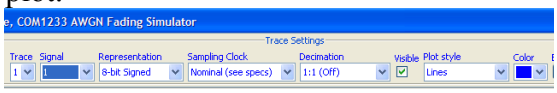
1. Install the ComBlock Control Center software (ComBlock_Control_Center_windows_3_13.exe or later) from the CD-ROM onto the host computer.
2. Connect a USB cable between the host computer and the COM-1824 module. The cable must be preferrably short (< 3 ft / 1m) and USB 2.0 approved.
3. Connect a 5V DC power supply to the ComBlock. Make sure that the hookup wire gauge is large enough not to cause any significant voltage drop between the power supply and the ComBlock s(AWG18 or below is recommended).
   The power supply should be rated for at least 2A.
4. Turn on the power. The first time a USB ComBlock is connected, the computer will ask the user to install a driver. In summary, point to the driver on the ComBlock CD-ROM in the \Windows Drivers\USB 2.0\Windows Driver folder. A step-by-step description is available on the CD-ROM USB20_UserManual.pdf
5. Start the ComBlock Control Center software. Select the communication medium by clicking on the first button from the left and select the USB (the COM-1824 must be powered for the choice to be enabled).
6. Verify that the communication between the host and the COM-1824 is established by clicking on the  button. A pop-up window will show "Detecting ComBlocks, Found 1 ComBlock so far".



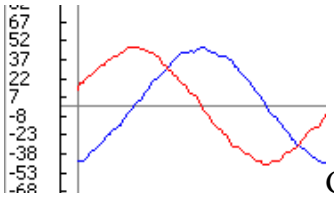
Verify Input Signal Integrity

It is a good practice in a new setup to verify the integrity of the high-speed digital signals going into and out of the COM-1824.

1. Send a known digital input signal to the COM-1824 (for example a sine/cosine).
2. Start the ComBlock Control Center.
   Detect ( button)
3. Start ComScope by highlighting the COM-1824 in the list and clicking on the ComScope button (6th button from the left).
4. Select trace 1, signal 1, 8-bit signed, nominal sampling clock, 1:1 no decimation, visible, line plot.



5. Select trace 2 signal 1 with the same attributes.
6. Click on the "Apply Changes" button, then on the "Re-arm trigger" button,
   then on the "Force trigger" button.
   Two traces will be plotted.
7. Verify that the sine/cosine traces are smooth without glitches (as illustrated below).



Glitches are indicative of timing problems between the source and the COM-1824 over the input cable.

Note: one can also do this test by connecting two COM-1824s back to back with the left-most ComBlock configured in internal tone test mode (see section below).

Verify Output Signal Integrity

The COM-1824 is designed with a built-in test signal generator to test the output connection.

1. Enable the internal test signal generator: click on the settings button and set the input selection to "Test mode: internal tone". Set the tone frequency in the field labeled "Input center frequency".
2. A test output signal consisting of a complex tone at full amplitude is generated and sent to the digital output connector J8.
3. At the receiving end of the cable, verify the integrity of the sine/cosine waveforms.

Save / Recover a Configuration

Configurations can be imported and exported into .stn settings file using the ComBlock Control Center File | Import and Export menu.

Operation

Sampling Rate

The input signal is not resampled (to avoid unnecessary aliasing) unless the user selects an integer decimation ratio greater than one. As the FPGA processing clock is fixed at 120 MHz, input sampling rate is limited to slightly less than 120 MHz. The output sampling rate equals the decimated input sampling rate.

When input decimation is used, it is preceded by anti-aliasing filters (CIC decimation filter + half-band filter).

Short-Term Fading

The short-term fluctuation in signal amplitude is due to multipath signals adding coherently in a constructive or destructive way. Even small changes in distance of the order of the wavelength can cause significant changes in amplitude at the receiver.

In essence, the COM-1824 is a real-time implementation of the following general multipath equation:

$$w(t) = \sum_{k=1}^{N} \alpha_k . z(t - \tau_k) . e^{-j2\pi(f_m \cos\psi_k + \varphi_k)t}$$

where
z(t) is the complex transmitted signal,
w(t) is the complex received signal,
N the number of paths,
α_k the k^{th} path amplitude,
τ_k the k^{th} path delay,
ψ_k the angle of incidence of the k^{th} received path with respect to the receiver motion,
φ_k an initial phase condition for the k^{th} path,
f_m the maximum Doppler frequency offset.

The user-specified parameters are

(a) The maximum Doppler frequency f_m, which is related to the transmitted radio frequency f_0 and the speed v of the receiver relative to the transmitter

$$f_m(Hz) = v(m/s).\frac{f_0(MHz)}{300}$$

(b) The delay spread Δ_τ, a function of the environment type: in-building, open area, suburban area, urban area, etc.

(c) The mean path amplitude.

α_k, τ_k , ψ_k , φ_k are random variables. For simplicity, these random variables are modeled as independent.

The delay spread τ_k is modeled as an exponential distribution with a probability density function expressed as

$$f(\tau) = \frac{1}{\Delta_\tau}.e^{-\tau/\Delta_\tau}$$

where
Δ_τ is the delay spread standard deviation, as specified by the user. Physically, this distribution expresses the fact that most of the multipath signals are grouped just after the earliest received signal. Signal with large delays are seldom received.

The initial phase condition φ_k is modeled as uniformly distributed over [0, 2π[.

The angle of incidence ψ_k is also modeled as uniformly distributed over [0, 2π[.

The path amplitude α_k is also modeled as an exponential distribution.

In the case when there exists a line-of-sight component (**Rician Fading**), the path index 0 represents the direct path between transmitter and receiver. The strength of the direct component $\alpha_0 = k_d$ is user-specified. To disable the LOS path, set k_d to zero.

When Rician Fading is enabled, the delay τ_0, the angle of incidence ψ_0 and the initial phase offset φ_0 are set to zero.

Long-Term Fading (Lognormal Shadowing)

The long-term variation in the mean received signal level is the result of movement over distances large enough to cause gross variations of the overall path between the transmitter and the receiver. For example, the receiver may move in or out of the shadow of surrounding objects like buildings and hills.

When long-term fading is enabled, the COM-1824 attenuates the complex received signal w(t) by L(t). When the attenuation L(t) is expressed on a log scale (in dBs), L(t) is a zero-mean Gaussian random variable with a standard deviation σ_L.

The time dependency of the attenuation L(t) is implemented by periodic independent random draws once ever T_L seconds. To prevent discontinuities, the attenuation L(t) is subject to a linear interpolation between two successive random draws.

The user-specified parameters are

(d) The standard deviation σ_L of the power attenuation L (in dBs)

(e) The time T_L between two independent random draws of L.

Users can disable the long-term fading by setting the standard deviation σ_L to zero.

Programming Template

Custom multi-path models can also be developed starting with the C-language templates supplied in the CD-ROM. The C-language template allows one to program delay, phase offset, frequency offset and amplitude scaling coefficients for each path. The connection between the host computer and the ComBlock assembly is assumed to be over USB or over a standard LAN/TCP-IP connection.

In the latter case, the client PC should open a TCP connection with the COM-1824 built-in TCP server at port 1028, then send text (ASCII) commands.

AWGN Algorithm

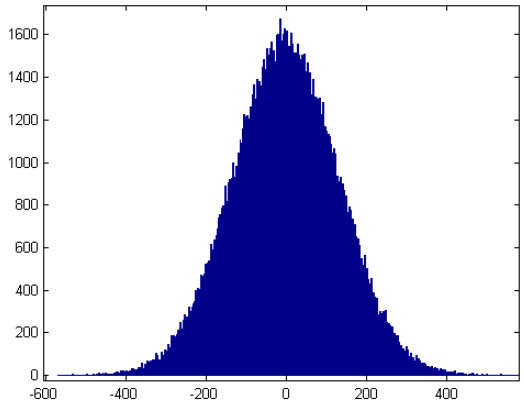
The Box-Muller algorithm is used to transform a uniformly distributed random variable to a Gaussian-distribution random variable. A description of the algorithm, together with an elegant FPGA implementation method can be found in reference [1].

The MATLAB program below illustrates how the algorithm works:

```
% Box Muller algorithm
verification
nsamples = 1000000;

% generate two independent
uniform distributed random
variables
x1 = rand(nsamples,1);
x2 = rand(nsamples,1);

% transform the
distributions
f = sqrt(-log(x1));
g = sqrt(2.0)*cos(2*pi*x2);

%gaussian distribution
n = f.*g;

% plot histogram
hist(n,500)

% standard deviation is 1.0
std(n)

% mean is zero
mean(n)
```

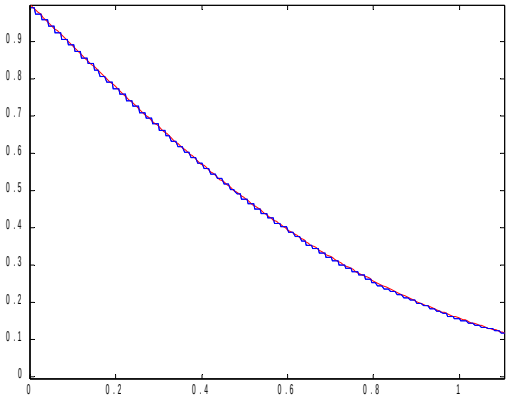
[1] “Efficient FPGA Implementation of Gaussian Noise Generator for Communication Channel Emulation”. Jean-Luc Danger, Adel Ghazel, Emmanual Boutillon, Hedi Laamari. 2002.

The resulting noise sample distribution is shown below:



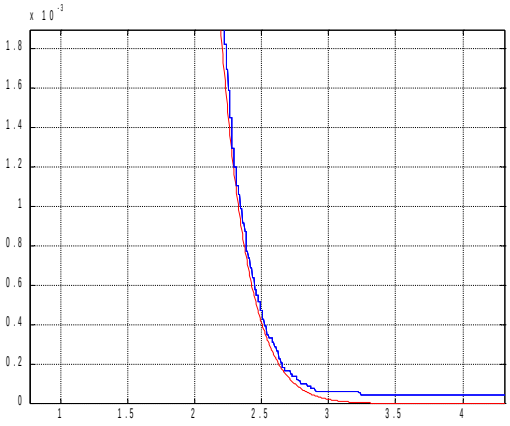
Noise sample histogram (130K samples)
Mean = 0.
Standard deviation = 128

The plots below illustrate how accurate the noise generation is, by comparing the erfc function (red) with the AWGN normalized distribution (blue)



Theoretical erfc function (red) vs actual AWGN normalized distribution measurements (blue). Range 0 – 1, 130K samples.

The theoretical curve and the measured statistical distribution of noise samples are nearly superposed.



Theoretical erfc function (red) vs actual AWGN normalized distribution measurements (blue). Range 1-4, 130K samples.

SNR Test Setup

In order to accurately set the signal to noise ratio, the following information must be known:

(a) received signal power S
(b) scaled noise power N
(c) received signal bandwidth B_s

The received signal power S and the scaled noise power N are measured by the COM-1824, using a running average over 1024 complex samples of the squared magnitude.

The received signal power is computed after the signal has been subject to multipath. The noise power is computed after the noise has been scaled by the user-defined scaling coefficients in control registers REG39/38.

The input signal bandwidth B_s must be known by the user.

The noise signal bandwidth equals the decimated input sampling rate, as all noise samples are statistically independent.

The signal to noise density ratio is
$S/N_0 = (S / N) * (\text{input sampling rate} /R)$
It is displayed in the control panel.

The SNR in the modulation bandwidth is
$S/N = S/N_0 * B_s$

Computation Overflow Detection

The COM-1824 module is intended to simulate linear channels. To maintain the linearity, it is essential to avoid any computation overflow condition which can occur in fixed-length digital signal processing. For most configurations and externally-supplied input signals, the COM-1824 ComBlock maintains the signal linearity throughout. In the rare cases when linearity cannot be preserved, the user should be made aware of it. For this reason, the COM-1824 includes several test points allowing the user to check linear operations.

To minimize the negative effects of overflow, overflow signals are clamped to the maximum (positive or negative) value. Overflow never causes a change in the signal sign.

Fractional Representation

Throughout this document, key signals are described in fractional binary format denoted by x.y. The total number of bits is x+y. The number of bits representing the numerical value below the decimal point is y. x denotes the number of bits representing the numerical value above the decimal point, including one bit for the sign in the case of signed values.

Examples:

Format	*Fractional representation*	*Decimal Equivalent*
1.17 signed	0.10000000000000000	0.5
1.17 signed	1.10000000000000000	-0.5

Options

Several interface types are supported through multiple firmware options. All firmware versions can be downloaded from www.comblock.com/download.

Changing the firmware option requires loading the firmware once using the ComBlock control center, then switching between the stored firmware versions The selected firmware option is automatically reloaded at power up or upon software command within 18 seconds

Option	Definition
-A	Input on left (J4) connector. (compatible with COM-30xx receivers) Output on right (J8) connector (compatible with COM-2001 dual DAC)
-B	Input/output on right (J8) connector. (compatible with COM-3504 dual Analog<->Digital conversion.
-E	J8 Right connector : 2*16-bit LVDS output samples. This interface is compatible with the COM-4009 broadband RF modulator.

Recovery

This module is protected against corruption by an invalid FPGA configuration file (during firmware upgrade for example) or an invalid user configuration. To recover from such occurrence, connect a jumper in J3 prior and during power-up. This prevents the FPGA configuration and restore communication. Once this is done, the user can safely re-load a valid FPGA configuration file into flash memory using the ComBlock Control Center.

Electrical Interface

Digital Input (J4) Option --A	Definition
DATA_I_IN[11:0] DATA_Q_IN[11:0]	Input signal, real and imaginary axes. 12-bit precision. Unsigned format. Unused LSBs are pulled low.
SAMPLE_CLK_IN	Enable signal. Can be continuously high (in which case all input samples are valid) or CLK_IN-wide pulse. Read the input signal at the rising edge of CLK_IN when SAMPLE_CLK_IN = '1'. Signal is pulled-up.
CLK_IN	Input reference clock for synchronous I/O. RX_DATA_x_IN and RX_SAMPLE_CLK_IN are read at the rising edge of CLK_IN. Maximum 105 MHz.
AGC_OUT	Output. When this demodulator is connected directly to an external receiver (COM-300x), it a 0 – 3.3V signal to control the gain prior to A/D conversion. The purpose is to use the maximum dynamic range while preventing saturation at the A/D converter. 0 is the maximum gain, +3.3V is the minimum gain.

Monitoring & Control	Definition
USB 2.0	Type B receptacle. This interface is used only for monitoring and control. Use USB 2.0 approved cable for connection to a host computer. Maximum recommended cable length is 3'.
TCP IP server over gigabit Ethernet LAN (GbE)	10/100/1000 Mbps Ethernet LAN through RJ45 connector. Supports auto MDIX to alleviate the need for crossover cable. The COM-1824 comprises a TCP server at port 1028 for the sole purpose of monitoring and control. The TCP server listens for a connection request from a remote TCP client (PC). Once the TCP connection is established, the client can send or receive M&C text (ASCII) messages. No programming is needed when using the supplied ComBlock Control Center. Custom applications can be developed using standard TCP socket programming.
Power Interface	4.75 – 5.25VDC. Terminal block. The maximum current consumption is 1.5A.

Use of the COM-1824 requires an oversized power supply capable of supplying a peak current of 2A for a very short period (5ms). Hook-up cable should be 18AWG or thicker to minimize voltage drop between power supply and terminal block.

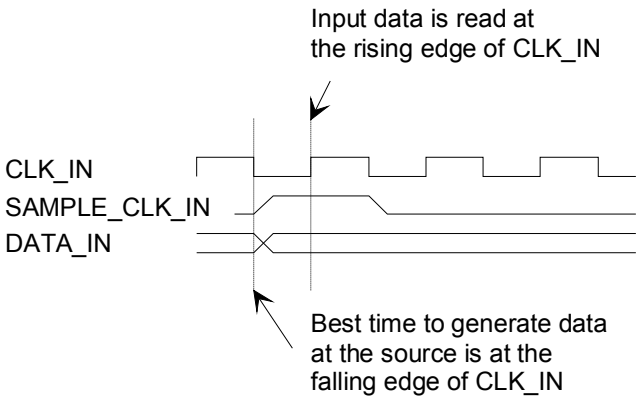
Absolute Maximum Ratings

Supply voltage	-0.5V min, +6V max
40-pin connector inputs (LVTTL)	-0.5V min, +3.6V max
40-pin connector inputs (LVDS)	-0.5V min, +2.8V max

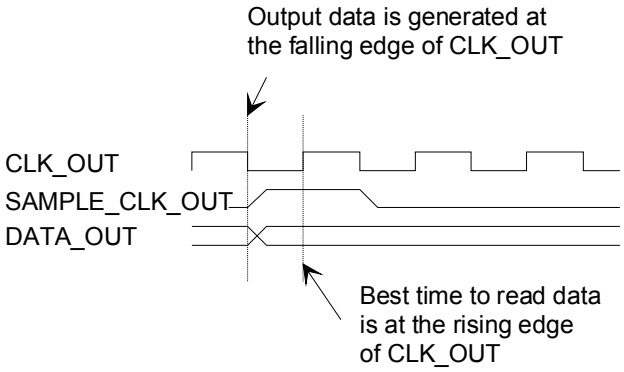
Important: Inputs are NOT 5V tolerant!

Timing

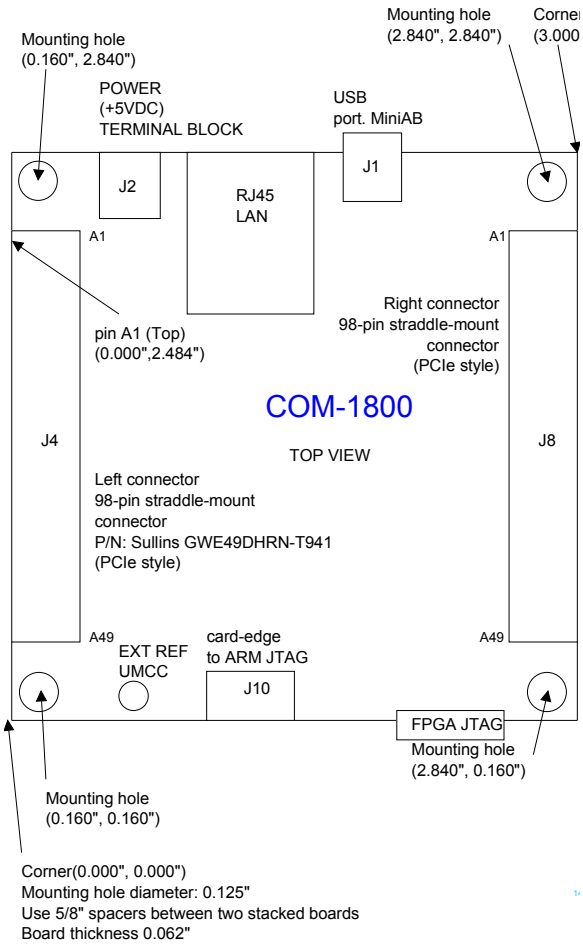
LVTTL Synchronous Serial Input

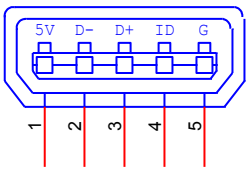


LVTTL Synchronous Serial Output



Mechanical Interface





Schematics

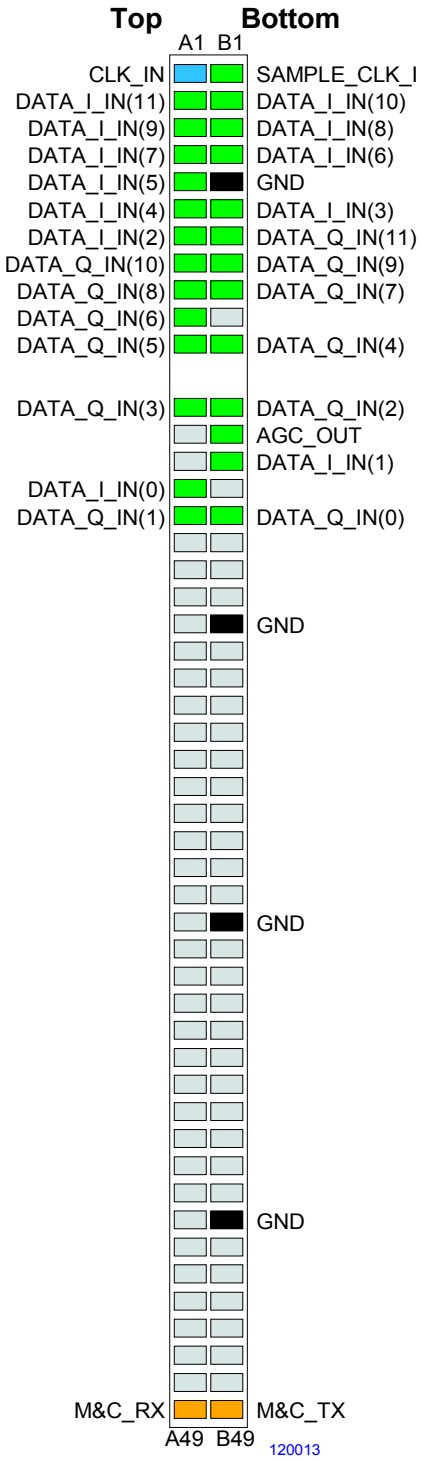
The board schematic is available on-line at ComBlock.com/download/com_1800schematics.pdf

Pinout

USB

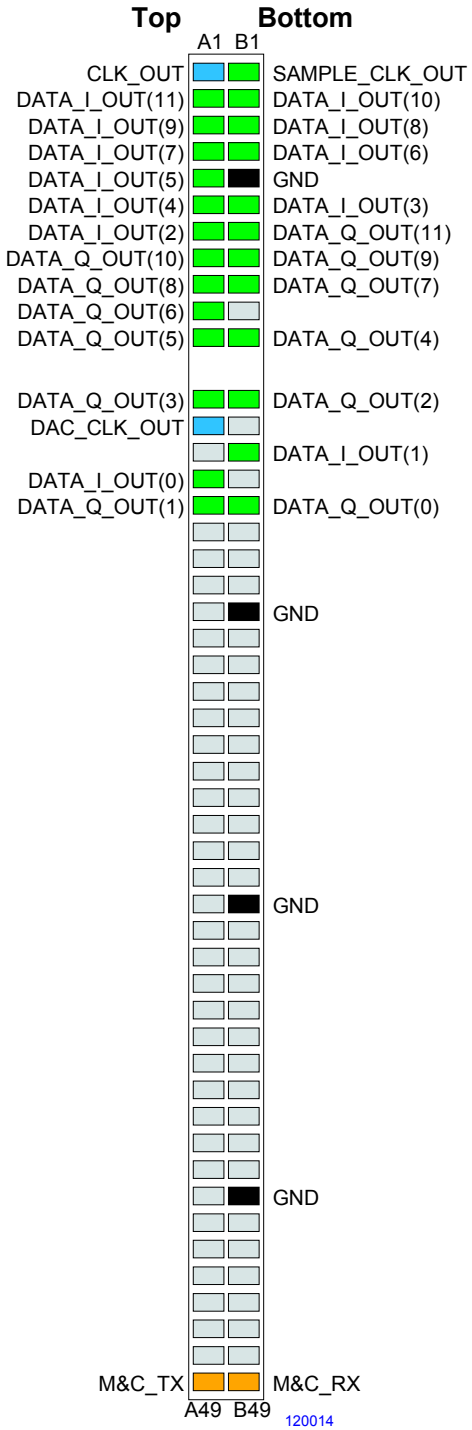
Both USB ports are equipped with mini type AB connectors. (G = GND). In both cases, the
COM-1824 acts as a USB device.

Left Connector J4

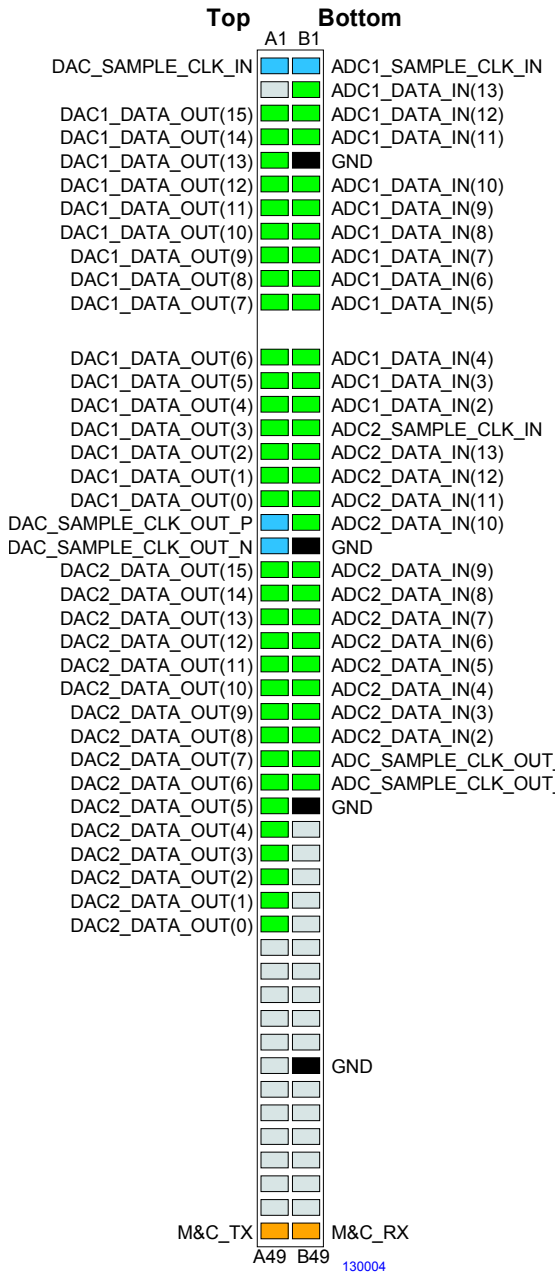


Firmware Option **-A**. Input compatible with COM-30xx receivers.

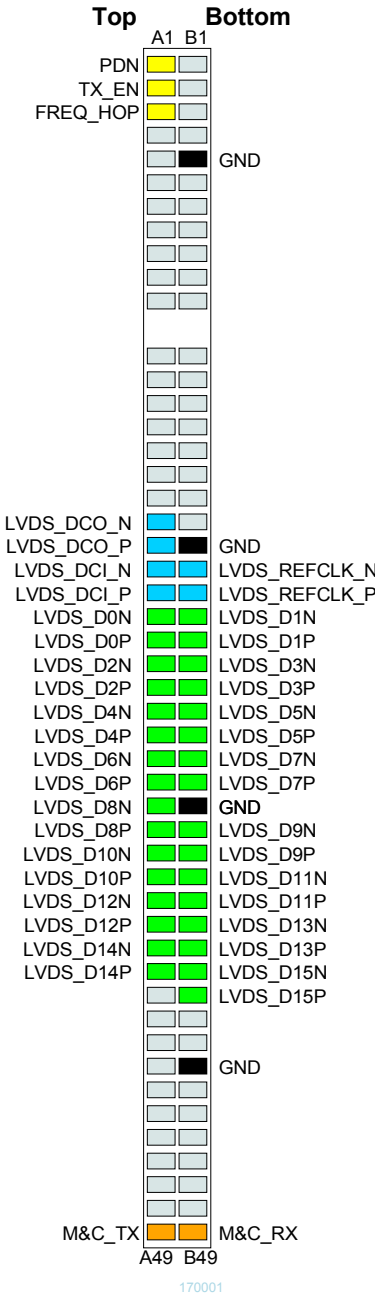
Right Connector J8



Firmware Option **-A**. This interface is compatible with the COM-2001 dual DACs.



Firmware Option **-B**. This interface is compatible with the COM-3504 dual Analog<->Digital Conversions.



Firmware Option **-E** 2*16-bit output samples (2's complement). This interface is compatible with the COM-4009 RF modulator

Configuration Management

This specification is to be used in conjunction with VHDL software revision 1.

The VHDL code was developed using Xilinx Vivado.

Compatibility List

(Not an exhaustive list)

Left connector (J4)
COM-1800 FPGA (XC7A100T) + ARM + DDR3 SODIMM socket + GbE DEVELOPMENT PLATFORM [2]
–A firmware
COM-30xx RF/IF/Baseband receivers for frequencies ranging from 0 to 3 GHz.
Right connector (J8)
–A firmware
COM-2001 digital-to-analog converter (baseband).
–B firmware
COM-3504 Dual Analog <-> Digital Conversions
–D firmware
COM-4009 digital to [400MHz – 4.4GHz] broadband RF modulator

ComBlock Ordering Information

COM-1824 Channel Emulator

ECCN 5B001.a

MSS • 845-N Quince Orchard Boulevard•
Gaithersburg, Maryland 20878-1676 • U.S.A.
Telephone: (240) 631-1111
Facsimile: (240) 631-1676
E-mail: sales@comblock.com

[2] 98-pin to 40-pin adapters to interface with other Comblocks are supplied free of charge. Please let us know about your interface requirements at the time of order.