COM-1826SOFT_TX TDRSS DSSS Transmitter VHDL source code overview / IP core

Overview

The COM-1826SOFT_TX is a NASA/TDRSS-compliant Direct Sequence Spread-Spectrum (DSSS) transmitter written in generic VHDL.

The entire **VHDL source code** is deliverable. It is portable to a variety of FPGA targets.

Key features and performance:

- TDRSS spread-spectrum digital modulator including
  - BPSK and SQPN spread-spectrum modulation
  - Programmable 1023- (forward command link) or 2047-chip (return mode 2 link) periodic I and Q Gold codes
  - Programmable bit rates from 1 to 150 Kbits/s independent on each channel.
  - Convolutional/Viterbi error correction: K=7 Rate ½
  - NRZ conversion
  - Digital baseband I/Q output to external DAC
  - 3 types of baseband modulated output waveforms: digital word to DAC, tab-delimited text file, NASA SDDS formatted stream.
- Provided with IP core:
  - VHDL source code
  - Matlab signal generation .m program for generating baseband waveforms.
  - PRBS11 test sequence generator, AWGN noise generator

Configuration

Synthesis-time configuration parameters

The following constants are user-defined in the *COM1826_TX.vhd* component generic section prior to synthesis. These parameters generally affect the size of the transmitter embodiment.

Synthesis-time configuration parameters	Configuration
AWGN_INST	Additive White Gaussian Noise generator instantiation (1). (0) during operations to save space in FPGA (and to increase clock speed.
SIMULATION	(1) to use *COM1826_TX.vhd* as its own testbed, with internal clock generation. (0) during deployment or when in use with external testbeds such as *tbcom1826_tx.vhd*

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Run-time configuration parameters

The user can set and modify the following controls at run-time through the top level component interface:

Tx Parameters	Configuration
NRZ1_TX_CONTROL (2:0) **NRZ2_TX_CONTROL (2:0)**	Converts NRZ-L to NRZ-L/M/S Two converters, for I and Q channels respectively 000 = NRZ-L unchanged 001 = NRZ-L to NRZ_M 010 = NRZ-L to NRZ_S
FEC_ENCODER_ENABLED (1:0)	Independent convolutional encoder control for each I/Q channels Bit 0: I-channel Bit 1: Q-channel (0) disabled/bypassed, (1) enabled
CHIP_RATE (32:0)	Chip rate expressed as 2^32* chip rate / f_{CLK} Chip rate must be strictly less than $f_{CLK}/2$. Typically 3.077799479166 Mchips/s for TDRSS SMA
SYMBOL_RATE1(31:0) **SYMBOL_RATE2(31:0)**	Two symbol rates, for I and Q channels respectively. Symbol rate expressed as 2^32* symbol rate / f_{CLK}
LFSRA_INIT(10:0) **LFSRC_INIT(10:0)**	Gold code selection as spreading sequence. LFSR initialization. see definition in Space network interoperable pn code libraries, Appendix A
CODE_MODE	0 = forward command link Gold codes 1 = return mode 2 link Gold codes
MOD_SIGNAL_GAIN (15:0)	Output scaling factor to modulator output (excluding added noise). 16-bit unsigned.
NOISE_GAIN(15:0)	Additive White Gaussian Noise level (amplitude) for test purposes. Generic parameter AWGN_INST must be '1'.
	16-bit unsigned
CENTER_FREQ(31:0)	Modulated signal center frequency. Expressed as 2^32 * fc/ f_{CLK}
MOD_CONTROL(15:0)	bit 0: spectrum inversion enabled (1) or not (0) bit 1: BPSK (0) vs SQPN(1) bit 2: dual source (0), or identical data on I/Q (1) bit 3: (1) when 1/2 symbol delay added on Q bit bit 4: enable (1)/disable (0) the modulated signal bit 5: unused bit 6: When enabled, the input data stream is demultiplexed into the I and Q paths. The symbol rate must be identical on both I and Q channels. Two independent FEC encoders are used on the I and Q paths respectively. Enabled(1)/Disabled(0) bit 7: output spectrum shaping filter (square root raised cosine) bypass (1) or enable (0) bits 9:8: test mode: 00 no test, 01 = PRBS11, 10 = unmodulated carrier bit 10: (1) to enable sync word and/or preamble insertion. (0) to disable both. bit 11: spreading enabled(1) / disabled(0) bit 12: differential modulation (1) bits 15:13: unused
CONFIG_CHANGE_TOGGLE	toggle upon changing the above settings

I/Os

General

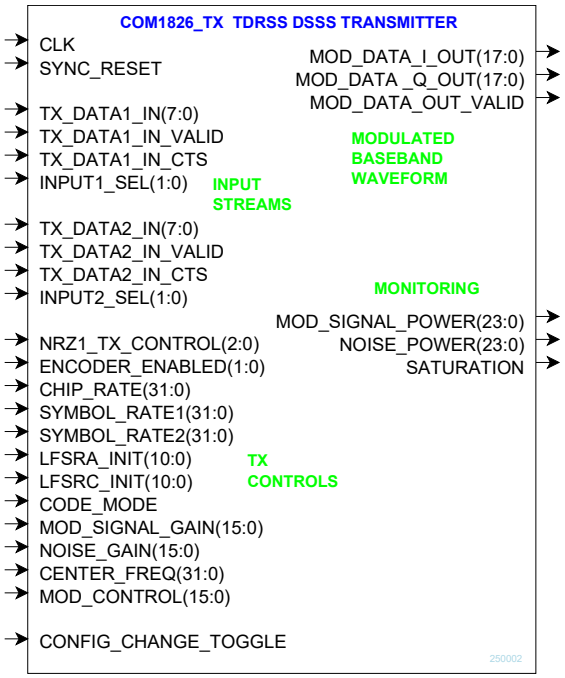
All signals are synchronous with a single input clock **CLK_IN** which also serves as DAC sampling clock for the baseband modulated output.

The clock period must be constrained in the constraint file (.xdc for Xilinx Vivado) associated with the project.

This clock must be global clocks (i.e. use BUFG before supplying the clock to the transmitter).

A synchronous reset **SYNC_RESET** must be supplied. The recommended use is to keep the reset high until the input clock is stable (i.e. PLL or MMCM locked).

Transmitter



Data Path

The x indices 1 and 2 refer to the I and Q channels respectively.

TX_DATAx_IN: 8-bit wide input data for the I(x=1) or Q(x=2) channel respectively. Bit order: MSb first. Read when **TX_DATAx_IN_VALID**= '1'

The user must check the "Clear To Send" flow control signal first before sending the next input Byte.

TX_DATAx_IN_VALID:1 CLK-wide input pulses indicating that the associated **TX_DATAx_IN** input Byte is valid.

TX_DATAx_IN_CTS: output.
Clear-To-Send flow control signal. '1' indicates that the transmitter is ready to accept another input byte. Thanks to an input elastic buffer, the data source is allowed to send a few more bytes after the CTS signal goes low, so timing is generally not critical.

INPUTx_SEL(1:0): input selection for the I and Q channels.
00 = no input
01 = user input
10 = internally generated PRBS11 test sequence
11 = zeros

Software Licensing

This software is supplied under the following key licensing terms:

1. A nonexclusive, nontransferable license to use the VHDL source code internally, and
2. An unlimited, royalty-free, nonexclusive transferable license to make and use products incorporating the licensed materials, solely in bit stream format, on a worldwide basis.

The complete VHDL/IP Software License Agreement can be downloaded from
http://www.comblock.com/download/softwarelicense.pdf

Portability

The VHDL source code is written in generic VHDL and thus can be ported FPGAs from various vendors.

Configuration Management

The current software revision is 062025.

Directory	Contents
/doc	Specifications, user manual, implementation documents
/src	.vhd source code,.pkg packages, .xdc constraint files (Xilinx) One component per file.
/sim	VHDL test benches
/matlab	Matlab .m program generating stimulus files for VHDL simulation and for end-to-end BER performance analysis at various signal to noise ratios

Project files:

Xilinx Vivado v2020 project files:
project_1/project_1txvivado2020.xpr
project_1/project_1txvivado2020.tcl

VHDL development environment

The VHDL software was developed using the following development environment:
Xilinx Vivado 2020 for synthesis, place and route and VHDL simulation

Device Utilization Summary

Transmitter device utilization (no AWGN)
Device: Xilinx xc7a100tfgg484-1

Resource	Estimation	Available	Utilization...
LUT	4258	63400	6.72
LUTRAM	41	19000	0.22
FF	8016	126800	6.32
BRAM	5.50	135	4.07
DSP	12	240	5.00
IO	305	285	107.02
BUFG	1	32	3.13

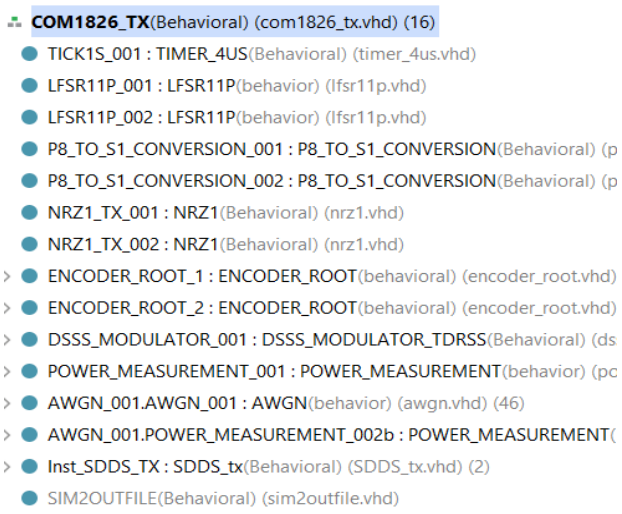
Clock and decoding speed

The entire design is synchronous with the CLK_IN input clock (must be a global clock). A low speed grade Artix7 is sufficient.
Typical maximum clock frequencies for representative FPGA families are listed below:

Device family	**Transmitter**
AMD Artix7 100T -1 speed grade	161 MHz
Xilinx Kintex7 ultrascale+ -1 speed grade	341 MHz

VHDL components overview

Top level



COM1826_TX.vhd is the transmitter top level component. Inputs consist of one or two streams. The output is a complex baseband modulated signal interpolated to one sample per CLK. Internal processing comprises NRZ conversion, convolutional encoding, DSSS modulation and final interpolation.

The input data stream is user-selected among either external input data or internal PRBS-11 pseudo-random test sequence (*LFSR11P.vhd*). The latter is useful in measuring end-to-end tx-rx BER.

The *NRZ1.vhd* component is useful in converting NRZ-M/L/S formats to NRZ-M/L/S.

The *ENCODER_ROOT.vhd* component performs various convolutional encoding. Two such components can be used for the I and Q channel independently.

DSSS_MODULATOR_TDRSS.vhd performs the spread-spectrum modulation, root raised cosine filtering, fine frequency translation, level control, and interpolation.

FIRRCOS20.vhd is a 20-tap root raised cosine filter operating at 2 samples/chip.

DIGITAL_DC2.vhd implements a digital center frequency translation to fine-tune the output center frequency.

Ancillary components

LFSR11P.vhd is a pseudo-random sequence generator used for test purposes. It generates a PRBS11 test sequence commonly used for bit error rate testing at the receiving end of a transmission channel.

AWGN.vhd generates a precise Additive White Gaussian Noise. The noise bandwidth is 2*symbol rate.

BRAM_DP2.vhd is a generic dual-port memory, used as input and output elastic buffers. Memory is inferred (no Xilinx primitive is used).

SIM2OUTFILE.vhd writes modulated output waveform to a tab-delimited file (`com1826_tx.txt`) which can be subsequently read by Matlab (load command) for plotting or analysis. This output file can also be used as input waveform for the receiver testbench `tbcom1826_rx.vhd`. Set SIMULATION to '1' to enable this feature.

Alternatively, the modulated output waveform can be formatted as NASA/SDDS on an Ethernet LAN using the `sdds_tx.vhd` component.

VHDL simulation

VHDL testbenches are located in the /sim directory.

The `tbcom1826_tx.vhd` sends two PRBS-11 test sequences through the transmitter . The output consists of modulated complex baseband samples. It generates the clock, reset and configures the transmitter for chip rate, symbol rates, NRZ conversion, spreading code selection, transmit level, center frequency, etc.

Matlab simulation

The `siggen_tdrss.m` is a matlab program to generate a TDRSS spread-spectrum modulation waveform, saved into a file which can serve as a stimulus input to a receiver. It is functionally equivalent to the `tbcom1826_tx.vhd` VHDL testbed.

Reference documents

[1]] Space Network Users Guide; Rev 10

Acronyms

Acronym	Definition
AWGN	Additive White Gaussian Noise
CTS	Clear-To-Send flow control flag
DAS	Demand Access System
DSSS	Direct Sequence Spread Spectrum (modulation)
FPGA	Field Programmable Gate Array
GbE	Gigabit Ethernet
LFSR	Linear Feedback Shift Register
LSb	Least Significant bit in a word
MSb	Most Significant bit in a word
RF	Radio Frequency
rx	Receive
SDDS	Signal Data Distribution Standard
SQPN	Staggered Quadriphase PN (spread-spectrum modulation)
SRRC	Square Root Raised Cosine (filter)
TDRSS	Tracking and Data Relay Satellite System
tx	Transmit

ComBlock Ordering Information

COM-1826SOFT_TX TDRSS DSSS transmitter, VHDL source code / IP core

ECCN: EAR99

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