COM-1831SOFT
Burst mode Spread-Spectrum modem
VHDL source code overview / IP core

Overview

The COM-1831SOFT is a burst-mode direct-sequence spread-spectrum modem for transmitting and receiving UDP data frames over a wireless or cable medium. It not only includes the DSSS modulation and demodulation functions, but also ancillary functions such as error correction, internet protocol stack and Ethernet MAC.

The chip rates, symbol rates, spreading Gold code, and center frequency are fully programmable at run time. Several other generic parameters allow one to customize the code for the target application. Frame length, frequency acquisition range, acquisition threshold, preamble length, number of parallel code search circuits are all adjustable prior to code synthesis.

The entire **VHDL source code** is deliverable.

Key features and performance:

- Burst mode operation:
  - Fixed-length data frames from/to LAN/UDP ports
  - Multiple frames transmitted efficiently with only 32-symbol separation.
- Acquisition: 1600-symbol preamble with no apriori knowledge of arrival time
- Large frequency acquisition range: ±(chip_rate / 64) or (1.8*symbol_rate), whichever is smaller, with no apriori knowledge.
- End-to-end latency: 2672 symbol / modulation symbol rate. For example 1.2ms at 2.5Msymbols/s.
- Programmable chip rate, up to 79.5 Mchips/s (limited by FPGA technology XC7A100T-1)
- 2047-chip Gold codes
- Data rate practical range from chip_rate/2047 to chip_rate/30
- Built-in tools: PRBS-11 pseudo-random test sequence, BER tester, AWGN generator, and internal loop back mode.
- Monitoring:
  - Carrier frequency error
  - SNR
  - BER
- Provided with IP core:
  - VHDL source code
  - VHDL test bench with PRBS11 sequence generator and bit error rate measurement.
  - Java code to send UDP frames

Target Hardware

The code is written in generic standard VHDL so as to be ported to a variety of FPGAs. It was compiled and simulated using Xilinx Vivado v2015.2 tools.

It was tested on Xilinx 7-series FPGA (Artix7-100T)

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Configuration

Synthesis-time configuration parameters

The following constants are user-defined in the generic section of the encoder and decoder components prior to synthesis. These parameters generally define the size of the decoder embodiment.

Parameters	Configuration
Tx payload length (in bits) **MOD_PAYLOAD_LENGTH**	Typically 512 bits (no FEC) or 1040 (with FEC), but can be changed as needed
Rx payload length (in bits) **DEMOD_PAYLOAD_ LENGTH**	Typically 512 bits (no FEC) or 1040 (with FEC), but can be changed as needed
32-bit sync word **SYNC_WORD**	Baseline 0x5A0FBE66
FEC encoder code selection **ENC_CODE_SEL**	Baseline K=9, rate ½ See COM-1510SOFT for the full range of convolutional FEC codes.
FEC decoder code selection **DEC_CODE_SEL**	Baseline K=9, rate ½ See COM-1510SOFT for the full range of convolutional FEC codes.
Number of parallel code acquisition circuits **NACQ = NMUX * NACQ_DIV**	**NACQ** parallel circuits accelerate the search for the receiver code replica to match the received signal's. Trade-off acquisition time versus FPGA occupancy. Because of a timing constraint, these circuits are divided into **NMUX** groups of **NACQ_DIV** circuits. See comments within the burst_dsss_demod.vhd code regarding the timing constraints to select **NMUX** and **NACQ_DIV**
Non-coherent integration & dump period **N_NCID**	Trade-off acquisition time versus threshold C/No
First preamble extension **FIRST_PREAMBLE_ EXTENSION**	Modulator-inserted preamble length, expressed in number of symbols. Baseline: 1600. The preamble must be long enough for the demodulator to acquire the burst prior to the payload field. Depends on **NACQ**, **N_NCID** and threshold C/No.
Enable internal additive white Gaussian noise generation **AWGN_EN**	Generally not needed during operations. Useful during development testing as it eliminates the need for an external noise generator.
BER tester measurement window **BER_CONTROL(2:0)**	Baseline: 10,000 bits ("001")

Run-time configuration parameters

The user can set and modify the following controls at run-time through the top-level component interface:

Parameters	Configuration
Tx	
Modulator clock frequency	**CLK_TX_GEN_D,_M,_O** The modulator clock **CLK_TXg** frequency must be programmable dynamically (see CLKGEN7_MMCM_DYNAMIC) for fine control of the chip rate.
Chip rate	**MOD_CHIP_RATE_NDIV** The modulator chip rate is in the form $f_{chip\_rate\_tx} = f_{clk\_tx} / 2^n$ where n ranges from 1 (2 samples per chip) to 15 (chip rate = f_{clk_tx} / 32768).
Symbol rate	**MOD_SYMBOL_RATE1** The I-channel symbol rate can be set independently of the spreading code period as $f_{symbol\_rate} * 2^{32} / f_{clk\_tx}$
Spreading code	The I-channel Gold code is selected through the linear feedback shift register initialization. **MOD_LFSRA_INIT**
Output center frequency	**MOD_CENTER_FREQ** The modulated signal center frequency can be shifted in frequency 32-bit signed integer (2's complement

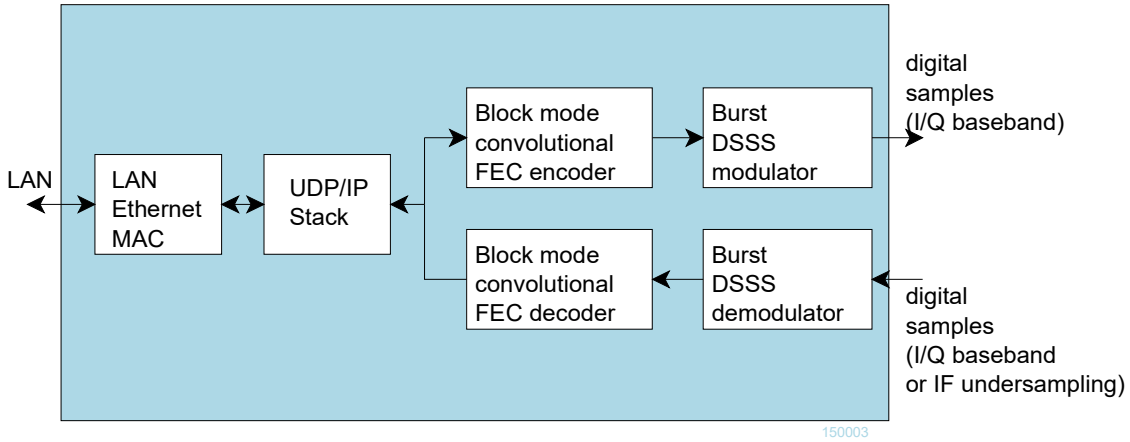
	representation) expressed as $f_c * 2^{32} / f_{clk\_tx}$
Output level	**MOD_GAIN** 16-bit amplitude scaling factor for the modulated signal. The maximum level should be adjusted to prevent saturation. The settings may vary slightly with the selected chip rate. Please check for saturation (see test points) when changing either the chip rate or the signal gain.
Rx	
CIC decimation factor	**CIC_R** Receiver decimation factor from f_{clk_adc} to 4* $f_{chip\_rate\_rx}$. Valid range 1 - 16384
Nominal chip rate	**NOMINAL_CHIP_RATE** 32-bit integer expressed as $f_{chip\_rate\_rx} * 2^{32} / f_{clk\_adc}$. The maximum practical chip rate is f_{clk_adc} /2. The maximum allowed error between transmitted and received chip rate is +/- 100ppm.
Symbol rate	**NOMINAL_SYMBOL_RATE1** Nominal I-channel symbol rate, defined as $f_{symbol\_rate\_i} * 2^{32} / f_{clk\_adc}$
Spreading code	The I-channel Gold code is selected through the linear feedback shift register initialization. **LFSRA_INIT**
Nominal input center frequency	**RECEIVER_CENTER_FREQ** The nominal center frequency is a fixed frequency offset applied to the input samples. It is used for fine frequency corrections, for example to correct clock drifts. 32-bit signed integer (2's complement representation) expressed as $f_c * 2^{32} / f_{clk\_adc}$
Loopback mode	**LOOPBACK_MODE** Binary flag to connect the modulated output (possibly including noise and frequency offset) to the receiver input within the FPGA.
Receiver AGC response	**RECEIVER_AGC_RESPONSE** Users can to optimize AGC response time while avoiding instabilities (depends on external factors such as gain signal filtering at the RF front-end and chip rate). The AGC_DAC gain control signal is updated as follows 0 = every chip, 1 = every 2 input chips, 2 = every 4 input chips, 3 = every 8 input chips, etc…. 10 = every 1000 input chips. Valid range 0 to 14.

Operation

See www.comblock.com/download/com1831.pdf [1] or www.comblock.com/download/com1931.pdf [5] for a detailed description of the modem operation.

Limitations

1. The spreading factor (chip rate / symbol rate) must be in the range 30 to 2047



Functional block diagram

Software Licensing

The COM-1831SOFT is supplied under the following key licensing terms:

1. A nonexclusive, nontransferable license to use the VHDL source code internally, and
2. An unlimited, royalty-free, nonexclusive transferable license to make and use products incorporating the licensed materials, solely in bitstream format, on a worldwide basis.

The complete VHDL/IP Software License Agreement can be downloaded from http://www.comblock.com/download/softwarelicense.pdf

Configuration Management

The current software revision is 1.

Directory	Contents
/doc	Specifications, user manual, implementation documents
/src	.vhd source code. One component per file.
/sim	Test benches
/bin	.bit files
/java	Java source code to send UDP frames

Key files:

Xilinx Vivado project file: /project1/project_1.xpr

VHDL development environment

The VHDL software was developed using the following development environment for VHDL synthesis and VHDL simulation.

(a) Xilinx Vivado 2015.2

The size is compatible with the free Xilinx WebPack tools.

Ready-to-use Hardware

The COM-1831SOFT was developed on, and therefore ready to use on the following commercial off-the-shelf hardware platform:

FPGA development platform
COM-1800 FPGA Artix7-100T + GbE + DDR3 socket + ARM development platform
COM-1931 L/S-band transceiver
Analog
COM-3504 Dual Analog <-> Digital Conversions
COM-3506 [400 MHz – 3GHz] RF transceiver

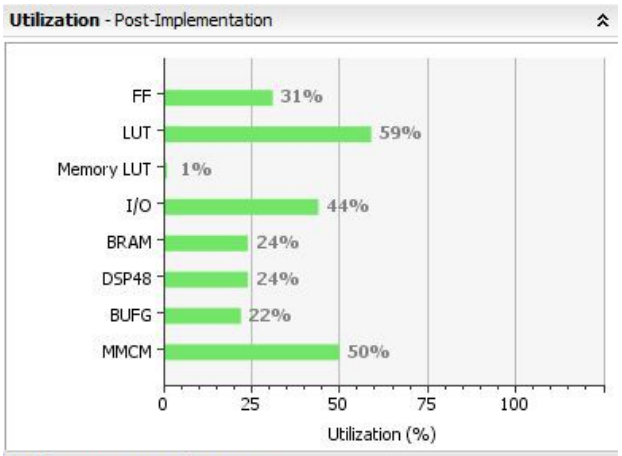
Device Utilization Summary

The implementation size depends essentially on two key user-defined parameters in the generic section of the demodulator, namely:

- The number of parallel code acquisition circuits **NACQ**
- The FEC code constraint length K selected through the **DEC_CODE_SEL** parameter (K=9 is the largest implementation)

Device: Xilinx Artix7-100T

NACQ = 48, K = 9 convolutional codec, 160 MHz ADC clock, 80-160 MHz DAC clock



Utilization - Post-Implementation

Resource	Utilization	Available	Utilization %
FF	39223	126800	30.93
LUT	37140	63400	58.58
Memory LUT	85	19000	0.45
I/O	124	285	43.51
BRAM	33	135	24.44
DSP48	57	240	23.75
BUFG	7	32	21.88
MMCM	3	6	50.00

Clock and decoding speed

The design uses three different clocks, all locked onto either a 10 MHz or a 19.2 MHz external frequency reference, as selected by the **OPTION** generic parameter. Other frequency references can also be used by changing the *CLK_GEN_MMCM_ADJ.vhd* multiply, divide and period parameters.

CLK_ADCg: Fixed frequency analog-to-digital converter sampling clock. Drives the external ADCs. Controls the maximum receive chip rate.

CLK_TXg: Dynamically programmable DAC sampling clock. Used for fine control of the chip rate. Drives the external DACs. Controls the maximum transmit chip rate.

CLK_P: 125 MHz processing clock used for gigabit Ethernet interface, FEC encoder, and FEC decoder. There is no advantage in increasing this clock frequency beyond 125 MHz.

Typical maximum clock frequencies for various FPGA families are listed below:

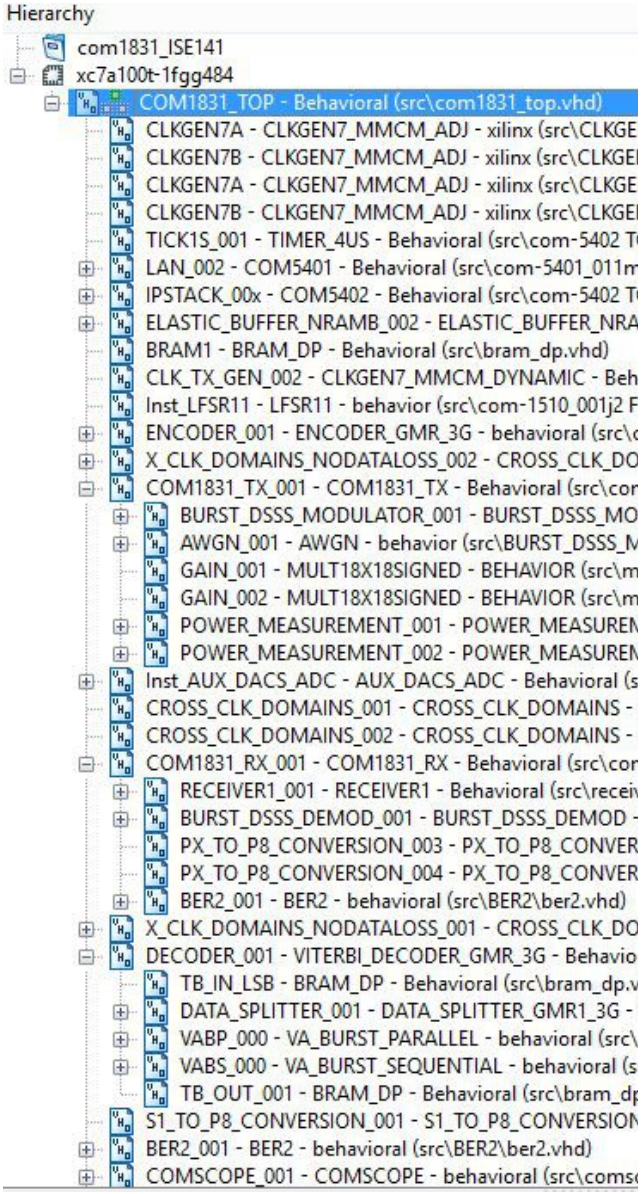
Device family	CLK_ADCg	CLK_TXg	CLK_P
Xilinx Kintex 7 -2	250 - 300 MHz	250 - 300 MHz	125 MHz
Xilinx Artix 7 Spartan-1	160 MHz	160 MHz	125 MHz

No Xilinx-specific code

The VHDL source code is written in generic VHDL. No Xilinx CORE is used. No Xilinx primitive need to be used. Dual-port RAM blocks are inferred.

VHDL components overview

Top level



The code is stored with one, and only one, entity per file as shown above.

COM1831_TOP.vhd is the top level. It includes several other ComBlock components such as the COM-1510SOFT burst FEC encoder and decoder, the COM-5402SOFT IP stack and the COM-5401SOFT tri-mode Ethernet MAC.

LFSR11.vhd: pseudo random binary sequence generator PRBS-11. Generates a PRBS11 test sequence at the modulator input. The PRBS11 sequence is recognized by the BER2 bit error rate tester at the receiving end to measure the link quality. Disabled during normal operation.

ENCODER_GMR_3G.vhd is the block convolutional encoder. It supports zero-tail insertion mechanism. The data source sends a complete frame, as delineated by the SOF_IN and EOF_IN flags. Once a complete input frame is received, the encoder will generate a complete encoded output frame. Thus, the encoding latency is one input frame duration.

CROSS_CLK_DOMAINS_NODATALOSS.vhd preserves the signal integrity while crossing clock domains (from the general processing clock domain CLK_P to the digital modulator clock domain CLK_TXg for example).

BURST_DSSS_MODULATOR.vhd implements the digital modulation and spectrum shaping. Key controls include chip rate, modulation symbol rate, output signal amplitude, spreading code.

AWGN.vhd implements the optional additive white Gaussian noise by generating complex (I,Q) independent Gaussian random samples once every CLK_TXg clock period. Instantiation is controlled by the generic flag **AWGN_EN**.

RECEIVER1.vhd is the front-end digital receiver which processes digital samples from the A/D converter(s). Its functions include fixed frequency translation to (near-zero) baseband, AGC, variable decimation (CIC) filters and one half-band filter for image rejection. Input digital samples can be complex (in the case of baseband input samples) or real (in the case of IF undersampling).

BURST_DSSS_DEMOD.vhd is the heart of the demodulator. It conducts parallel search of the spreading code during acquisition. Once the code is locked, an internal 2048-point FFT computes the frequency error. Once corrected for frequency error, the received signal is fed into carrier and symbol timing tracking loops for coherent demodulation. A matched filter detects the presence of the sync word marking the start of the fixed-length data field.

VITERBI_DECODER_GMR_3G.vhd is the block FEC decoder top component in this hierarchical design. It includes state machines to handle tail-biting and zero tail when applicable.

BER2.vhd synchronizes with the received bit stream and counts the number of bit error when a PRBS-11 sequence is being transmitted.

COM5401.vhd implements the 10/100/1000 Ethernet MAC functions. It is designed to interface with an external Gigabit Ethernet PHY integrated circuit via a standard RGMII or GMII interface. The default interface is RGMII. [2]

COM5402.vhd implements the higher-level IP protocols, namely ARP, PING, TCP server, UDP (unicast and multicast), IGMP. [3]

SIM2OUTFILE.vhd writes three 12-bit data variables to a tab delimited file which can be subsequently read by Matlab (load command) for plotting or analysis.

Test environment

tbcom1831.vhd in the /sim directory is a test bench consisting of a back-to-back PRBS-11 pseudo-random sequence generator, convolutional encoder, modulator, additive white Gaussian noise, demodulator, Viterbi decoder and bit error rate tester. No stimulus file is needed.

Reference documents

[1] COM-1831 Burst mode DSSS modem 80 Mchip/s, specifications for the ready-to-use hardware module.

[2] COM-5401SOFT Tri-mode 10/100/1000 Ethernet MAC, VHDL source code overview
www.comblock.com/download/com5401soft.pdf

[3] COM-5402SOFT
IP/TCP/UDP/ARP/PING STACK for GbE
VHDL source code overview
www.comblock.com/download/com5402soft.pdf

[4] COM-1510SOFT
Block-mode convolutional FEC codec
VHDL source code overview
www.comblock.com/download/com1510soft.pdf

[5] COM-1931 L/S-band burst-mode spread-spectrum transceiver
www.comblock.com/com1931.html

ComBlock Ordering Information

COM-1831SOFT BURST MODE SPREAD-SPECTRUM MODEM, VHDL SOURCE CODE / IP CORE

ECCN: 5E001.b.4

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