COM-1849 TCP STREAM TO 32/64 PARALLEL DIGITAL OUTPUTS

Key Features

- Converts a TCP stream received over Gigabit Ethernet to 32- or 64-bit digital output samples.
- Electrical format: differential LVDS (32-bit max) or single-ended LVTTL (64-bit max)
- External sampling clock or internally generated output sampling clock.
- User-defined output sample width: 1 through 8 Bytes.
- Maximum output sampling rate > (800 Mbits/s / number of output bits), e.g. 100 Msamples/s for 8-bit wide outputs
- Internal TCP server awaits for connection from the TCP client.
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.
- Connectorized 3”x 3.5” module for ease of prototyping. Single 5V supply with reverse voltage and overvoltage protection. Interfaces with 3.3V LVTTL logic.

MSS • 845 Quince Orchard Boulevard Ste N • Gaithersburg, Maryland 20878-1676 • U.S.A.
Telephone: (240) 631-1111 www.ComBlock.com

Configuration

An entire ComBlock assembly comprising several ComBlock modules can be monitored and controlled centrally over a single connection with a host computer. Connection types include built-in types:

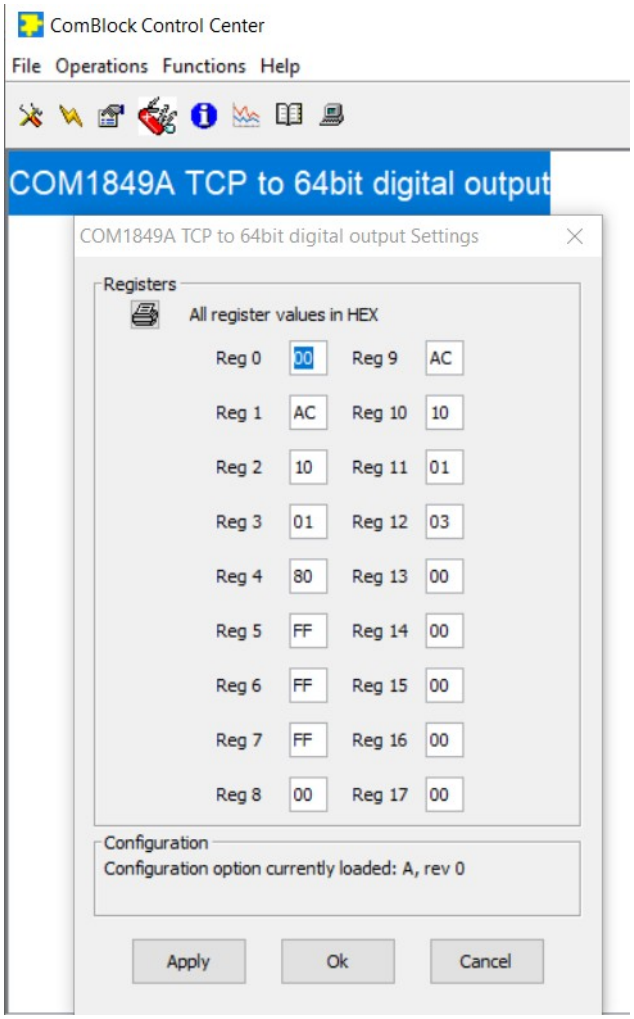
- USB, TCP-IP/LAN

or connections via adjacent ComBlocks

The module configuration is stored in non-volatile memory.

Configuration (Basic)

The easiest way to configure the COM-1849 is to use the **ComBlock Control Center** software (downloadable here). In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-1845 module to be configured, next click the *Settings* button to display the *Settings* window shown below.



Control Registers

The module configuration parameters are stored in volatile memory.

General	
Parameters	**Configuration**
Internal/External frequency reference	0 = internal TCXO as frequency reference. 1 = external. Use the 10 MHz clock externally supplied through the J7 SMA connector as frequency reference. REG0(0)
Byte to Word alignment method in TCP stream	0 = unframed Byte stream. The first Byte received after the TCP connection is the first Byte in the first output sample word. 1 = integer number of output sample words encapsulated within a HDLC frame REG0(1)
HDLC frame CRC check	0 = enabled 1 = bypassed Ignored when HDLC is disabled (unframed Byte stream) REG0(2)
Output sample word width (in Bytes)	Valid entries: 1,2,3,4,5,6,7,8 Bytes for LVTTL samples width 1,2,3,4 Bytes for LVDS samples width Important: the HDLC frame payload size must always be an integer multiple of output samples. REG0(7:4)
Output sampling clock selection	0 = external sampling clock 1 = internally generated output sampling clock. Frequency determined by the NCO control below. REG13(0)
Ouput sampling clock frequency	If clock is generated internally, its frequency $\mathbf{f_s}$ is determined by the 32-bit word computed as $\mathbf{f_s} * 2^{32}$ / 333.333 MHz REG17 (MSB) – REG14 (LSB)

Network Interface	
Parameters	**Configuration**
Static IP address	4-byte IPv4 address. Example : 0x AC 10 01 80 designates address 172.16.1.128 REG1 (MSB) - REG4 (LSB)
Subnet mask	REG5 (MSB) – REG8(LSB)
Gateway IP address	REG9 (MSB) – REG12(LSB)

Status Registers

Parameters	Monitoring
Hardware self-check	At power-up, the hardware platform performs a quick self check. The result is stored in status registers SREG0-9 Properly operating hardware will result in the following sequence being displayed: 01 F1 1D xx 1F 93 10 00 22 07.
LAN PHY ID	0x22 SREG8
LAN MAC address	SREG9 – SREG14
TCP connections	SREG15(0) M&C connected SREG15(1) Data stream connected
Sampling rate	Expressed in Hz SREG(16)(LSB) - SREG(19)(MSB)

Operation

Prerequisite

In order to perform the one-time initial configuration, one must first install the ComBlock USB driver. See
https://comblock.com/gettingstarted.html

Network configuration

The built-in TCP server must be assigned a static address consistent with the user's LAN. This operation is typically done once before connecting the COM-1849 to a different LAN. To that effect, connect the supplied USB cable between a PC and the COM-1849.

In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-1849 module to be configured, next click the *Settings* button to display the *Settings* window.

Enter the static IP address in control registers REG1-REG4, in hexadecimal using upper case characters. For example
AC 10 01 80 designates the address 172.16.1.128

Click on the Apply or OK button. Wait 10 seconds before turning power off.

Note: the static address must be consistent with existing LAN, namely:

- same first three address numbers as the PC
- unique fourth address number not already in use over the LAN

TCP

Before sending data over the LAN, the PC (TCP client) must first establish a TCP connection with the COM-1849 (TCP server) at IP port 1024.

Once the TCP connection is established, the PC can send the formatted data stream.

As the TCP protocol includes an end-to-end flow-control mechanism, the PC application should try to send data as fast as the TCP connection allows it.

When the application calls the send function to send a data buffer, the send function will return the actual number of Bytes sent.

Stream format

Output samples data sent over the TCP connection can be carried as an unformatted Byte stream, or encapsulated in a HDLC frame, based on the control register REG1(1) selection.

Byte-wise HDLC conveys the Byte to word alignment information. Each HDLC frame must contain an integer number of samples/words.

The HDLC rules are as follows:

- A HDLC frame is delineated with 0x7E flags at the start and end.
- The frame type is a two byte number appended immediately after the 0x7E opening flag. (meaning TBD)
- A two byte CRC is appended after the information field. CRC is calculated over frame type and information fields only, before byte stuffing.
  CRC-16 CCITT polynomial is used x^16 + x^12 + x^5 + 1
- Empty frames do not include any CRC or frame type, just two 0x7E markers.
- DATA and CRC fields are stuffed by the following rules
  7E hex => 7D 5E hex
  7D hex => 7D 5D hex
- Maximum HDLC frame size is 1024 Bytes

Digital Test Points

Test Point	Definition
J4/A15	TCP stream1 connection
J4/A16	TCP stream1 received data valid
J4/A17	TCP stream1 flow control
J4/A18	HDLC decoder output data valid
J4/A19	HDLC decoder output flow control
J4/A20	Toggle when bad received HDLC frame
J4/A21	Output word valid (CLK_P clock domain)
J4/A22	Output word valid (CLK_S clock domain), should be always '1' unless there is an underflow condition (not enough data sent over TCP connection)
J4/A23	

Options

Several interface types are supported through multiple firmware options. All firmware versions can also be downloaded from http://www.comblock.com/download.html

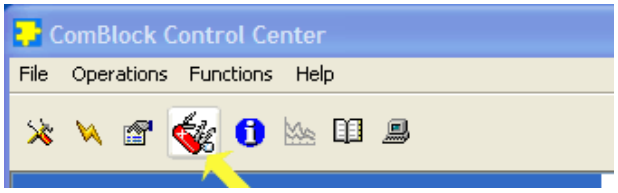
Changing the firmware option requires loading the firmware once using the ComBlock control center, then switching between the stored firmware versions The selected firmware option is automatically reloaded at power up or upon software command within 18 seconds

Option	Definition
-A	Differential LVDS output
-B	Single-ended LVTTL output

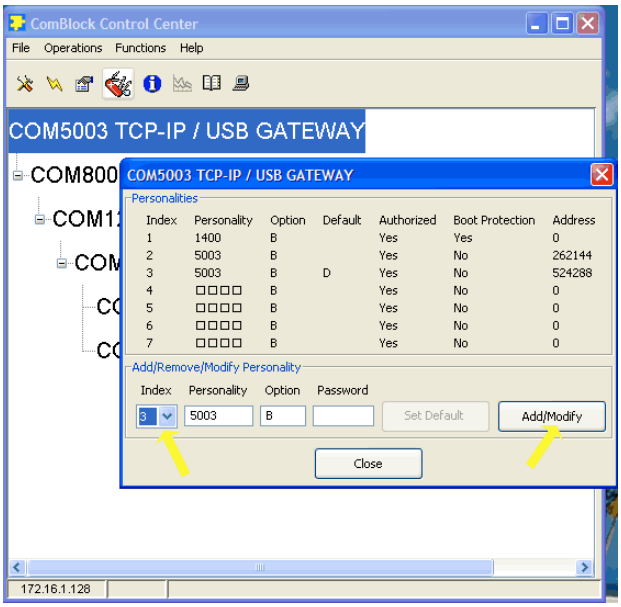
Load Software Updates

From time to time, ComBlock software updates are released.

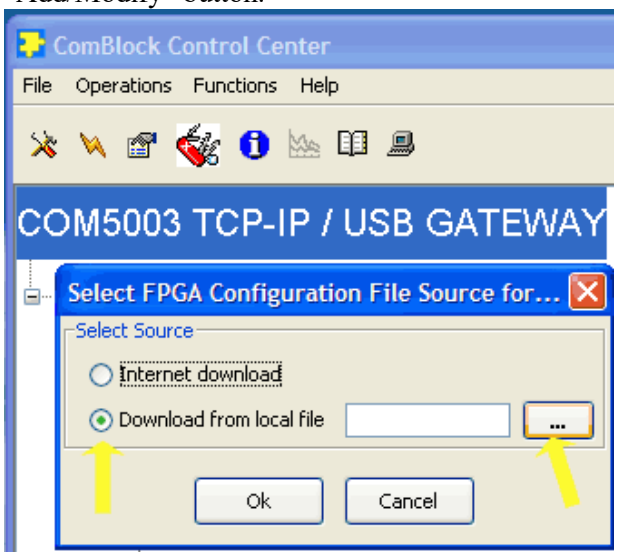
To manually update the software, highlight the ComBlock and click on the Swiss army knife button.



The receiver can store multiple personalities. The list of personalities stored within the ComBlock Flash memory will be shown upon clicking on the Swiss army knife button.



The default personality loaded at power up or after a reboot is identified by a ‘D’ in the Default column. Any unprotected personality can be updated while the Default personality is running. Select the personality index and click on the “Add/Modify” button.



The software configuration files are named with the .bit extension. The bit file can be downloaded via the Internet, from the ComBlock CD or any other local file.

The option and revision for the software currently running within the FPGA are listed at the bottom of the advanced settings window.

Recovery

This module is protected against corruption by an invalid FPGA configuration file (during firmware

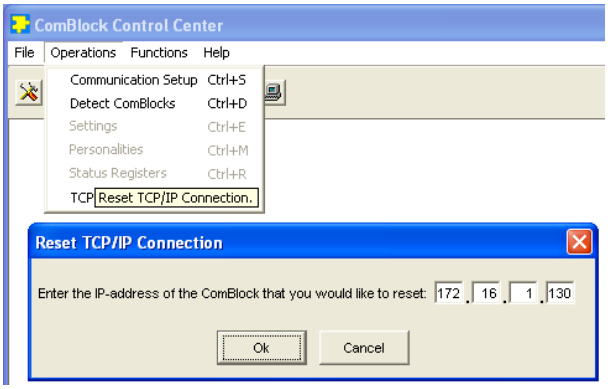
upgrade for example) or an invalid user configuration. To recover from such occurrence, connect a jumper in J3 and during power-up. This prevents the FPGA configuration and restore USB communication [LAN communication is restored only if the IP address is known/defined for the personality index selected as default]. Once this is done, the user can safely re-load a valid FPGA configuration file into flash memory using the ComBlock Control Center.

UDP Reset

Port 1029 is open as a UDP receive-only port. This port serves a single purpose: being able to reset the modem (and therefore the TCP-IP connection) gracefully. This feature is intended to remedy a common practical problem: it is a common occurrence for one side of a TCP-IP connection to end abnormally without the other side knowing that the connection is broken (for example when a client 'crashes'). In this case, new connections cannot be established without first closing the previous ones. The problem is particularly acute when the COM-1849 is at a remote location.

The command "@001RST<CR><LF>" sent as a UDP packet to this port will reset all TCP-IP connections within the COM-1849.

TCP-IP connections can also be cleared remotely from the ComBlock Control Center as illustrated below:



VHDL code

The FPGA code is written in VHDL. It does not use any IP core or third-party software.
It occupies the following FPGA resources:

Resource	Utilization	Available	Utilization...
LUT	7014	63400	11.06
LUTRAM	3	19000	0.02
FF	5972	126800	4.71
BRAM	10	135	7.41
IO	98	285	34.39
BUFG	9	32	28.13
MMCM	2	6	33.33
PLL	1	6	16.67

Operating input voltage range

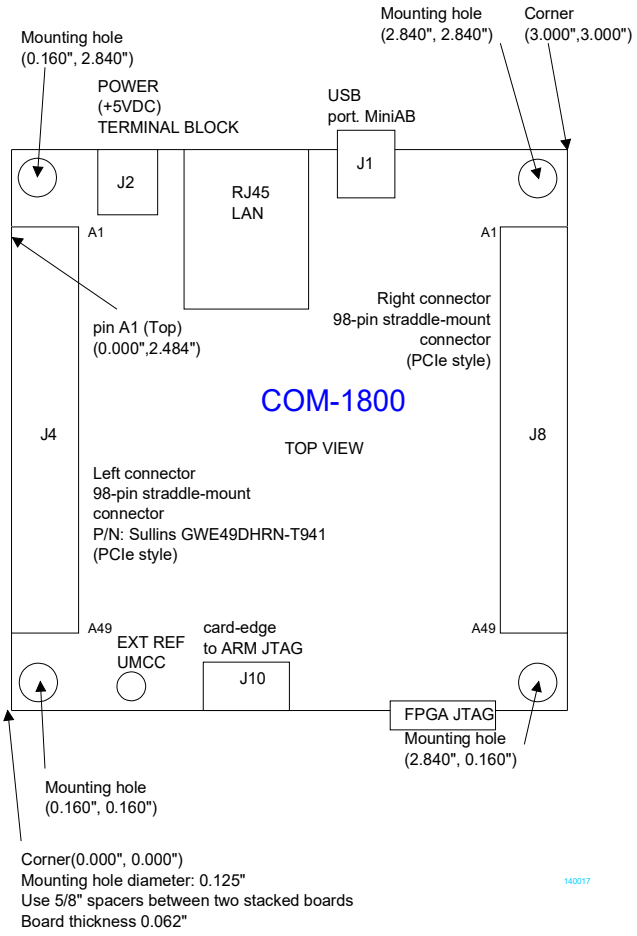
Supply voltage	+4.5V min, +12V max 650mA typ.

Absolute Maximum Ratings

Supply voltage	-0.5V min, +20V max
98-pin connector inputs	-0.5V min, +3.6V max

Important:
The I/O signals connected directly to the FPGA are NOT 5V tolerant!

Mechanical Interface



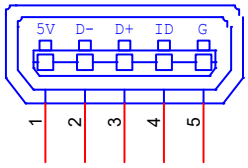
Schematics

The board schematics are available on-line at
http://comblock.com/download/com_1800schematics.pdf

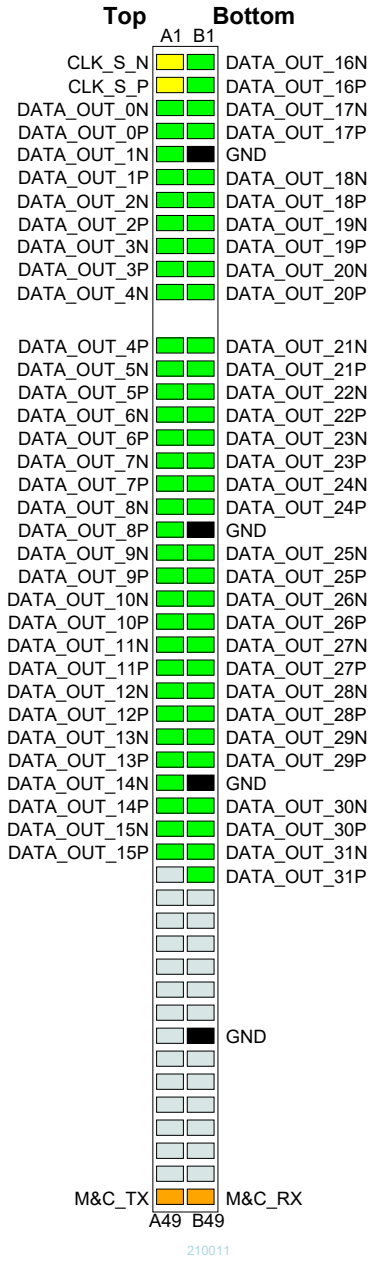
Pinout

USB

The USB port is equipped with mini type AB connectors. (G = GND). The COM-1849 acts as a USB device.

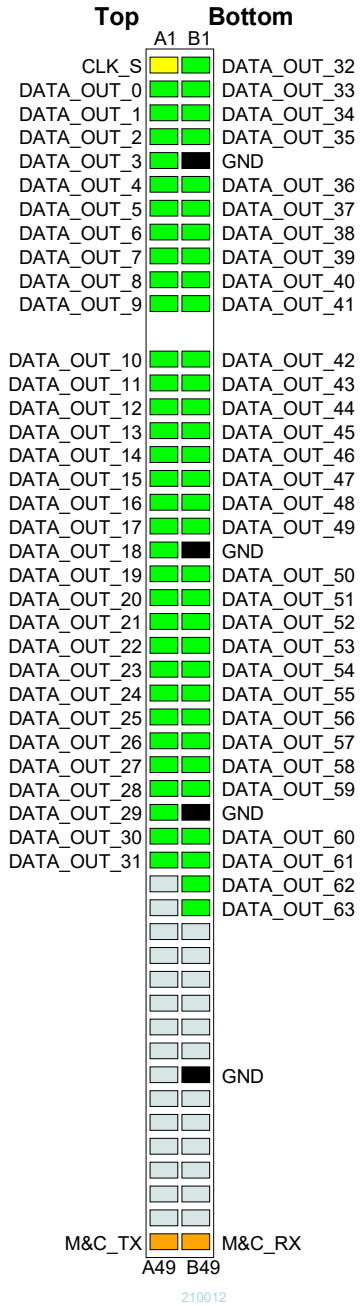


Right Connector J8



LVDS output samples (**-A** firmware option)

Right Connector J8



LVTTL output samples (**-B** firmware option)

Configuration Management

This specification is to be used in conjunction with VHDL software revision 1 and ComBlock control center revision 3.13g and above.

It is possible to read back the option and version of the FPGA configuration currently active. Using the ComBlock Control Center, highlight the COM-1849 module, then go to the advanced settings. The option and version are listed at the bottom of the configuration panel.

For the latest data sheet, please refer to the **ComBlock** web site: http://www.comblock.com/download/com1849.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to http://www.comblock.com/product_list.html .

ComBlock Ordering Information

COM-1849 TCP stream to 32/64 parallel digital outputs converter

ECCN: EAR99

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