COM-1902 L/S-band burst PSK transceiver

Key Features

- L/S-band modem to send and receive short UDP frames over wireless, satellite or cable.
- BPSK/QPSK modulation with coherent demodulation. Convolutional or turbo code error correction.
- Nominal frequency of operation: 950 – 2175 MHz for direct connection to external LNB or BUC. Customization to other frequency bands is possible.
- Burst mode operation:
  - Programmable fixed-length data frames from/to LAN/UDP ports
  - Multiple frames transmitted efficiently with only 44-symbol separation.
- Acquisition: 94-symbol preamble with no apriori knowledge of arrival time
- Large frequency acquisition range: +/- 20% of symbol rate with no apriori knowledge.
- Programmable symbol rate up to 39.5 MSymbols/s
- Supply voltage: 18[1] – 36VDC with reverse voltage and surge protection.
- Frequency reference: internal TCXO or input for an external, higher-stability 10 MHz frequency reference.
- Built-in tools: PRBS-11 pseudo-random test sequence, BER tester, AWGN generator, internal loopback mode.
- Monitoring:
  - Carrier frequency error
  - SNR
  - BER
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.

For the latest data sheet, please refer to the **ComBlock** web site: http://www.comblock.com/download/com1902.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to http://www.comblock.com/product_list.html .

[1] 5.6V min when not supplying external LNB power

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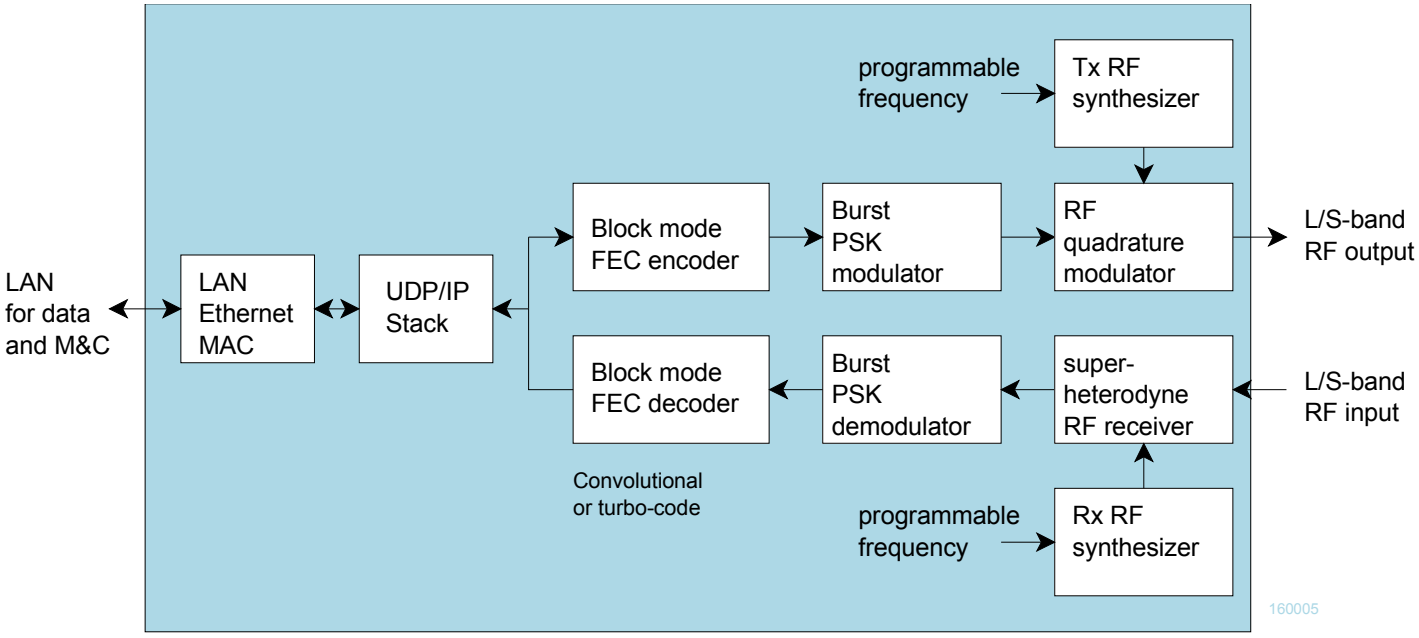
 Issued 1/13/2020

Functional Block Diagram

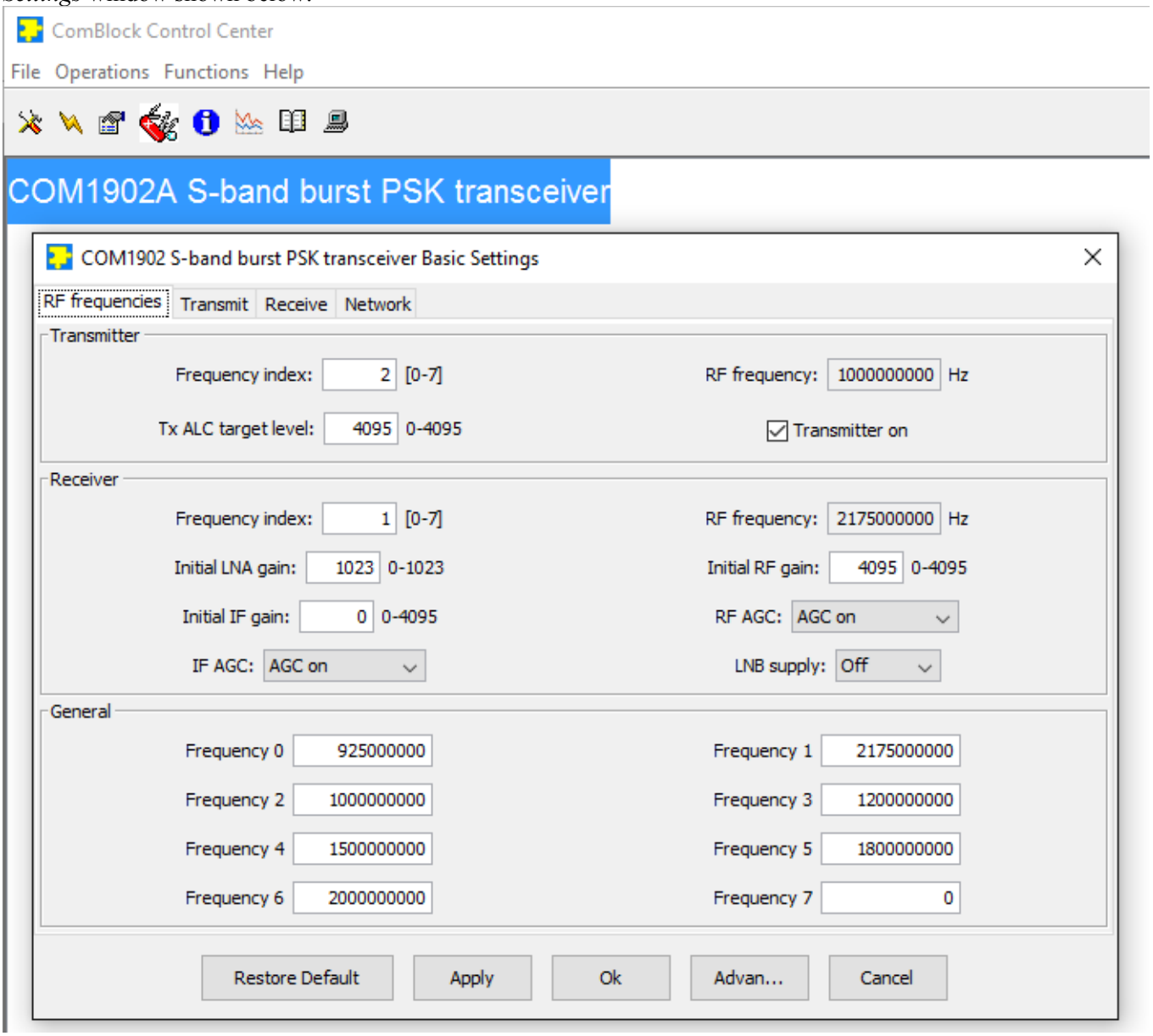


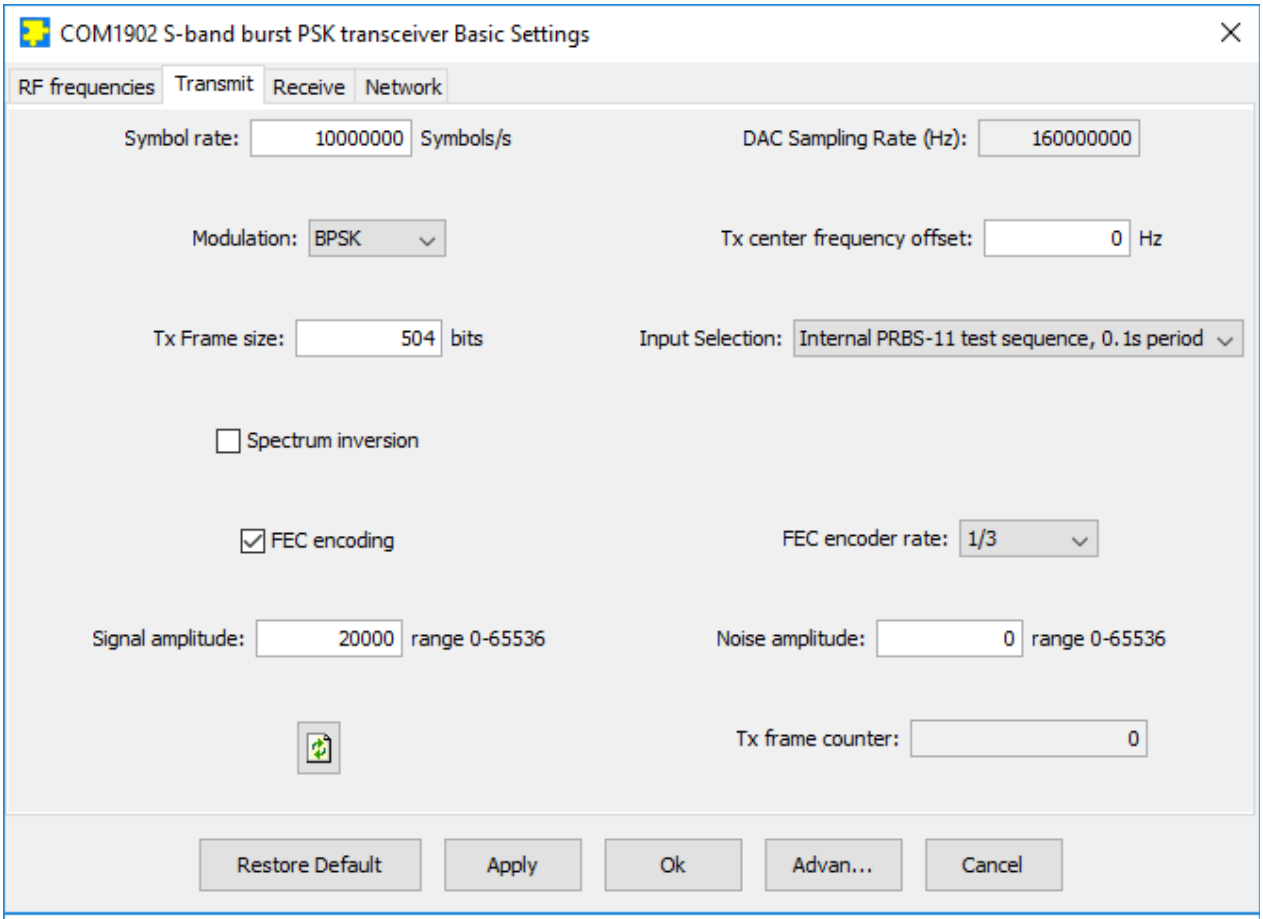
Configuration (Basic)

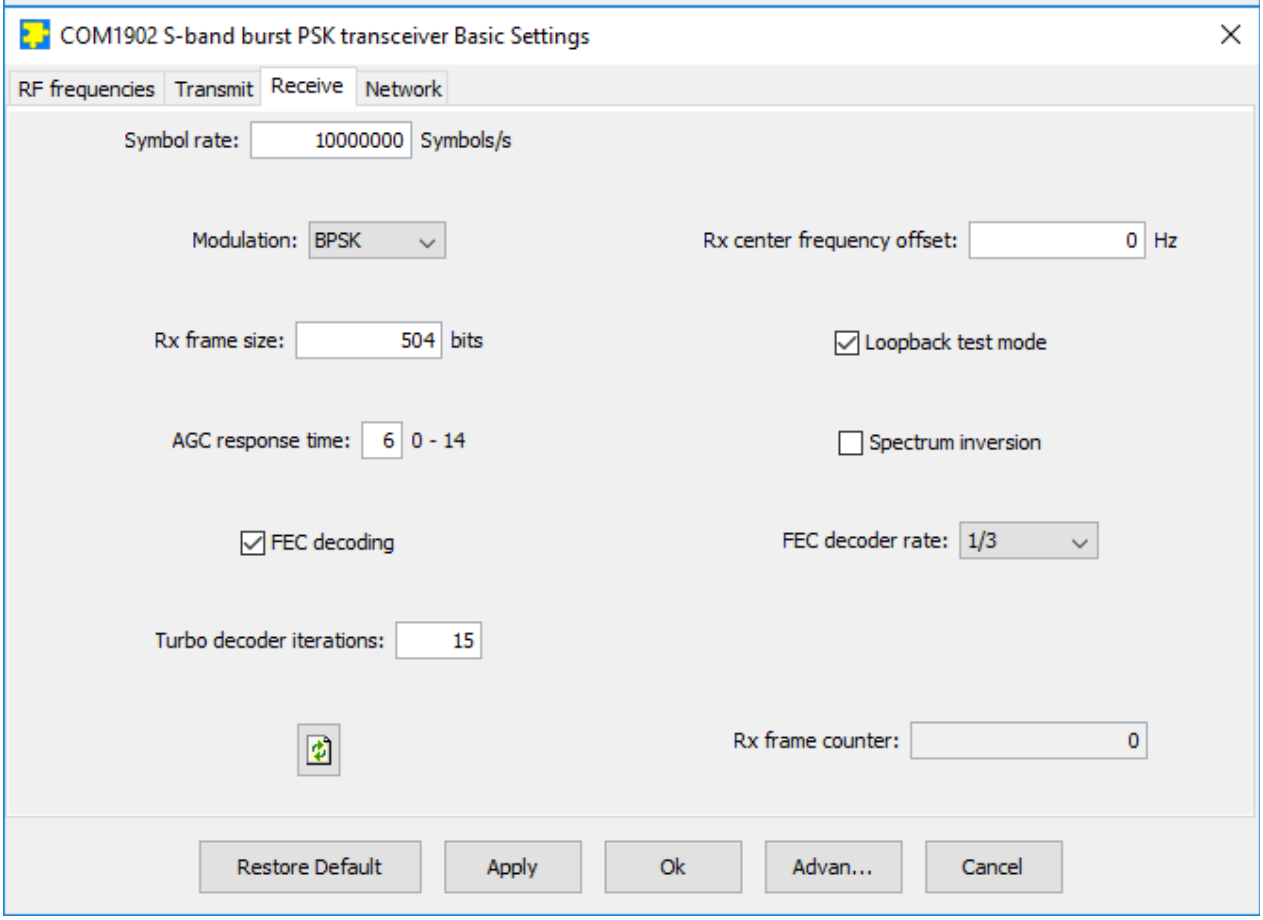
The easiest way to configure the COM-1902 is to use the **ComBlock Control Center** software supplied with the module on CD. Please follow the few simple steps described in the user manual "ccchelp.pdf" document to install the ComBlock Control Center software "ComBlock_Control_Center_windows_rev.exe"

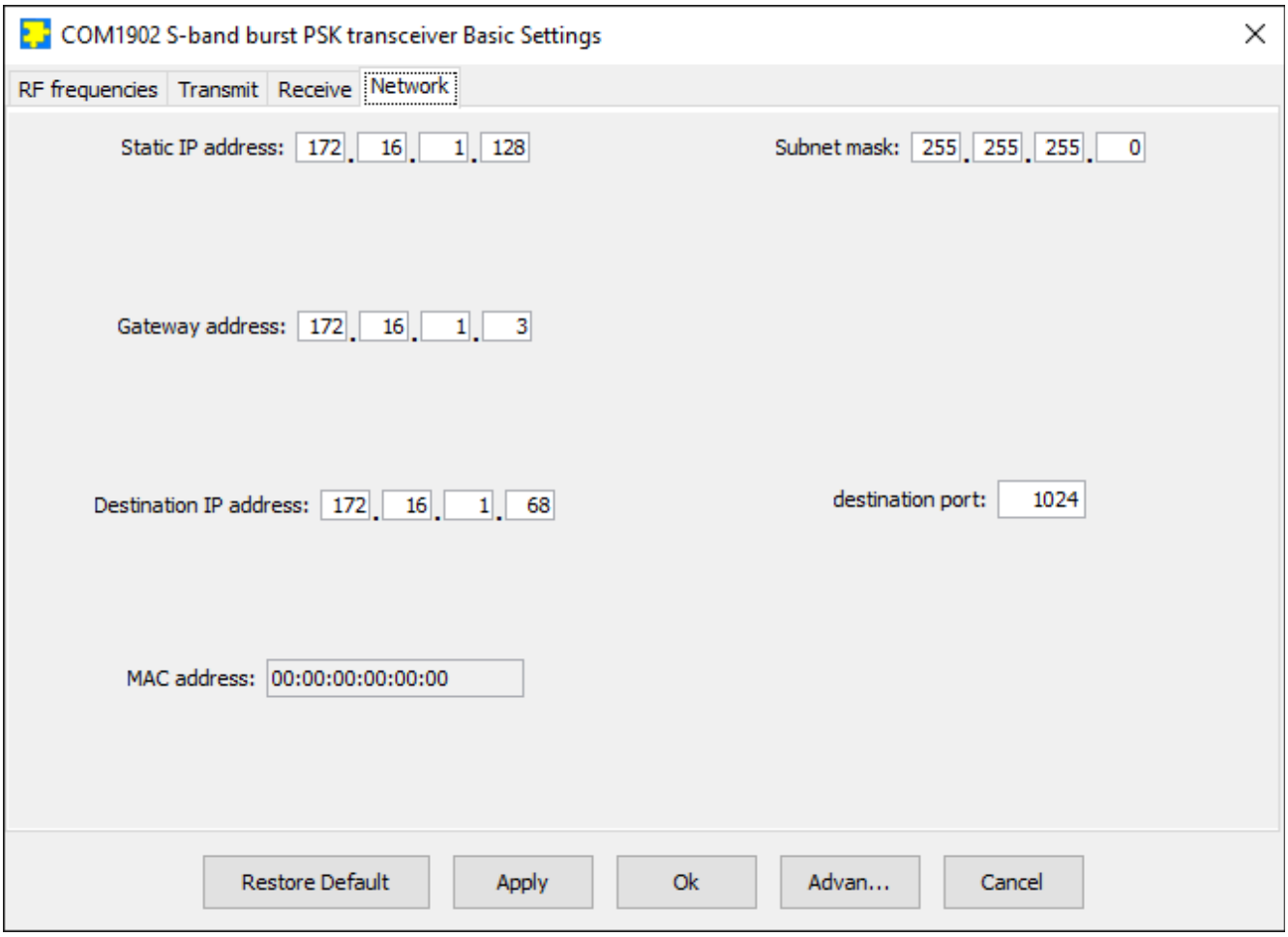
Connect the LAN cable between PC and transceiver RJ45 connector labeled "M&C LAN". Turn the transceiver power supply on and wait approximately 5-10 seconds. In the **ComBlock Control Center** window, click on the left-most button and select LAN as primary communication media. The default IP address is 172.16.1.128.

In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-1902 module to be configured, next click the *Settings* button to display the *Settings* window shown below.




COM1902 S-band burst PSK transceiver Basic Settings
RF frequencies
Transmit
Receive
Network
Symbol rate:
10000000
Symbols/s
DAC Sampling Rate (Hz):
160000000
Modulation:
BPSK
Tx center frequency offset:
0
Hz
Tx Frame size:
504
bits
Input Selection:
Internal PRBS-11 test sequence, 0.1s period
Spectrum inversion
FEC encoding
FEC encoder rate:
1/3
Signal amplitude:
20000
range 0-65536
Noise amplitude:
0
range 0-65536
Tx frame counter:
0
Restore Default
Apply
Ok
Advan...
Cancel


COM1902 S-band burst PSK transceiver Basic Settings
RF frequencies
Transmit
Receive
Network
Symbol rate:
10000000
Symbols/s
Modulation:
BPSK
Rx center frequency offset:
0
Hz
Rx frame size:
504
bits
Loopback test mode
AGC response time:
6
0 - 14
Spectrum inversion
FEC decoding
FEC decoder rate:
1/3
Turbo decoder iterations:
15
Rx frame counter:
0
Restore Default
Apply
Ok
Advan...
Cancel



Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center "Advanced" configuration or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write. Definitions for the Control registers and Status registers are provided below.

Control Registers

The module configuration parameters are stored in volatile (SRT command) or non-volatile memory (SRG command). The stored configuration is automatically loaded up at power up. All control registers are read/write.

Note: several multi-byte fields like the IP addresses are enacted upon (re-)writing to the last control register (REG141)

Several key parameters are computed on the basis of the 160 MHz ADC clock f_{clk_adc} or the 125 MHz internal processing clock f_{clk_p}.

RF	Configuration
Stored frequency f_0	Preselected transmitter or receiver frequency f_0. (one of eight stored frequencies) Valid range 925 MHz – 2.175 GHz, expressed in Hz. REG0: bit 7:0 (LSB) REG1: bit 15:8 REG2: bit 23:16 REG3: bit 31:24 (MSB)
Receiver frequency selection	Use to switch the receiver center frequency among preselected values. Range 0 through 7 REG6(2:0)
Transmitter frequency selection	Use to switch the transmitter center frequency among preselected values. Range 0 through 7 The rx/tx frequencies change is enacted upon writing to REG6. REG6(6:4)
Stored frequency f_x	Seven additional preselected frequencies x = 1 through 7 Same format as f_0. REG(3+4*x): bits 7:0 (LSB) REG(4+4*x): bits 15:8 REG(5+4*x): bits 23:16 REG(6+4*x): bits 31:24 (MSB)
Receiver RF Gain	Initial RF gain (before the RF AGC takes over). 12-bit. 0 for the minimum gain, 4095 for the maximum gain. The receiver RF gain change is enacted upon writing to REG5. REG4: bits 7:0 (LSB) REG5(3:0): bits 11:8
Receiver IF Gain	Initial IF gain (before the IF AGC takes over). 12-bit. 0 for the minimum gain, 4095 for the maximum gain. The receiver IF gain change is enacted upon writing to REG36. REG35: bits 7:0 (LSB) REG36(3:0): bits 11:8
Receiver LNA Gain	LNA gain 10-bit. 0 for the minimum gain, 1023 for the maximum gain. The receiver IF gain change is enacted upon writing to REG41. REG40: bits 7:0 (LSB) REG41(3:0): bits 11:8

Transmitter ALC target	The transmit gain is automatically adjusted so that the measured tx power equals this field. The transmitter gain change is enacted upon writing to REG38. REG37: bits 7:0 (LSB) REG38(3:0): bits 11:8
Receiver LNA AGC loop	0 = open loop. LNA path gain is fixed by control registers. 1 = AGC on. Gain is adjusted on the basis of the RSSI measurement. REG39(0)
Receiver RF AGC loop	0 = open loop. RF path gain is fixed by control registers. 1 = AGC on. Out-of-range conditions are detected at the RF mixer and IF power detector. REG39(1)
Receiver IFAGC loop	0 = open loop. IF1 path gain is fixed by control registers. 1 = AGC on. Out-of-range conditions are detected at the IF power detector. REG39(3:2)
Transmitter ON	0 = off 1 = on REG39(6)
LNB supply	The transceiver is capable of supplying up to 500mA at 13VDC or 18VDC to an external LNB. This supply voltage is multiplexed with the RF input signal onto the "RF Rx" input. 0 = LNB supply off 1 = LNB supply on **Warning: Enabling the LNB supply may cause damage to test equipment unless a DC block is used.** REG43(0)
LNB supply 13V vs 18V	0 = 13VDC LNB supply 1 = 18VDC LNB supply REG43(1)
General Parameters	**Configuration**
Internal/External frequency reference	REG46(0): frequency reference is external 10 MHz (1) or internal 19.2 MHz TCXO (0) REG46(1): enable(1)/disable(0) CLKREF_OUT (special connector on front-panel) REG46(2): enable(1)/disable(0) CLK_LNB (multiplexed with received signal) REG46(3): enable(1)/disable(0) CLK_TX (multiplexed modulated transmit signal + 10 MHz)
FEC encoding	Option **–A** K=9 rate ½ convolutional code with zero tail bits. Option **–B** Turbo code 0 = bypassed 1 = FEC encoding enabled REG47(0)
FEC decoding	Option **–A** K=9 rate ½ convolutional code with zero tail bits. Option **–B** Turbo code 0 = bypassed 1 = FEC decoding enabled REG47(1)
reserved	"00000" REG47(7:3)
Turbo code encoder rate	0 = rate 1/3 1 = rate 1/2 2 = rate 2/3 3 = rate 3/4

	4 = rate 4/5 5 = rate 5/6 6 = rate 6/7 7 = rate 7/8 REG94(3:0)
Turbo code decoder rate	0 = rate 1/3 1 = rate 1/2 2 = rate 2/3 3 = rate 3/4 4 = rate 4/5 5 = rate 5/6 6 = rate 6/7 7 = rate 7/8 REG95(3:0)
Turbo code decoder maximum number of iterations	1 – 15. Typical settings is 7. Must be an odd number REG96

Modulator	**Configuration**
Processing clock f_{clk_tx}	Modulator processing clock. Also serves as DAC sampling clock. Expressed as as f_{clk_tx} = 160 MHz * M / (D * O)) where D is an integer divider in the range 1 - 106 M is a multiplier in the range 2.0 to 64.0 by steps of 1.0. Fixed point format 7.3 O is a divider in the range 2.0 to 128.0 by steps of 1.0. Fixed point format 7.3 Note: the graphical use interface computes the best values for M, D and O. f_{clk_tx} recommended range 80-160 MHz. REG48(6:0) = D REG49 = M(7:0) REG50(1:0) = M(9:8) REG51 = O(7:0) REG52(2:0) = O(10:8)
Modulation symbol rate $f_{symbol\_rate\_tx}$	The modulator symbol rate is in the form $f_{symbol\_rate\_tx} = f_{clk\_tx} / 2^n$ where n ranges from 2 (4 samples per symbol) to 15 (symbol rate = f_{clk_tx} / 32768). n is defined in REG53(3:0)
Output center frequency (f_c)	The modulated signal center frequency can be shifted in frequency 32-bit signed integer (2's complement representation) expressed as $f_c * 2^{32} / f_{clk\_tx}$ REG57 (LSB) – REG54 (MSB)
Sinusoidal frequency offset	In addition to the fixed frequency offset above, a sinusoidal frequency offset can be generated to mimic Doppler rate in highly mobile applications. This offset is characterized by two parameters: amplitude and period. The amplitude (a frequency) is expressed as $f_{c\_amplitude} * 2^{32} / f_{clk\_tx}$ in the following control registers:

	REG58(LSB) – REG61 (MSB) The period is expressed as 2^{32} /(f_{clk_tx} *T) in the following control registers: REG62(LSB) – REG65 (MSB)
Digital Signal gain	16-bit amplitude scaling factor for the modulated signal. The maximum level should be adjusted to prevent saturation. The settings may vary slightly with the selected symbol rate. Please check for saturation (see test points) when changing either the symbol rate or the signal gain. REG66 = LSB REG67 = MSB
Additive White Gaussian Noise gain	16-bit amplitude scaling factor for additive white Gaussian noise. Because of the potential for saturation, please check for saturation (see test points) when changing this parameter. REG68 = LSB REG69 = MSB
Modulation type	0 = BPSK 1 = QPSK 2 = OQPSK REG70(5:0)
Spectrum inversion	Set to '1' when a spectrum inversion occurs in subsequent frequency upconverters. '0' otherwise. 0 = off 1 = on REG70(6)
Reserved	REG70(7) = '0'
Input selection	0 = from UDP port 1024 (burst-mode operation) 1 = internal pseudo-random test sequence. 100ms burst repetition 2 = internal pseudo-random test sequence continuous transmission 3 = unmodulated test mode (carrier only) NEW 4 = internal pseudo-random test sequence. 1s burst repetition 5 = internal pseudo-random test sequence. 3s burst repetition 6 = internal pseudo-random test sequence. 10s burst repetition 7 = from TCP server at port 1026 (continuous-mode operation) NEW REG71(2:0)
TX_ENB control	The TX_ENB signal at the interface controls the RF transmit circuit. During normal operations, the transmitter and ancillary circuits (RF LO) are muted outside of a transmit burst. REG71(5) = 0 However, during tests, the transmitter can be forced to stay ON at all times, for example when the AWGN is generated within. REG71(5) = 1
Transmit payload size	TX_PAYLOAD_SIZE Encoded frame size in modulation symbols, as seen by the PSK modulator. Must be consistent with the FEC code and modulation selections.

	This includes payload data and tail bits (Convolutional FEC) or CRC16 (turbo code FEC) but does not include preamble, sync word, or dummy bits. Must equal (ENC_FRAME_IN_SIZE/R + 16) when BPSK and convolutional FEC rate R encoding, or (ENC_FRAME_IN_SIZE/R + 16)/2 when QPSK and convolutional FEC rate R encoding, or (ENC_FRAME_IN_SIZE + 16)/R when BPSK and turbo code FEC rate R encoding, or (ENC_FRAME_IN_SIZE + 16)/2R when QPSK and turbo code FEC rate R encoding Constraint #1: Minimum burst size (including preamble, sync word) for best signal presence detection at the first frame: (58.6 us + 256/nominal symbol rate) REG72 = LSB REG73(4:0) MSB
Encoder input frame size	ENC_FRAME_IN_SIZE Frame size in bits before FEC encoding. Must be consistent with the modulator payload field size (see above). Constraint #2: when using convolutional code, the frame size is limited to 2048 bits. When using turbo code, the preferred frame sizes are 12,61 and 248 Bytes (96,488,1984 bits). Constraint #3: when using turbo code, the frame size is limited to 253 Bytes (2024 bits) Constraint #4: when using turbo code rates 2/3,3/4,5/6,6/7, ENC_FRAME_IN_SIZE must be in the form rate 2/3 case: (ENC_FRAME_IN_SIZE+16)/2 is multiple of 2 rate 3/4 case: (ENC_FRAME_IN_SIZE+16)/2 is multiple of 6 rate 4/5 case: (ENC_FRAME_IN_SIZE+16)/2 is multiple of 4 rate 5/6 case: (ENC_FRAME_IN_SIZE+16)/2 is multiple of 20 rate 6/7 case: (ENC_FRAME_IN_SIZE+16)/2 is multiple of 12 rate 7/8 case: (ENC_FRAME_IN_SIZE+16)/2 is multiple of 28 REG74 = LSB REG75(5:0) MSB

Demodulator	
Parameters	**Configuration**
Tx-Rx loopback	REG89(7): enable (1) or disable(0) loopback test mode
Receive window	**To enable the demodulator at all times (i.e. no restriction on the time of arrival of incoming bursts), set REG44(7) = '1'** When REG44(7) = '0', the demodulator is only enabled when the modulator is transmitting. The source code can be easily modified to limit the receive window to user-controlled time slots, for example in the case of a multi-node TDMA network.

Nominal symbol rate $f_{symbol\_rate\_rx}$	32-bit integer expressed as $f_{symbol\_rate\_rx} * 2^{32} / f_{clk\_adc}$. The maximum practical symbol rate is f_{clk_adc} /4. The maximum allowed error between transmitted and received symbol rate is +/- 100ppm. REG80 (LSB) – REG83 (MSB)
Nominal input center frequency (f_c)	The nominal center frequency is a fixed frequency offset applied to the input samples. It is used for fine frequency corrections, for example to correct clock drifts. 32-bit signed integer (2's complement representation) expressed as $f_c * 2^{32} / f_{clk\_adc}$ In addition to this fixed value, an optional time-dependent frequency profile can be entered (future). REG84 (LSB) – REG87 (MSB)
Modulation type	0 = BPSK 1 = QPSK 2 = OQPSK REG88(5:0)
Spectrum inversion	Nominally '1' as a spectrum inversion occurs on the COM-1902 receive path. 0 = off 1 = on REG88(6)
Receiver payload size	RX_PAYLOAD_SIZE Encoded frame size in modulation symbols, as seen by the PSK demodulator. This includes payload data and tail bits (Convolutional FEC) or CRC16 (turbo code FEC) but does not include preamble, sync word, or dummy bits. Must equal (DEC_FRAME_IN_SIZE/R + 16) when BPSK and convolutional FEC rate R encoding, or (DEC_FRAME_IN_SIZE/R + 16)/2 when QPSK and convolutional FEC rate R encoding, or (DEC_FRAME_IN_SIZE + 16)/R when BPSK and turbo code FEC rate R encoding, or (DEC_FRAME_IN_SIZE + 16)/2R when QPSK and turbo code FEC rate R encoding Constraint #1: Minimum burst size (including preamble, sync word) for best signal presence detection at the first frame: (58.6 us + 256/nominal symbol rate) REG90 = LSB REG91(4:0) MSB
Decoder output frame size	DEC_FRAME_OUT_SIZE Frame size in bits after decoding. Must be consistent with the modulator payload field size (see above). Constraint #2: when using convolutional code, the frame size is limited to 2048 bits. When using turbo code, the preferred frame sizes are 12,61 and 248 Bytes (96,488,1984 bits). Constraint #3: when using turbo code, the frame size is limited to 253 Bytes (2024 bits) Constraint #4: when using turbo code rates 2/3,3/4,5/6,6/7, ENC_FRAME_IN_SIZE must be in the form rate 2/3 case: (DEC_FRAME_OUT_SIZE +16)/2 is multiple of 2

	rate 3/4 case: (DEC_FRAME_OUT_SIZE +16)/2 is multiple of 6 rate 4/5 case: (DEC_FRAME_OUT_SIZE +16)/2 is multiple of 4 rate 5/6 case: (DEC_FRAME_OUT_SIZE +16)/2 is multiple of 20 rate 6/7 case: (DEC_FRAME_OUT_SIZE +16)/2 is multiple of 12 rate 7/8 case: (DEC_FRAME_OUT_SIZE +16)/2 is multiple of 28 REG92 = LSB REG93(5:0) MSB

Network Interface	
Parameters	**Configuration**
LAN MAC address LSB	REG123. To ensure uniqueness of MAC address. The MAC address most significant bytes are tied to the FPGA DNA ID. However, since Xilinx cannot guarantee the DNA ID uniqueness, this register can be set at the time of manufacturing to ensure uniqueness.
Static IP address	4-byte IPv4 address. Example : 0x AC 10 01 80 designates address 172.16.1.128 (default IP address) REG132 (MSB) – REG135(LSB)
Subnet mask	REG128 (MSB) – REG131(LSB)
Gateway IP address	REG124 (MSB) – REG127(LSB)
Destination IP address	4-byte IPv4 address Destination IP address for UDP frames with decoded data. REG136 (MSB) – REG139(LSB)
Destination ports	I-channel data is routed to this user-defined port number: REG140(LSB) – REG141(MSB)

Note: several multi-byte fields like the IP addresses are enacted upon (re-)writing to the last control register (REG141)

Monitoring

Status Registers

Parameters	**Monitoring**
Hardware self-check	At power-up, the hardware platform performs a quick self check. The result is stored in status registers SREG0-4, SREG16-18 Properly operating hardware will result in the following sequence being displayed: SREG0-SREG4 = 01 F1 1D xx 7F, where xx (bad NAND flash sectors) must be less than 10 SREG16-18 = 0x22 00 87
Power supply check	SREG4(0): PGOOD1 RF1_+3.1V SREG4(1): PGOOD2 IF1+_3.1V SREG4(2): PGOOD3 A_+4.75V SREG4(3): PGOOD4 MOD_+4.8V SREG4(4): PGOOD5 TX_SYNTH_+3.3V SREG4(5): PGOOD6 RX_+4.75V SREG4(6): PGOOD7 RX_SYNTH_+3.3V Overall valid response: 0x7F
RSSI	Received signal strength indicator. 12-bit number Practical range –70 to -5 dBm after LNA See RF_POWER_DET1 in schematic. SREG5 = LSB SREG6(3:0) = MSB
Received power at RF mixer	Power detection at RF mixer. Target is 0xEC0 while the RF AGC is tracking See RF_POWER_DET2 in schematic. SREG7 = LSB

	SREG8(3:0) = MSB
Received power at IF	Power detection at IF after bandpass filter and IF gain control. Target is 0xE80 while the IF AGC is tracking. See IF1_POWER_DET in schematic. SREG9 = LSB SREG10(3:0) = MSB
Transmit power	Power detection at the RF transmit output. See TX_POWER_DET in schematic. SREG11 = LSB SREG12(3:0) = MSB
RF synthesizers locked	'1' when locked SREG19(0): rx synthesizer locked SREG19(1): tx synthesizer locked
FPGA PLLs locked	'1' when locked SREG19(2): reference clock presence (either 10 MHz external or 19.2 MHz internal TCXO) SREG19(3): 160 MHz ADC sampling clock locked SREG19(4): 125 MHz LAN clock locked SREG19(5): DAC sampling clock locked
FEC codec type	0 = convolutional K=9 rate ½ 1 = turbo code Depends on the firmware currently active SREG19(6)
VCTCXO frequency drift w.r.t. external 10 MHz frequency reference NEW	Signed frequency error of internal VCTCXO frequency reference w.r.t. an external 10 MHz frequency reference connected to the 10 MHz IN SMA connector. This measurement is in 10ppb units. It helps the user compute the necessary compensation for the RF transmit and RF receive center frequency due to the VCTCXO drift. SREG63(LSB)-SREG66(MSB)

Modem monitoring	
FEC decoder input BER measurement	Option **–A** K=9 rate ½ convolutional code with zero tail bits. The burst-mode FEC decoder computes the input BER prior to decoding. Mesasured in a frame. This method works with any bit sequence. SREG20 (LSB) - SREG22 (MSB)
Decoded frame error counter (FER)	Option **–B** Turbo code SREG20 (LSB) - SREG22 (MSB)
BER tester synchronized	Option **–A** K=9 rate ½ convolutional code with zero tail bits. The built-in BER tester counts the number of errors after error correction. Option **–B** Turbo code case: the BER tester is meaningless as the turbo code decoder will block erroneous frames that do not pass the CRC check. SREG23(0): 1 when the BERT is synchronized with the received PRBS-11 test sequence.
Bit error rate	Monitors the BER (number of bit errors over 80,000 received bits) when the modulator is sending a PRBS-11 test sequence. Valid only when the BER tester is synchronized. SREG24 (LSB) – 27 (MSB)
Number of transmitted frames	SREG28 (LSB) – 30 (MSB)
Number of received frames	SREG31 (LSB) – 33 (MSB)
Preamble + sync field length	Length in symbols for the current active FPGA configuration SREG34 (LSB) – SREG35 (MSB)
Measured modulated signal power	SREG37(LSB) SREG38 SREG39(MSB)
Measured AWGN	Approximation: noise power is uniform over a range of +/- f_{clk_tx} /2

power	Therefore, the noise density depends on the selected modulator chip rate (see $\mathbf{f}_{clk\_tx}$ equation above) SREG40(LSB) SREG41 SREG42(MSB)
Carrier frequency offset1	Residual frequency offset with respect to the nominal carrier frequency. Part 1/2. 32-bit signed integer expressed as fcerror * 2^{32} / $\mathbf{f}_{clk\_p}$ SREG43 (LSB) – SREG46 (MSB)
Carrier frequency offset2	Residual frequency offset with respect to the nominal carrier frequency, measured at the start of burst. Part 2/2. 32-bit signed integer expressed as fcerror * 2^{30} / $\mathbf{f}_{symbol\_rate}$ SREG47 (LSB) – SREG50 (MSB)
reserved	SREG51 (LSB) – SREG52 (MSB)
CIC_R	Receiver decimation factor from $\mathbf{f}_{clk\_adc}$ to 4* $\mathbf{f}_{symbol\_rate\_rx}$. Valid range 1 - 16384 SREG53 (LSB) – SREG54 (MSB)
Signal presence detector false alarms	Number of false alarms in a 100ms window. The demodulator includes an adaptive threshold for detecting the presence of incoming bursts. The algorithm takes typically 10 seconds after power up to converge. When tracking, the algorithm will aim at 1 false alarm per 100ms. SREG61
Network monitoring	
LAN PHY ID	Expect 0x22 when LAN adapter is plugged in. SREG16
MAC address	Unique 48-bit hardware address (802.3). In the form SREG55:SREG56:SREG57:…:SREG60

Multi-byte status variables are latched upon (re-)reading SREG16.

ComScope Monitoring

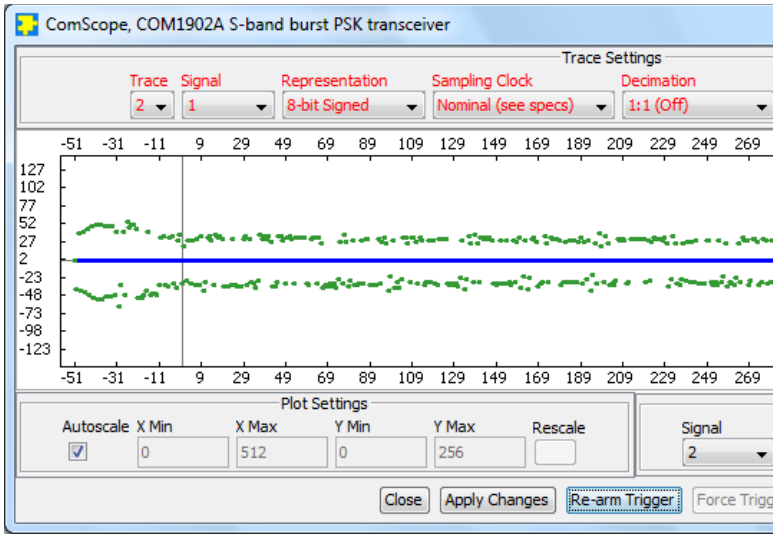
Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. Click on the button to start, then select the signal traces and trigger are defined as follows:

Trace 1 signals (demod)	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: I-channel samples, directly from ADC (after IF undersampling or baseband). Real-time.	8-bit signed	ADC clock f_{clk_adc}	512
2: Demodulated Q-channel at optimum sampling instant. (after elastic input buffer: use T2 trigger)	8-bit signed	1 samples / symbol	512
3: FFT magnitude	8-bit unsigned	ADC clock f_{clk_adc}	512
4: Signal presence detection level (in-burst)	8-bit unsigned	typ. every 90us	512
Trace 2 signals (demod)	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: I-channel input at near-zero center frequency	8-bit signed	ADC clock f_{clk_adc}	512
2: Reconstructed carrier phase (coarse)	8-bit unsigned	ADC clock f_{clk_adc}	512
4: Signal presence detection level (out of-burst)	8-bit unsigned	typ. every 90us	512
Trace 3 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: Demodulated I-channel at optimum sampling instant. (after elastic input buffer: use T2 trigger)	8-bit signed	1 samples / symbol	512
2: Cumulative symbol timing error	8-bit signed	symbol rate	512
3: Reconstructed carrier phase (fine)	8-bit unsigned	ADC clock f_{clk_adc}	512
4: Signal presence detection adaptive threshold (compare with actual detection level on Trace 1/signal 4)	8-bit unsigned	typ. every 90us	512
Trigger Signal	**Format**		
1: transmit burst boundaries	1-bit		
2: end of first sync word in rx burst	1-bit		

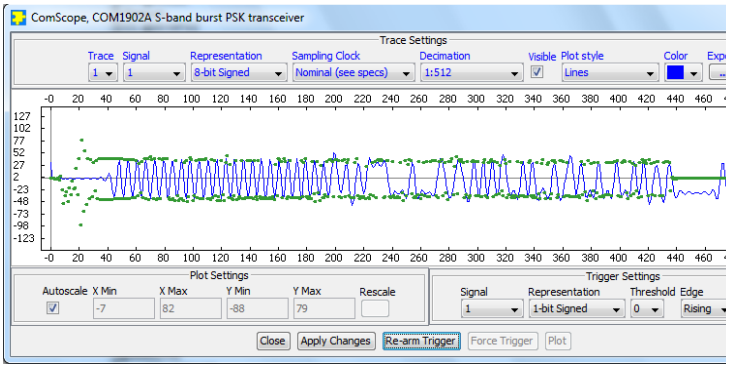
Signals sampling rates can be changed under software control by adjusting the decimation factor and/or selecting the f_{clk_adc} demod clock as real-time sampling clock.

In particular, selecting the f_{clk_adc} demod clock as real-time sampling clock allows one to have the same time-scale for all signals.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.



ComScope Window Sample: showing BPSK demodulated bits (green = I channel, blue = Q channel). Trigger on start of payload field.



ComScope Window Sample: showing baseband start of receive burst, mostly preamble (blue) and demodulated bits (green). Different time scales.

LEDs

LED	**Definition**
Power	Green when power is applied
Alarm (red)	Red when one of these conditions occur:

	• Tx RF frequency synthesizer is out of lock • Rx RF frequency synthesizer is out of lock
Tx	Blink green when a frame from LAN/UDP is being transmitted
Rx	Blink green when a received frame is forwarded to the LAN/UDP
Sync	Yellow when BER tester synchronized (while in test mode. Transmitter must send PRBS11 test sequence)
Tx on	Yellow when BER tester byte error (valid only if BER tester is synchronized)

Digital Test Points

The test points are only accessible after opening the enclosure. They are intended to be used only for debugging purposes.

Test Point	Definition
J4.1	Received UDP frame at port 1024
J4.2	Transmit burst boundaries (0 = idle)
J4.3	Modulator saturation
J4.4	Rx: Signal presence detected in receiver (FFT)
J4.5	Rx: Sync word detected in receiver (matched filter)
J4.6	Rx: payload data field
J4.7	Rx: Demodulator recovered carrier/center frequency (coarse)
J4.8	Rx: recovered symbol center
J4.9	Viterbi decoder input bit error (Option–**A**),or Turbo code decoder valid CRC frame (Option–**B**),
J4.10	BER tester synchronized
J4.11	BER tester matched filter output (detects start of PRBS11 sequence)
J4.12	Byte error detected by BER tester

Operation

Frequency reference

Two frequency references are software-selectable:

- external 10 MHz signal supplied through the front panel
- internal 19.2 VCTCXO

Warning: when selected as external frequency reference, the 10 MHz frequency reference must be present prior to powering on the modem.

If no 10 MHz signal is available and the modem expects such a signal, it is possible to reinitialize the modem by removing the backpanel (where the power switch is located) and pressing the hidden reset button. See the recovery section below.

Output 10 MHz frequency reference

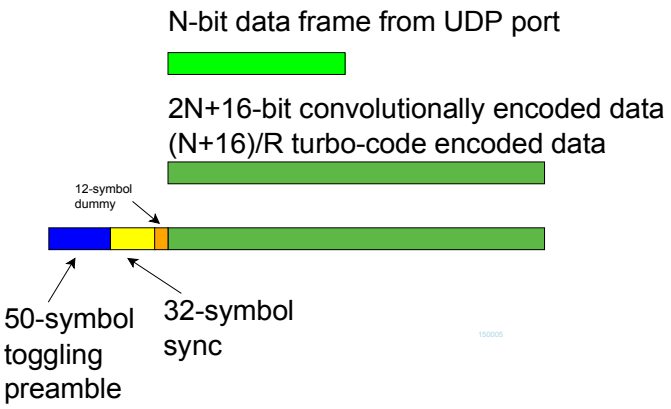
A 10 MHz frequency reference signal can be multiplexed with RF signals on the RF input (to an external LNB) and RF output (to an external BUC). The same 10 MHz is also available as an output on the front panel, labeled "10 MHz OUT". Each one of these three clocks signals can be enabled or disabled by software command.

Burst format

The modulator input receives fixed-length data frames over LAN/UDP. The size, ENC_FRAME_IN_SIZE is user-defined but should remain fixed during operation.

Upon UDP reception, the data frame is immediately FEC encoded with either a convolutional code K=9, rate ½ code or a rate R turbo code, depending on the firmware version. After convolutional code encoding, the encoded frame length is 2*ENC_FRAME_IN_SIZE+16 bits (including the 16 tail bits). After turbo code encoding, the encoded frame length is (ENC_FRAME_IN_SIZE+16)/R bits

The encoded frame is then encapsulated into a PSK frame comprising a short (50 symbols typically) preamble, a 32-symbol synchronization field and a 12-symbol dummy field.



When transmitting multiple frames, follow-on frames are appended without preamble, separated only with a 32-bit sync word + 12 symbol dummy field.

The sync word is 0x5A0FBE66

Transmission timing

A data frame received over UDP is transmitted without delay. The transmission time uncertainty is small (< TBD us). The user application is therefore fully in control of the burst scheduling, for example to prevent collisions in a multi-node radio network.

When the modulator is configured in PRBS11 test mode, the PRBS11 pseudo-random test sequence is generated internally, packetized in a fixed-length frame and transmitted one frame every 100 ms. The UDP input is ignored while in this test mode.

Input elastic buffer

When longer data is needed, multiple data frames can be queued for transmission in the input elastic buffer. The modulator expects any follow-on frame to be entirely within the input elastic buffer before the previous frame transmission is complete (so as to avoid transmitting another preamble). In this case, the modulator only inserts a 42-bit synchronization word between payload frames.

The input elastic buffer size is 8Kbit

Minimum burst duration

To guarantee receiver detection, the burst duration, including preamble and sync word must be greater than
(58.6 us + 256/nominal symbol rate),

For example, at 20 Msymbols/s, the minimum burst duration is 71.4 us.

Spacing between successive receive bursts (no a priori time-of-arrival information)

At high symbol rates, and when there is no a priori information about the time of arrival of bursts, there must be a minimum separation in time between successive bursts. The minimum time between the starts of two successive bursts is a complex function of the symbol rate and payload length:

65us + (256/symbol rate) +
4*(burst payload symbols+(symbol rate * 117.2us))/ f_{clk_adc}

Example1:
22 Msymbols/s, 2048-symbol burst: 192.3us min separation between starts of successive bursts.
In this case, the bursts are 96.8us long.

At lower symbol rates, this constraint does not apply because the minimum separation is less than the burst duration. For example:
5 Msymbols/s, 2048-symbol burst: 182.1us min separation between starts of successive bursts.
However, the bursts are always longer (426 us), so this constraint is practically void.

Symbol Rate

The receiver is capable of handling any symbol rate up to the specified 39.5 Msymbols/s.

The modulator implementation imposes a coarser granularity in the selected symbol rate. The modulator symbol rate steps are uneven but always within 0.2% of the target value. See the constraints when computing the modulator processing clock f_{clk_tx} (page 5)

The GUI calculates the precise modulation symbol rate based on the user's requirement. Please be sure to set the nominal demodulation symbol rate accordingly.

Threshold Eb/No

When configured for BPSK, turbo code rate 1/3, 1984 bits/frame, the frame error rate (FER) is as follows:
3.8 dB E_b/N_o, FER = 2%.
5.8 dB E_b/N_o, FER = 2.10^{-3}

Frequency acquisition & tracking

The frequency acquisition window is +/- 20% of symbol rate with no apriori knowledge.

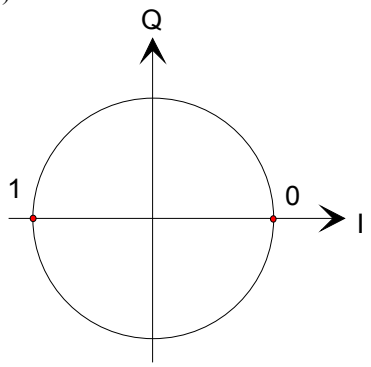
Once locked, the carrier tracking loops tracks the carrier phase over a very wide frequency range.

Constellation: Symbol Mapping

The packing of serial data stream into symbols is done with the Most Significant bit first.

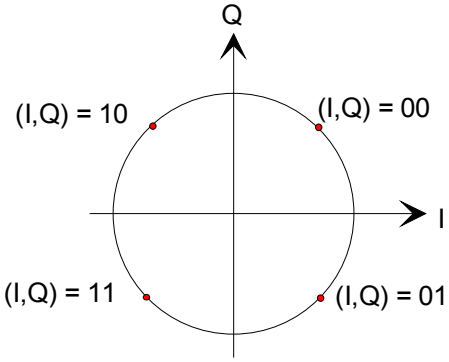
BPSK

REG70(5:0) = 0



QPSK

REG70(5:0) = 1
Gray encoding.

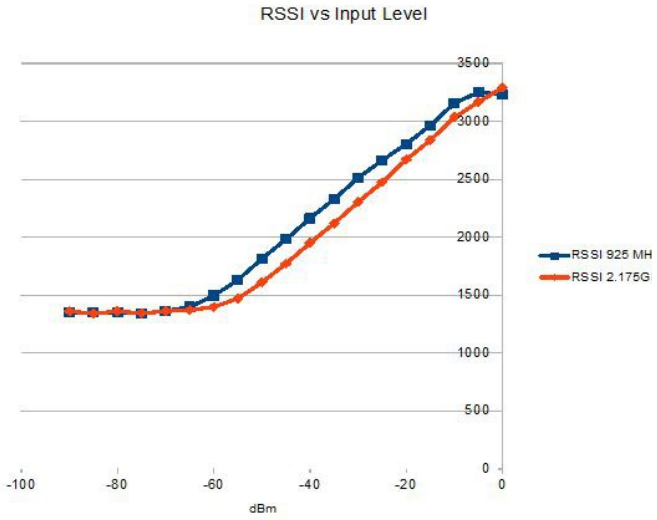


Format Conversion

Serial to parallel conversion occurs when converting the demodulated data stream into 8-bit byte over the UDP-IP link. The general rule is that the first received bit is placed at the MSb position in the byte.

RSSI

The RSSI measurements (as reported in status registers SREG5/6) versus the receiver input level is plotted below for the two extreme operational frequencies. The measurements are monotonous between -70 dBm and -5 dBm.



Note: RSSI measurement below –50Bm is affected by the presence of 10 MHz frequency reference when supplied to an external LNB (see control register REG46(2)).

Customization

The transceiver design can be customized to meet alternate customer requirements. The customizable features are

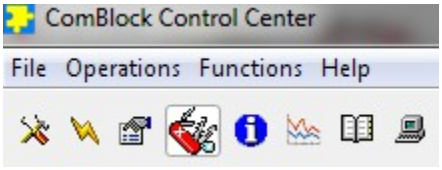
- Custom radio-frequency bands within 400 MHz– 3GHz at no extra charge.
- Trade-off preamble length versus acquisition threshold Eb/No. The baseline preamble is 1600 symbols for a threshold E_b/N_0 of 16 dB (PER > 99.9%). Lower threshold are achievable by increasing the integration time and thus the preamble length, down to E_b/N_0 of 5 dB for a preamble length of 32K symbols.

Customization has to be specified and quoted at the time of order.

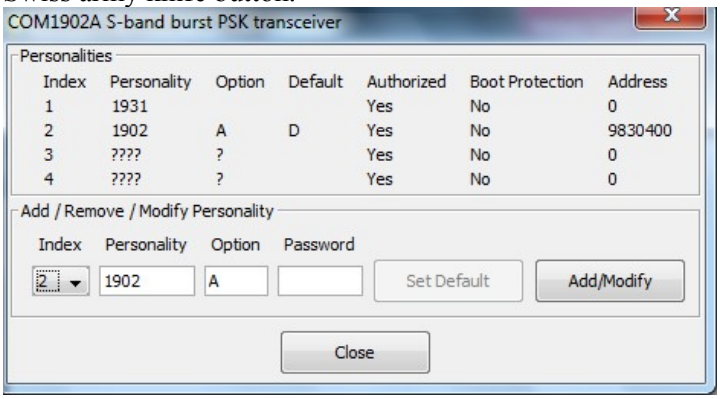
Load Software Updates

From time to time, ComBlock software updates are released.

To manually update the software, highlight the ComBlock and click on the Swiss army knife button.

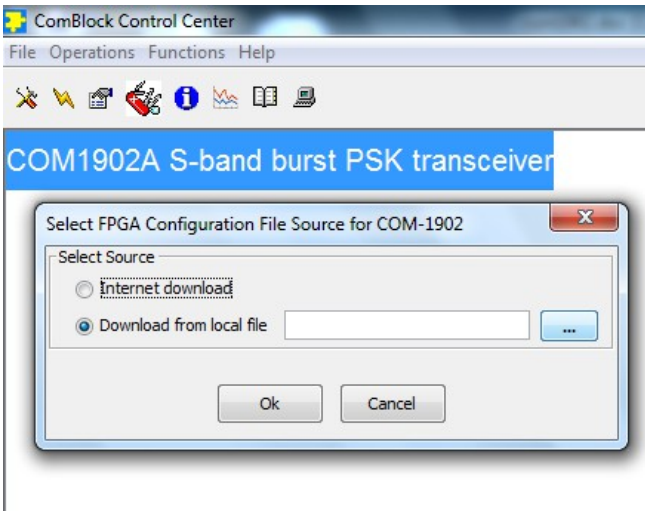


The receiver can store multiple personalities. The list of personalities stored within the ComBlock Flash memory will be shown upon clicking on the Swiss army knife button.



The default personality loaded at power up or after a reboot is identified by a ‘D’ in the Default column. Any unprotected personality can be updated while the Default personality is running.

Select the personality index and click on the "Add/Modify" button.



The software configuration files are named with the .bit extension. The bit file can be downloaded via the Internet, from the ComBlock CD or any other local file.

The option and revision for the software currently running within the FPGA are listed at the bottom of the advanced settings window.

Two firmware options are available for this receiver:
-A Convolutional rate ½ FEC
-B Turbo code FEC

Recovery

The toggle button under the backpanel can be used to

(a) prevent the FPGA configuration at power up. This can be useful if a bad FPGA configuration was loaded which resulted in loss of communication with the user.
(b) reset the LAN1 IP address to 172.16.1.128.

To prevent the FPGA configuration at power up, turn off power. Toggle the button. Turn on power, wait 1 second, then toggle the button a second time.

To reset the LAN1 IP address to a factory default of 172.16.1.128: Turn on power. Toggle the button, wait at least 30 seconds, during which time the red led blinks, then toggle the button a second time. Wait another 10 seconds, then cycle power off/on.

Interfaces

10/100/1000 Ethernet LAN for data, monitoring and control	RJ45 Supports auto MDIX to alleviate the need for crossover cable.
10 MHz frequency reference input	10 MHz frequency reference input for frequency synthesis. Sinewave, clipped sinewave or squarewave. SMA female connector Input is AC coupled. Minimum level 0.6Vpp. Maximum level: 3.3Vpp.
10 MHz frequency reference output	10 MHz frequency reference output
RF Rx	Receiver input. 50 Ohm, SMA female connector. Operating range: -60 to -10 dBm Maximum no damage input level: + 20 dBm Two other signals can be multiplexed onto the same coaxial connection between the COM-1902 transceiver and an external LNB: • 10 MHz frequency reference (software enabled) Level: -2 dBm typ. • 13/18V supply (software enabled)
RF Tx	Transmitter output. 50 Ohm, SMA female connector. Transmit level: -30 to 0 dBm, user selectable. One other signal can be multiplexed onto the same coaxial connection between the COM-1902 transceiver and an external BUC: • 10 MHz frequency reference (software enabled) Level: 0 dBm typ.

Operating input voltage range

Supply voltage	+18V min, +36V max 320mA typ. under +28VDC
Supply voltage (when no LNB 13/18V supply needed)	+5.6V min, +36V max

The positive voltage is on the center pin, the ground on the outer barrel.

Absolute maximum ratings

Supply voltage	+45 V max
RF input	+20dBm max

Mechanical Interface

Aluminum enclosure with rubberized end caps.
L x W x H: 168.5mm x 138.96 mm x 40.98 mm.
Includes two optional 40mm mounting flanges for mounting to a flat support plate.

Schematics

The board schematics are available on-line at
http://comblock.com/download/com_1900schematics.pdf

Configuration Management

This specification is to be used in conjunction with ComBlock control center revision 3.12s and above and the following:

ARM processor firmware version:
CB1900_1_6b.hex 6/20/17

FPGA/VHDL version:
COM1902_002k 8/4/17

It is possible to read back the option and version of the FPGA configuration currently active. Using the ComBlock Control Center, highlight the COM-1902 module, then go to the advanced settings. The option and version are listed at the bottom of the configuration panel.

Troubleshooting Checklist

Excessive power consumption:

- The receiver input is capable of supplying 13/18V DC to an external LNB. When using RF attenuators at the input in a RF loopback test, please make sure to use a DC block between the RFin and the attenuator.

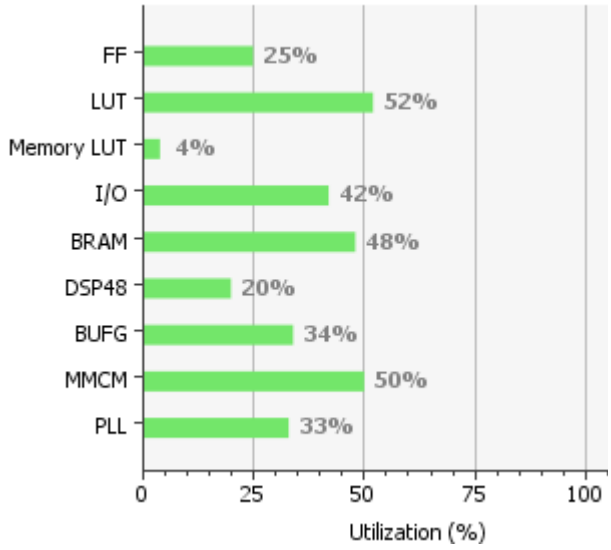
Demodulator can't achieve lock even at high signal-to-noise ratios:

- Make sure the modulator baseband I/Q signals do not saturate, as such saturation would strongly distort the modulation phase information. (this is a phase demodulator!)

VHDL code / IP core

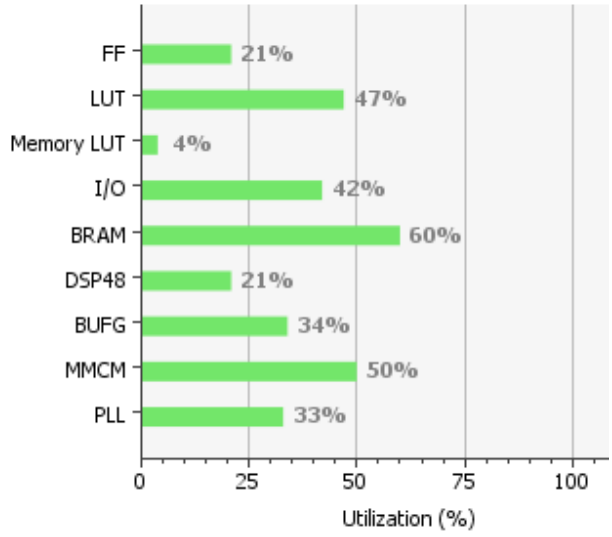
The FPGA code is written in VHDL. It does not use any third-party software. It occupies the following FPGA resources

Firmware Option **-A** (no AWGN)



Resource	Utilization	Available	Utilization %
FF	31574	126800	24.90
LUT	33098	63400	52.21
Memory LUT	836	19000	4.40
I/O	120	285	42.11
BRAM	65	135	48.15
DSP48	48	240	20.00
BUFG	11	32	34.38
MMCM	3	6	50.00
PLL	2	6	33.33

Firmware Option **-B**



Resource	Utilization	Available	Utilization %
FF	26902	126800	21.22
LUT	29879	63400	47.13
Memory LUT	849	19000	4.47
I/O	121	285	42.46
BRAM	81.5	135	60.37
DSP48	50	240	20.83
BUFG	11	32	34.38
MMCM	3	6	50.00
PLL	2	6	33.33

The maximum symbol rate is limited by the FPGA technology. For example nearly 40 Msymbols/s for Xilinx Artix 7 –1 speed (XC7A100T-1)

The IP core, which includes all VHDL source code, can be purchased separately. It is not needed to operate the ready-to-use COM-1902 transceiver.

ComBlock Ordering Information

COM-1902 L/S-band burst PSK transceiver

ECCN: 5A001.b.3

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