COM-1918 L/S-band spread-spectrum transceiver

Key Features

- L/S-band modem to send and receive continuous streams over wireless, satellite or cable. (for burst-mode see COM-1931)
- Direct-Sequence Spread-Spectrum (DSSS) modulation. Programmable chip rate, up to 40 Mchips/s
- Nominal frequency of operation: 950 – 2175 MHz for direct connection to external LNB or BUC. Customization to other frequency bands is possible.
- Acquisition: < 1 second for most configuration cases.
- Large frequency acquisition range: ±(chip_rate / 256)
- Spreading codes: Gold, Maximal length, Barker, GPS C/A.
- Symbol rate: practical range from chip_rate/2047 to chip_rate/3. Maximum processing gain: 33 dB. Spreading factor: 3 to 2047
- Demodulation performances: within 1.5 dB from theory at threshold Eb/No of 2 dB.
- Convolutional or Turbo code error correction, programmable rate.
- Built-in IP router with gigabit Ethernet LAN port
- Supply voltage: 18 – 36VDC with reverse voltage and surge protection. (5.6V min when not supplying external LNB)
- Frequency reference: internal TCXO or input for an external, higher-stability 10 MHz frequency reference.
- Built-in tools: PRBS-11 pseudo-random test sequence, BER tester, AWGN generator, internal loopback mode.
- Monitoring:
  - Carrier frequency error
  - SNR
  - BER
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.

For the latest data sheet, please refer to the **ComBlock** web site: http://www.comblock.com/download/com1918.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to http://www.comblock.com/product_list.html .

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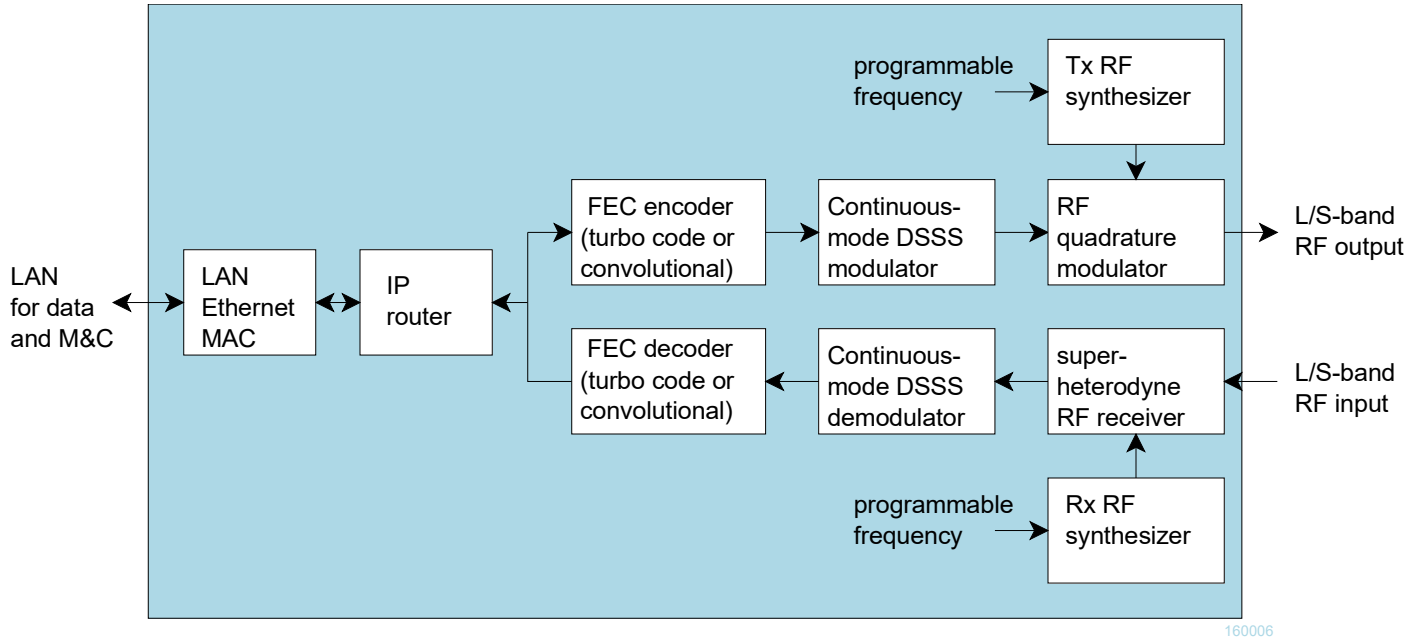
Functional Block Diagram

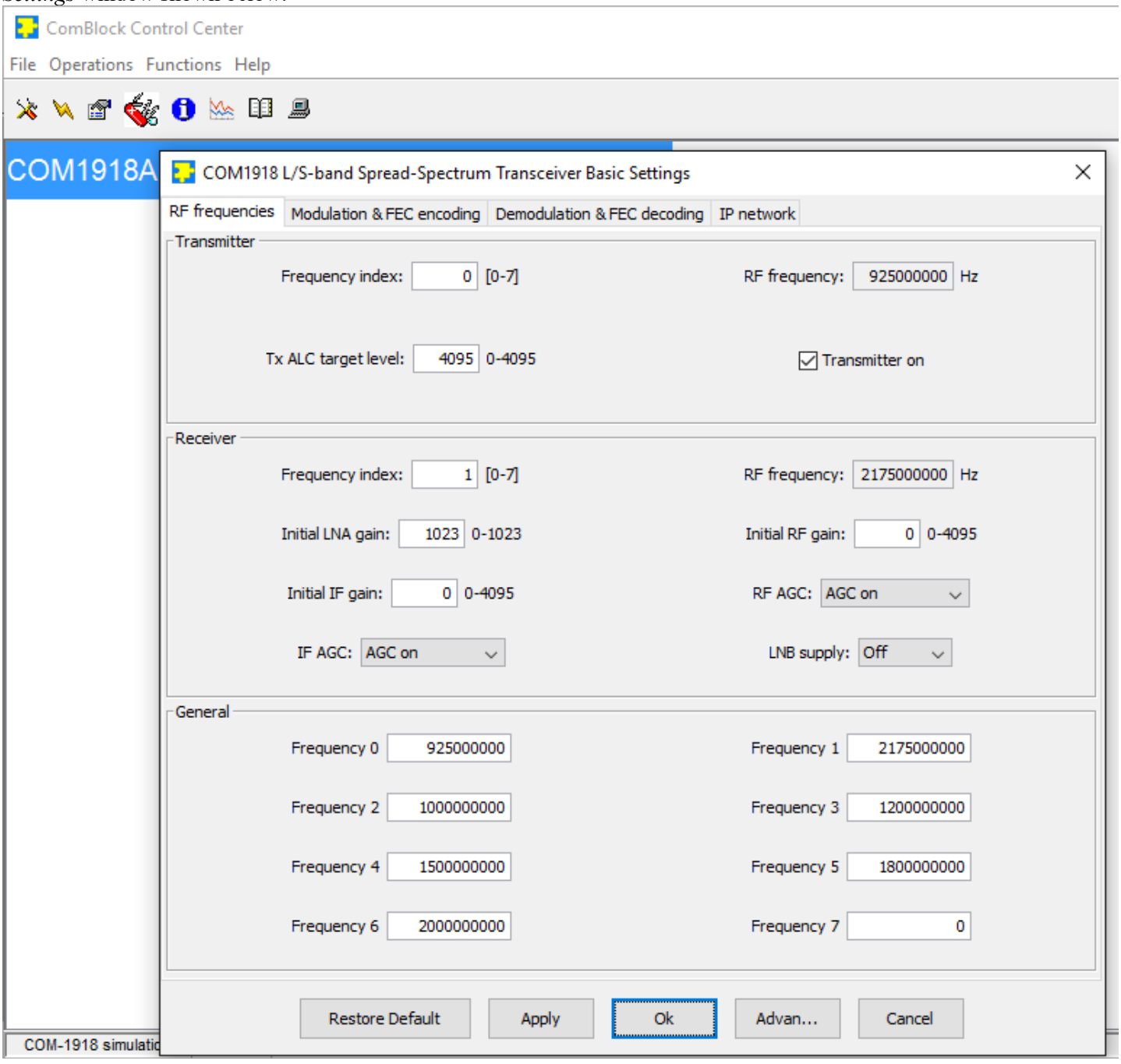


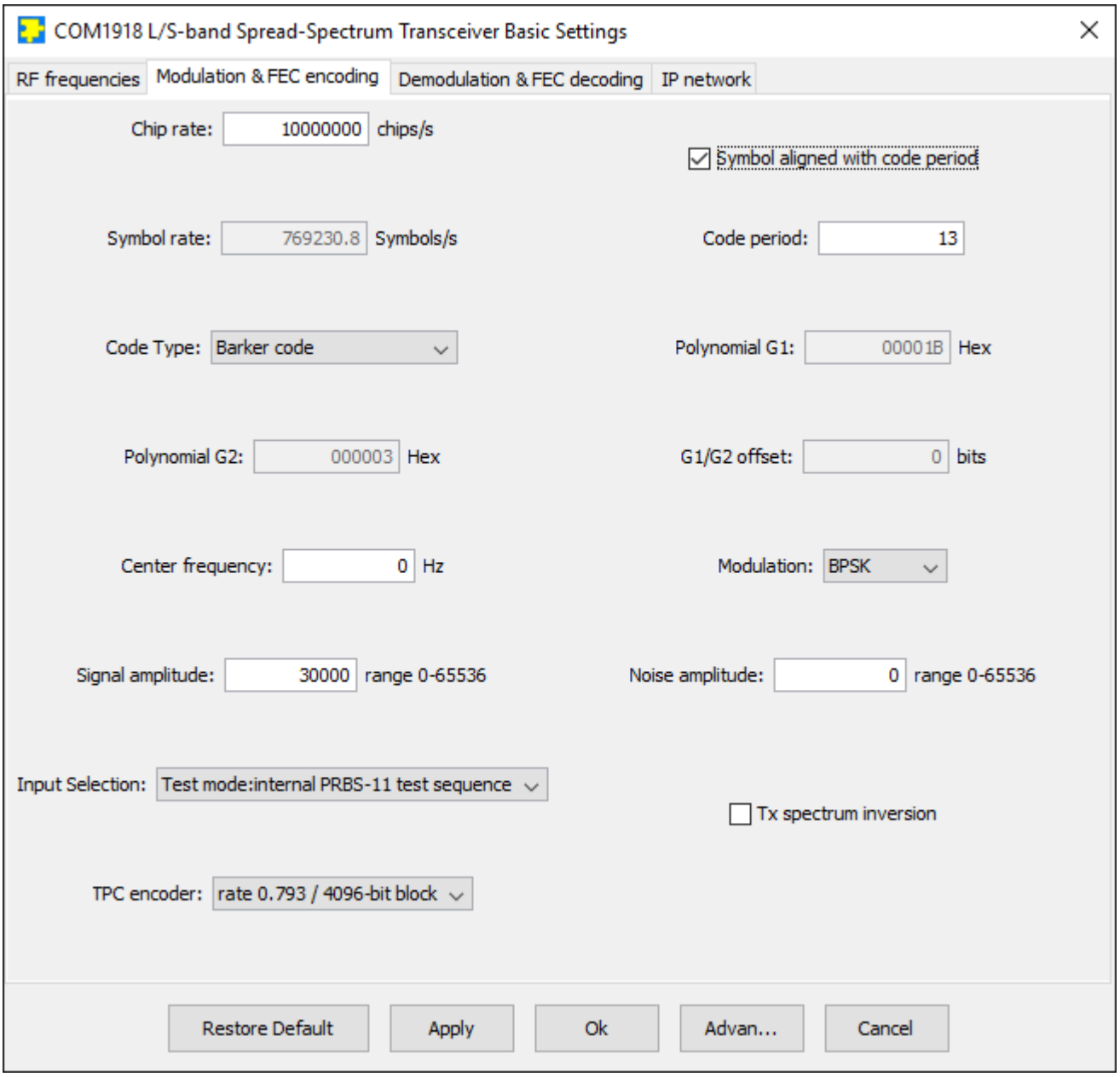
Configuration (Basic)

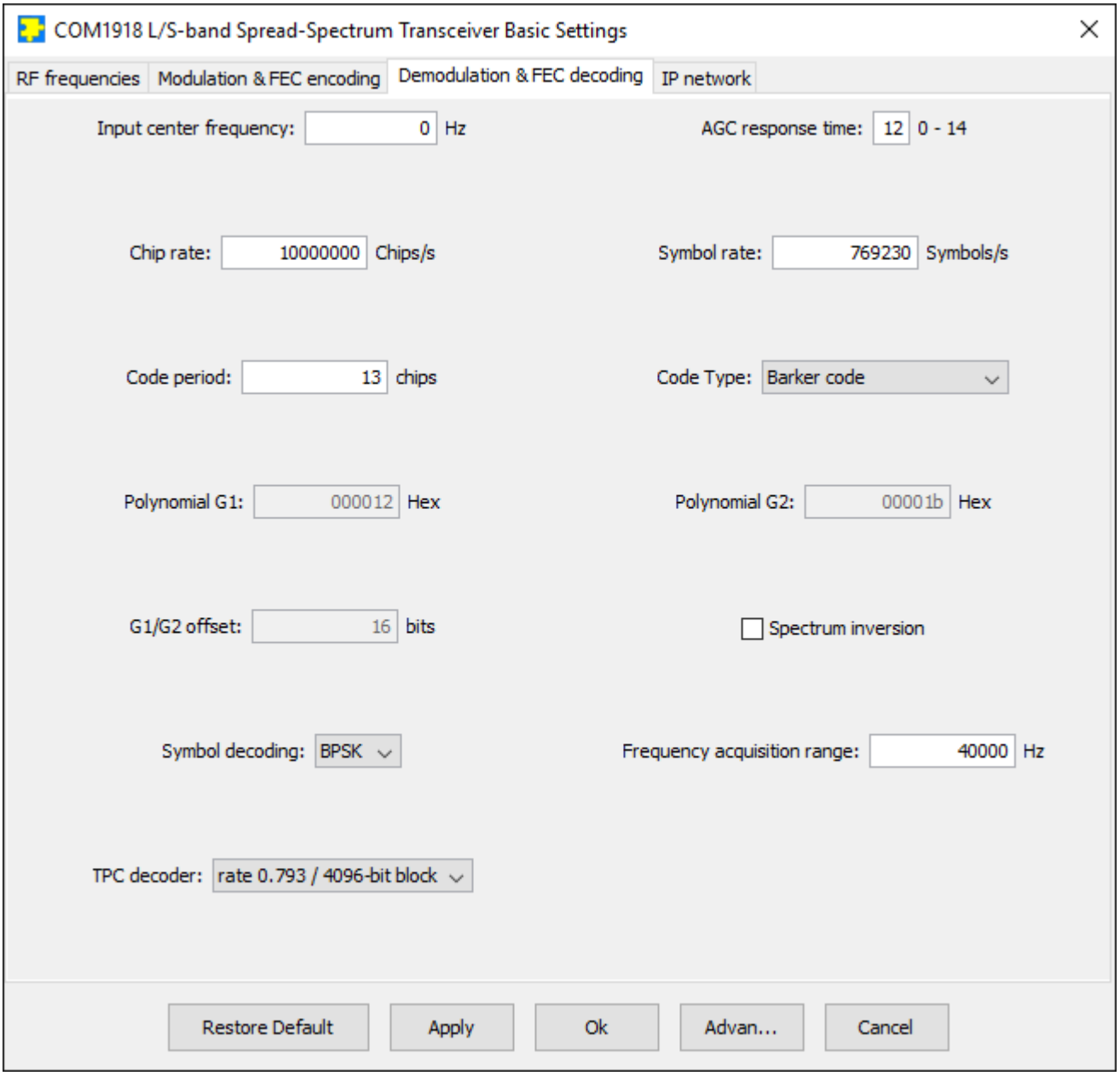
The easiest way to configure the COM-1918 is to use the **ComBlock Control Center** software supplied with the module on CD. Please follow the few simple steps described in the user manual "ccchelp.pdf" document to install the ComBlock Control Center software "ComBlock_Control_Center_windows_rev.exe"

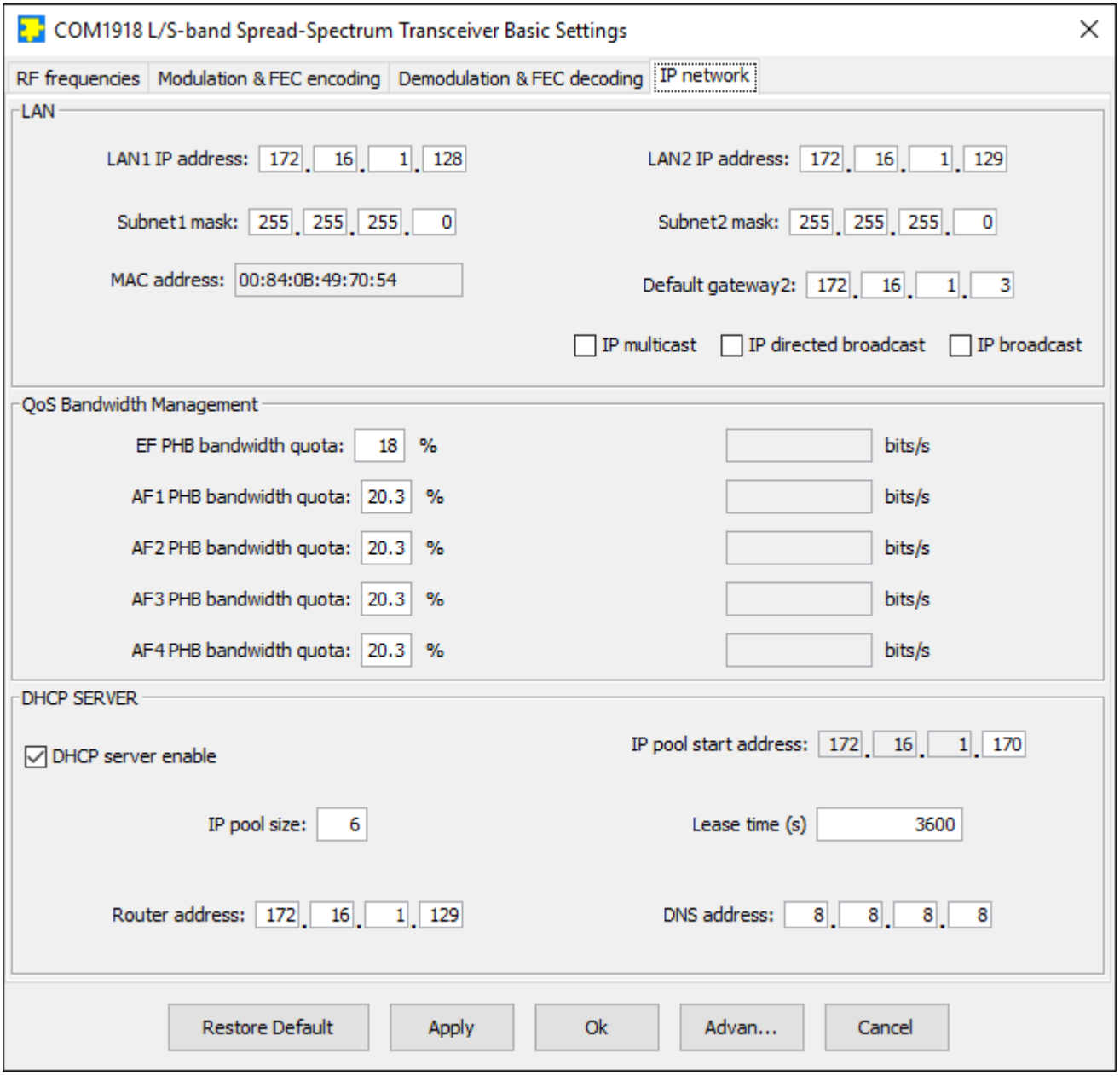
Connect the LAN cable between PC and transceiver RJ45 connector labeled "M&C LAN". Turn the transceiver power supply on and wait approximately 5-10 seconds. In the **ComBlock Control Center** window, click on the left-most button and select LAN as primary communication media. The default IP address is 172.16.1.128.

In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-1918 module to be configured, next click the *Settings* button to display the *Settings* window shown below.




COM1918 L/S-band Spread-Spectrum Transceiver Basic Settings
RF frequencies
Modulation & FEC encoding
Demodulation & FEC decoding
IP network
Chip rate:
10000000
chips/s
Symbol aligned with code period
Symbol rate:
769230.8
Symbols/s
Code period:
13
Code Type:
Barker code
Polynomial G1:
00001B
Hex
Polynomial G2:
000003
Hex
G1/G2 offset:
0
bits
Center frequency:
0
Hz
Modulation:
BPSK
Signal amplitude:
30000
range 0-65536
Noise amplitude:
0
range 0-65536
Input Selection:
Test mode:internal PRBS-11 test sequence
Tx spectrum inversion
TPC encoder:
rate 0.793 / 4096-bit block
Restore Default
Apply
Ok
Advan...
Cancel


COM1918 L/S-band Spread-Spectrum Transceiver Basic Settings
RF frequencies
Modulation & FEC encoding
Demodulation & FEC decoding
IP network
Input center frequency: 0 Hz
AGC response time: 12 0 - 14
Chip rate: 10000000 Chips/s
Symbol rate: 769230 Symbols/s
Code period: 13 chips
Code Type: Barker code
Polynomial G1: 000012 Hex
Polynomial G2: 00001b Hex
G1/G2 offset: 16 bits
Spectrum inversion
Symbol decoding: BPSK
Frequency acquisition range: 40000 Hz
TPC decoder: rate 0.793 / 4096-bit block
Restore Default
Apply
Ok
Advan...
Cancel



Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center "Advanced" configuration or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write. Definitions for the Control registers and Status registers are provided below.

Control Registers

The module configuration parameters are stored in volatile (SRT command) or non-volatile memory (SRG command). The stored configuration is automatically loaded up at power up. All control registers are read/write.

Note: several multi-byte fields like the IP addresses are enacted upon (re-)writing to the last control register (REG172)

Several key parameters are computed on the basis of the 160 MHz ADC clock $\mathbf{f_{clk\_adc}}$ or the 120 MHz internal processing clock $\mathbf{f_{clk\_p}}$.

RF	
Parameters	**Configuration**
Stored frequency $\mathbf{f_0}$	Preselected transmitter or receiver frequency $\mathbf{f_0}$. (one of eight stored frequencies) Valid range 925 MHz – 2.175 GHz, expressed in Hz. REG0: bit 7:0 (LSB) REG1: bit 15:8 REG2: bit 23:16 REG3: bit 31:24 (MSB)
Receiver frequency selection	Use to switch the receiver center frequency among preselected values. Range 0 through 7 REG6(2:0)
Transmitter frequency selection	Use to switch the transmitter center frequency among preselected values. Range 0 through 7 The rx/tx frequencies change is enacted upon writing to REG6. REG6(6:4)
Stored frequency $\mathbf{f_x}$	Seven additional preselected frequencies x = 1 through 7 Same format as $\mathbf{f_0}$. REG(3+4*x): bits 7:0 (LSB) REG(4+4*x): bits 15:8 REG(5+4*x): bits 23:16 REG(6+4*x): bits 31:24 (MSB)
Receiver RF Gain	Initial RF gain (before the RF AGC takes over). 12-bit. 0 for the minimum gain, 4095 for the maximum gain. The receiver RF gain change is enacted upon writing to REG5. REG4: bits 7:0 (LSB) REG5(3:0): bits 11:8
Receiver IF Gain	Initial IF gain (before the IF AGC takes over). 12-bit. 0 for the minimum gain, 4095 for the maximum gain. The receiver IF gain change is enacted upon writing to REG36. REG35: bits 7:0 (LSB) REG36(3:0): bits 11:8
Receiver LNA Gain	LNA gain 10-bit. 0 for the minimum gain, 1023 for the maximum gain. The receiver IF gain change is enacted upon writing to REG41. REG40: bits 7:0 (LSB) REG41(1:0): bits 9:8
Transmitter ALC target	The transmit gain is automatically adjusted so that the measured tx power equals this field. The transmitter gain change is enacted upon writing to REG38. REG37: bits 7:0 (LSB) REG38(3:0): bits 11:8
Receiver LNA AGC loop	0 = open loop. LNA path gain is fixed by control registers. 1 = AGC on. Gain is adjusted on the basis of the RSSI measurement. REG39(0)
Receiver RF AGC loop	0 = open loop. RF path gain is fixed by control registers.

	1 = AGC on. Out-of-range conditions are detected at the RF mixer and IF power detector. REG39(1)
Receiver IFAGC loop	0 = open loop. IF1 path gain is fixed by control registers. 1 = AGC on. Out-of-range conditions are detected at the IF power detector. REG39(3:2)
Transmitter ON	0 = off 1 = on REG39(6)
LNB supply	The transceiver is capable of supplying up to 500mA at 13VDC or 18VDC to an external LNB. This supply voltage is multiplexed with the RF input signal onto the "RF Rx" input. 0 = LNB supply off 1 = LNB supply on **Warning: Enabling the LNB supply may cause damage to test equipment unless a DC block is used.** REG43(0)
LNB supply 13V vs 18V	0 = 13VDC LNB supply 1 = 18VDC LNB supply REG43(1)
General Parameters	**Configuration**
Internal/External frequency reference	10 MHz output generated from 10 MHz input (-B firmware option) or 19.2 MHz TCXO (-A firmware option) REG46(1): enable(1)/disable(0) CLKREF_OUT (special connector on front-panel) REG46(2): enable(1)/disable(0) CLK_LNB (multiplexed with received signal) REG46(3): enable(1)/disable(0) CLK_TX (multiplexed modulated transmit signal + 10 MHz)
FEC encoding	0 = bypassed 1 = FEC encoding enabled REG47(0)
FEC decoding	0 = bypassed 1 = FEC decoding enabled REG47(1)
Turbo code encoder Uncoded payload size in Bytes.	Preferred sizes: 14, 63, 250 Bytes Must NOT be an integer multiple of 15 Maximum 254 Bytes. REG162
FEC encoder rate (turbo code or convolutional, depending on active firmware)	0 = rate 1/3 (turbo code only) 1 = rate 1/2 2 = rate 2/3 3 = rate 3/4 4 = rate 4/5 (turbo code only) 5 = rate 5/6 6 = rate 6/7 (turbo code only) 7 = rate 7/8 REG164(3:0)
Turbo code encoder Encoded frame size in bits	Encoded frame size in bits. For example: when payload size is 14, rate 1/3, the encoded frame size is 14*8*3 = 336 bits. Does not include any periodic synchronization field. REG165 LSB REG166(6:0) (MSB)
Turbo code decoder Decoded payload size in Bytes.	Preferred sizes: 14, 63, 250 Bytes Must NOT be an integer multiple of 15 Maximum 254 Bytes. REG167
FEC decoder rate (turbo code or	0 = rate 1/3 (turbo code only)

Viterbi, depending on active firmware)	1 = rate 1/2 2 = rate 2/3 3 = rate 3/4 4 = rate 4/5 (turbo code only) 5 = rate 5/6 6 = rate 6/7 (turbo code only) 7 = rate 7/8 REG168(3:0)
Turbo code decoder Coded frame size in bits	Coded frame size in bits. For example: when payload size is 14, rate 1/3, the coded frame size is 14*8*3 = 336 bits. Does not include any periodic synchronization field. REG169 LSB REG170(6:0) (MSB)
Turbo code decoder maximum number of iterations	1 – 15. Typical settings is 7. Must be an odd number REG171
DSSS Modulator	
Parameters	**Configuration**
Processing clock f_{clk_tx}	Modulator processing clock. Also serves as DAC sampling clock. Expressed as as f_{clk_tx} = 120 MHz * M / (D * O)) where D is an integer divider in the range 1 - 106 M is a multiplier in the range 2.0 to 64.0 by steps of 1.0. Fixed point format 7.3 O is a divider in the range 2.0 to 128.0 by steps of 1.0. Fixed point format 7.3 Note: the graphical use interface computes the best values for M, D and O. f_{clk_tx} recommended range 80-160 MHz. REG48(6:0) = D REG49 = M(7:0) REG50(1:0) = M(9:8) REG51 = O(7:0) REG52(2:0) = O(10:8)
Chip rate $f_{chip\ rate\ tx}$	The modulator chip rate is in the form $f_{chip\ rate\ tx} = f_{clk\_tx} / 2^n$ where n ranges from 1 (2 samples per chip) to 15 (chip rate = f_{clk_tx} / 32768). n is defined in REG53(3:0)
Code period	In chips. Valid range 3 – 65535 Can be less than the natural length of the selected code. In which case, the code is truncated. REG54: LSB REG55: MSB
Code selection	1 = Gold code (G1/G2 software selection) 2 = Maximal length sequence (G1 software selection) 3 = Barker code (lengths 11 or 13 only) 4 = GPS C/A code REG56(3:0)
Gold sequence / Maximal Length Sequence generator polynomial G1	24-bit. Describes the taps in the linear feedback shift register 1: Bit 0 is the leftmost tap (2^0 in the polynomial). The largest non-zero bit is the polynomial order n. n determines the code period $2^n - 1$. Example: G1 = $1 + x + x^4 + x^5 + x^6$ is represented as 0x000039 This field is used only if Gold code or Maximal length sequences are selected.

	REG57 = LSB REG58 REG59 = MSB
Gold code generator polynomial G2	24-bit. Describes the taps in the linear feedback shift register 2: Same format as G1 above. This field is used only if Gold codes are selected. REG60 = LSB REG61 REG62 = MSB
Gold code G1/G2 phase offset	A Gold code is generated by adding two maximal length sequences (as defined by their generator polynomials G1 and G2). A set of orthogonal Gold codes can be created by changing the phase offset between the two maximal length sequences. REG77 = bits 7 – 0 (LSB) REG78 = bits 15 – 8 REG79 = bits 23 – 16 (MSB)
Symbol rate f_{symbol_rate}	The symbol rate can be set independently of the spreading code period. In this case, set REG63-66 such that $f_{symbol\_rate} * 2^{32} / f_{clk\_tx}$ REG63 = LSB REG64 REG65 REG66 = MSB Alternatively, symbols can be aligned with the spreading code period. In this case, REG66(7) as '1'. REG63-65 are ignored.
Digital Signal gain	16-bit amplitude scaling factor for the modulated signal. The maximum level should be adjusted to prevent saturation. The settings may vary slightly with the selected symbol rate. Therefore, we recommend checking for saturation at the D/A converter when changing either the chip rate or the signal gain. Enacted upon writing the MSB. REG67 = LSB REG68 = MSB
Additive White Gaussian Noise gain	16-bit amplitude scaling factor for additive white Gaussian noise. Because of the potential for saturation, please check for saturation at the D/A converter when changing this parameter. REG69 = LSB REG70 = MSB
Modulation type	Modulation type before applying the direct-sequence spreading. Note: the modulation symbol transitions are not necessarily aligned with the chip transitions. 0 = BPSK 1 = QPSK REG71(5:0)
Spectrum inversion	Invert Q bit. (Inverts the modulated spectrum only, not the subsequent frequency translation) 0 = off 1 = on REG71(6)
Tx filter bypass	0 = root raised cosine 20% rolloff transmit filter is enabled 1 = bypass transmit filters REG71(7)
Input selection / format, test modes	Select the origin of the modulator input data stream. 0 = IP router WAN interface 1 = test sequence: internal generation of 2047-bit periodic pseudo-random bit sequence as

	modulator input. (overrides external input bit stream) 2 = test sequence: unmodulated carrier. This helps checking the follow-on RF modulator. 3 = spread-spectrum modulation without data. Test sequences override external input bit stream. REG72(2:0)
Output Center frequency (f_{c_tx})	Fine tuning of center frequency. Typically 0 Hz. 32-bit signed integer (2's complement representation) expressed as $f_{c\_tx} * 2^{32} / f_{clk\_tx}$ For a clean output waveform, we recommend keeping the maximum frequency (center frequency + ½ symbol rate) below 1/10th of the processing clock f_{clk_tx}. Note: as the AWGN noise samples are not frequency translated, noise tests should only be performed while the center frequency translation is smaller than the modulation bandwidth. REG73: LSB REG74 REG75 REG76: MSB
Sinusoidal frequency offset	In addition to the fixed frequency offset above, a sinusoidal frequency offset can be generated to mimic Doppler rate in highly mobile applications. This offset is characterized by two parameters: amplitude and period. The amplitude (a frequency) is expressed as $f_{c\_amplitude} * 2^{32} / f_{clk\_tx}$ in the following control registers: REG150: LSB REG151 REG152 REG153: MSB The period is expressed as $2^{32} /(f_{clk\_tx} *T)$ in the following control registers: REG154: LSB REG155 REG156 REG157: MSB
DSSS Demodulator	
Parameters	**Configuration**
Tx-Rx loopback	REG42(0): enable (1) or disable(0) loopback test mode
Input frequency offset (f_{c_rx})	Modulated signal center frequency offset. Typically 0. 32-bit signed integer (2's complement representation) expressed as $f_{c\_rx} * 2^{32} / f_{clk\_adc}$ REG85: LSB REG86 REG87 REG88: MSB
AGC response	REG89(4:0)
Spectrum inversion	Invert Q bit. 0 = off 1 = on REG89(5)
BPSK / QPSK decoding	Note: the modulation symbol transitions are not necessarily aligned with the chip

	transitions. 0 = BPSK 1 = QPSK REG89(6)
Nominal chip rate $f_{chip\_rate\_rx}$	32-bit integer expressed as $f_{chip\_rate\_rx} * 2^{32} / f_{clk\_adc}$ The maximum practical chip rate is 40 Mchips/s Example 10 Mchips/s: 0x10000000 The maximum allowed error between transmitted and received chip rate is +/- 100ppm. REG81 = bits 7-0 (LSB) REG82 = bits 15 – 8 REG83 = bits 23 – 16 REG84 = bits 31 – 24 (MSB)
Nominal symbol rate f_{symbol_rate}	The symbol rate can be set independently of the spreading code period as $f_{symbol\_rate} * 2^{32} / f_{clk\_adc}$ REG90 = bits 7 – 0 (LSB) REG91 = bits 15 – 8 REG92 = bits 23 – 16 REG93 = bits 31 – 24 (MSB)
Spreading factor (Processing gain)	Approximate (i.e truncated) ratio of chip rate / symbol rate Range: 3 – 8191 Note: to effectively achieve this processing gain, the code period must be longer than one symbol duration. REG94 = bits 7 – 0 (LSB) REG95(4:0) = bits 8 – 12 (MSB)
Code period	In chips. Valid range 3 – 65535 Can be less than the natural length of the selected code. In which case, the code is truncated. REG96 LSB REG97 MSB
Code selection	1 = Gold code 2 = Maximal length sequence 3 = Barker code (lengths 11 or 13 only) REG80(2:0)
Gold sequence / Maximal Length Sequence generator polynomial G1	24-bit. Describes the taps in the linear feedback shift register 1: Bit 0 is the leftmost tap (2^0 in the polynomial). The largest non-zero bit is the polynomial order n. n determines the code period $2^n - 1$. Example: G1 = $1 + x + x^4 + x^5 + x^6$ is represented as 0x000039 This field is used only if Gold code or Maximal length sequences are selected. REG98 = bits 7 – 0 (LSB) REG99 = bits 15 – 8 REG100 = bits 23 – 16 (MSB)
Gold code generator polynomial G2	24-bit. Describes the taps in the linear feedback shift register 2: Same format as G1 above. This field is used only if Gold codes are selected. REG101 = bits 7 – 0 (LSB) REG102 = bits 15 – 8

	REG103 = bits 23 – 16 (MSB)
Gold code G1/G2 phase offset	A Gold code is generated by adding two maximal length sequences (as defined by their generator polynomials G1 and G2). A set of orthogonal Gold codes can be created by changing the phase offset between the two maximal length sequences. REG104 = bits 7 – 0 (LSB) REG105 = bits 15 – 8 REG106 = bits 23 – 16 (MSB)
Network Interface	
Parameters	**Configuration**
LAN1 IP address	LAN1 is for monitoring & control only. No payload data traffic. 4-byte IPv4 address. Example : 0x AC 10 01 80 designates address 172.16.1.128 REG132 (MSB) - REG135(LSB)
LAN1 Subnet mask	Typically 0x FF FF FF 00 (255.255.255.0) REG136 (MSB) - REG139(LSB)
LAN2 IP address	LAN1 is for payload data traffic. No monitoring and control capabilities. 4-byte IPv4 address. Example : 0x AC 10 01 80 designates address 172.16.1.128 The new address becomes effective immediately (no need to reset the ComBlock). REG140 (MSB) - REG143(LSB)
LAN2 Subnet mask	Typically 0x FF FF FF 00 (255.255.255.0) REG144 (MSB) – REG147(LSB)
LAN2 Gateway IP address	Where to forward IP frames received over the modem link but not destined to this LAN. REG108 (MSB) - REG111 (LSB)
IP forwarding	The IP router can be configured to forward(1) or not forward (0): REG148(0): IP multicast frames REG148(1): IP directed broadcast frames REG148(2): IP broadcast frames The recommended setting is zero.
LAN MAC address LSB	REG107(7:1). To ensure uniqueness of MAC address. The MAC address most significant bytes are tied to the FPGA DNA ID. However, since Xilinx cannot guarantee the DNA ID uniqueness, this register can be set at the time of manufacturing to ensure uniqueness.

DHCP server	
Parameters	**Configuration**
Enable DHCP server	Enable(1)/disable(0) DHCP server. The DHCP server automatically assigns IP addresses to devices on the LAN. REG112(0)
IP pool starting address	The DHCP server assigns IP addresses from a pool of contiguous addresses, starting at address x.y.z.REG54, where x.y.z are the most significant bytes of this IP router. REG113
IP pool size	Number of IP addresses in the DHCP pool. Constraint1: maximum 253. Constraint2: IP router IP address must be outside the pool address. Constraint3: REG113+REG114 < 254 REG114
Lease time	Lease time (in seconds) for the IP addresses dynamically assigned by the DHCP. REG115 (LSB) - REG118 (MSB)

Gateway IP address	In addition to assigning an IP address to devices which request it, the DHCP server informs those devices of the designated gateway IP address. In most cases, this IP address is that of the IP router (see control REG100-103) REG119 (MSB) – REG122 (LSB)
DNS address	In addition to assigning an IP address to devices which request it, the DHCP server informs those devices of a Domain Name Server (DNS) IP address. For example 8.8.8.8 for Google DNS. REG123 (MSB) – REG126 (LSB)
QoS bandwidth management LAN -> WAN IP forwarding	
EF PHB bandwidth quota (%)	Differentiated Services configuration: Percentage of the overall LAN-to-WAN transmit bandwidth allocated to the Expedited Forwarding (EF). Expressed as percentage: 128 represents 100%. REG127
AF1 PHB bandwidth quota (%)	Differentiated Services configuration: Percentage of the overall LAN-to-WAN transmit bandwidth allocated to the Assured Forwarding class 1 (AF1). Expressed as percentage: 128 represents 100%. REG128
AF2 PHB bandwidth quota (%)	Differentiated Services configuration: Percentage of the overall LAN-to-WAN transmit bandwidth allocated to the Assured Forwarding class 2 (AF2). Expressed as percentage: 128 represents 100%. REG129
AF3 PHB bandwidth quota (%)	Differentiated Services configuration: Percentage of the overall LAN-to-WAN transmit bandwidth allocated to the Assured Forwarding class 3 (AF3). Expressed as percentage: 128 represents 100%. REG130
AF4 PHB bandwidth quota (%)	Differentiated Services configuration: Percentage of the overall LAN-to-WAN transmit bandwidth allocated to the Assured Forwarding class 4 (AF4). Expressed as percentage: 128 represents 100%. REG131

Note: several multi-byte fields like the IP addresses are enacted upon (re-)writing to the last control register (REG172)

Monitoring

Status Registers

Multi-byte status variables are latched upon (re-)reading SREG16.

Parameters	Monitoring
Hardware self-check	At power-up, the hardware platform performs a quick self check. The result is stored in status registers SREG0-4, SREG16-18 Properly operating hardware will result in the following sequence being displayed: SREG0-SREG4 = 01 F1 1D xx 7F, where xx (bad NAND flash sectors) must be less than 10 SREG16-18 = 0x22 22 87
Power supply check	SREG4(0): PGOOD1 RF1_+3.1V SREG4(1): PGOOD2 IF1+_3.1V SREG4(2): PGOOD3 A_+4.75V SREG4(3): PGOOD4 MOD_+4.8V SREG4(4): PGOOD5 TX_SYNTH_+3.3V SREG4(5): PGOOD6 RX_+4.75V SREG4(6): PGOOD7 RX_SYNTH_+3.3V

	Overall valid response: 0x7F
RSSI	Received signal strength indicator. 12-bit number Practical range –70 to -5 dBm after LNA See RF_POWER_DET1 in schematic. SREG5 = LSB SREG6(3:0) = MSB
Received power at RF mixer	Power detection at RF mixer. Target is 0xEC0 while the RF AGC is tracking See RF_POWER_DET2 in schematic. SREG7 = LSB SREG8(3:0) = MSB
Received power at IF	Power detection at IF after bandpass filter and IF gain control. Target is 0xE80 while the IF AGC is tracking. See IF1_POWER_DET in schematic. SREG9 = LSB SREG10(3:0) = MSB
Transmit power	Power detection at the RF transmit output. See TX_POWER_DET in schematic. SREG11 = LSB SREG12(3:0) = MSB
RF synthesizers locked	'1' when locked SREG19(0): rx synthesizer locked SREG19(1): tx synthesizer locked
FEC codec type	0 = convolutional K=7 rate ½ 1 = turbo code SREG19(7 downto 4)
DSSS demodulator monitoring	
Carrier lock status	SREG20(0) 0 = unlocked 1 = locked
Code lock status	SREG20(1) 0 = unlocked 1 = locked
Signal presence (from FFT)	SREG20(2) 0 = not present 1 = present
Despread signal power S	Average signal power after despreading. Compute the signal to noise ratio after despreading as S/N. The absolute value is meaningless because of multiple agcs. SREG21 = bits 7 – 0, LSB SREG22 = bits 15 – 8, MSB
Noise power N	Average noise power. Used to compute the SNR after despreading. The absolute value is meaningless because of multiple agcs. SREG23 = bits 7 – 0, LSB SREG24 = bits 15 – 8, MSB
Carrier frequency offset1	Residual frequency offset with respect to the nominal carrier frequency. Part 1 of 2: 32-bit signed integer expressed as fcdelta * 2^{32} / f_{clk_adc} SREG25 (LSB) – SREG28(MSB)
Carrier frequency offset2	Residual frequency offset with respect to the nominal carrier frequency. Part 2 of 2: 32-bit signed integer expressed as fcdelta * 2^{31} / f_{chip_rate} SREG60 (LSB) – SREG63(MSB)
Turbo code decoder monitoring	
Parameters	**Monitoring**
Sync word BER	Raw BER (no error correction) counted in the 32-bit sync words (counted over 1024 sync bits) SREG32 = bits 7 – 0 (LSB) SREG33 = bits 15 – 8 (MSB)
Viterbi FEC decoder monitoring	
Parameters	**Monitoring**

Synchronized	(FEC_DEC_LOCK_STATUS variable) Solid '1' when the Viterbi decoder is locked. '0' or toggling when unlocked. SREG30(0)
Decoder built-in BER	The Viterbi decoder computes the BER on the received (encoded) data stream irrespective of the transmitted bit stream. Encoded stream bit errors detected over a 1000-bit measurement window. SREG31 = bits 7 – 0 (LSB) SREG32 = bits 15 – 8 SREG33 = bits 23 – 16 (MSB)
BER tester monitoring	
Bit error rate	Monitors the BER (number of bit errors over 1,000,000 received bits) when the modulator is sending a PRBS-11 test sequence. SREG35: LSB SREG36: SREG37: SREG38: MSB
BER tester synchronized	SREG34(0): 1 when the BERT is synchronized with the received PRBS-11 test sequence.
Transmit SNR calibration	
Parameters	**Monitoring**
Measured modulated signal power	SREG54(LSB) SREG55 SREG56(MSB)
Measured AWGN power (Noise bandwidth is twice the modulated spread-spectrum signal bandwidth)	SREG57(LSB) SREG58 SREG59(MSB)
Tx saturation	Proper operation is predicated on operating in a linear channel, i.e. one without saturation. Saturation may occur after changing the symbol rate, the signal level or the noise level. Please verify the absence of saturation by reading this status register after adjusting these controls. Saturation occurrence in the last one second window for the following signals: Bit 0: PSK modulator output Bit 1: noise I-channel Bit 2: noise Q-channel Bit 3: signal + noise, I channel Bit 4: signal + noise, Q channel SREG39
IP router monitoring	
Parameters	**Monitoring**
MAC addresses	The 48-bit LAN1 ethernet MAC address is fixed and unique for each transceiver. It is displayed in status registers 19-24. The LAN2 Ethernet MAC address is incremented by one. SREG40-45
Transmitted to WAN	Monitors the number of payload bytes forwarded to WAN (does not include HDLC overhead or empty frames). 32-bit counter. SREG46 (LSB) to SREG49 (MSB)
Received from WAN	Monitors the number of payload bytes received from WAN (does not include HDLC overhead or empty frames). 32-bit counter. SREG50 (LSB) to SREG53 (MSB)

ComScope Monitoring

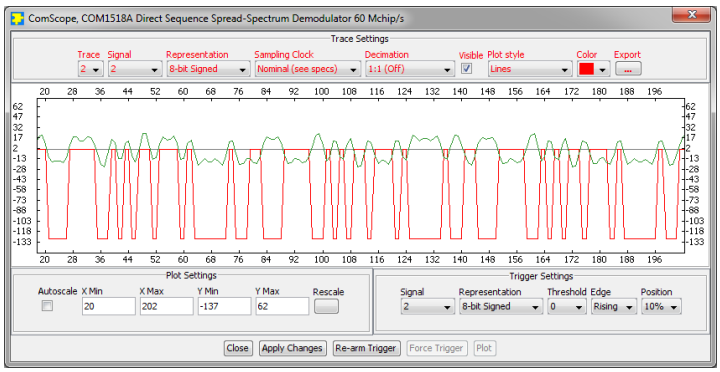
Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. Click on the button to start, then select the signal traces and trigger are defined as follows:

Trace 1 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: IF Input signal	8-bit signed	Input sampling rate	512
2: Input signal (I-channel) after AGC, frequency translation, decimation	8-bit signed	Input sampling rate/R	512
3: Despread I-channel, after coherent I&D	8-bit signed	2 samples / symbol	512
Trace 2 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
2: Code replica. Compare with spread input signals	8-bit signed	2 samples/chip	512
3: Demodulated I-channel	8-bit signed	1 sample / symbol	512
Trace 3 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: spread I-channel after carrier tracking and channel LPF	8-bit signed	2 samples/chip	512
2: Code tracking phase correction (accumulated)	8-bit signed	2 samples / symbol	512
3: Carrier tracking phase	8-bit signed	Input sampling rate/R	512
4: Symbol tracking phase (accumulated)	8-bit signed	1 sample / symbol	512
Trace 4 signals	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: 2(S+N)/N after despreading. Valid only if code is locked. Linear (i.e. not in dBs)	8-bit unsigned	f_{clk}	512
Trigger Signal	**Format**		
1: Start of code replica	Binary		
2. Code Lock	Binary		

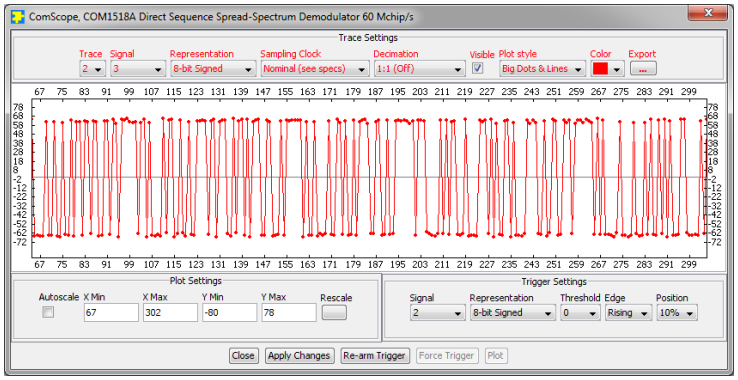
Signals sampling rates can be changed under software control by adjusting the decimation factor and/or selecting the f_{clk} processing clock as real-time sampling clock.

In particular, selecting the f_{clk} processing clock as real-time sampling clock allows one to have the same time-scale for all signals.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.



ComScope example, showing code lock with aligned: received spread signal after RRC filter (green) vs code replica (red)



ComScope example: showing demodulated I-channel

. LEDs

LED	Definition
Power	Green when power is applied
Alarm (red)	Red when one of these conditions occur: • Tx RF frequency synthesizer is out of lock • Rx RF frequency synthesizer is out of lock
Tx	Blink green when an IP frame is forwarded from LAN to WAN
Rx	Blink green when an IP frame is forwarded from WAN to LAN
Tx on	Yellow when the transmitter is on
Sync	Yellow when the DSSS demodulator and FEC decoder are synchronized

Digital Test Points

The test points are only accessible after opening the enclosure. They are intended to be used only for debugging purposes.

Test Point	Definition
TP1 PLL_LOCK	Tx RF frequency synthesizer lock status ('1' when locked)
TP2 DONE	FPGA configured ('1' when successfully configured)
TP3 PLL_LOCK	Rx RF frequency synthesizer lock status ('1' when locked)
TP4 RSSI	Received signal strength indicator. Practical range –70 to -5 dBm after LNA
J4.1	PRBS11 test sequence start of frame (once every 2047 bits). Compare with the BER tester detection at J4.11
J4.2	Turbo code encoder output SOF
J4.3	Modulator saturation
J4.4	Demod code lock
J4.5	Demod signal presence detected at FFT
J4.6	Demodulator recovered carrier/center frequency (coarse)
J4.7	Demod sync word detection
J4.8	Receiver sync word lock
J4.9	Received coded frame
J4.10	BER tester synchronized
J4.11	BER tester matched filter output (detects start of PRBS11 sequence)
J4.12	Byte error detected by BER tester

Operation

Power supply

This unit is designed for a +28V DC (18 – 36V) power supply. Power consumption depends somewhat on the configuration. Maximum power consumption: 350mA under 28V.
Power supply is through the front-panel connector.

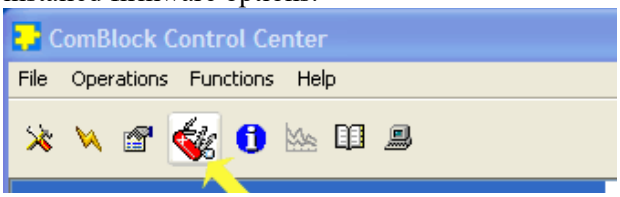
A lower supply voltage, down to 5.6V, can be used when the LNB supply output is unused.

Frequency reference

Depending on the firmware version loaded, the frequency reference is an external 10 MHz signal supplied through the front panel (**-B** firmware option) or an internal 19.2 MHz VC-TCXO (**-A** firmware option).
Both **-A** and **–B** firmware options are pre-loaded and can be switched easily.

Warning: when selected as external frequency reference, the 10 MHz frequency reference must be present prior to powering on the modem.

Click on the button below to switch between installed firmware options:



Output 10 MHz frequency reference

A 10 MHz frequency reference signal can be multiplexed with RF signals on the RF input (to an external LNB) and RF output (to an external BUC). The same 10 MHz is also available as an output on the front panel, labeled "10 MHz OUT". Each one of these three clocks signals can be enabled or disabled by software command.

Spreading codes

Spreading codes are pseudo random sequences which falls within the following categories:

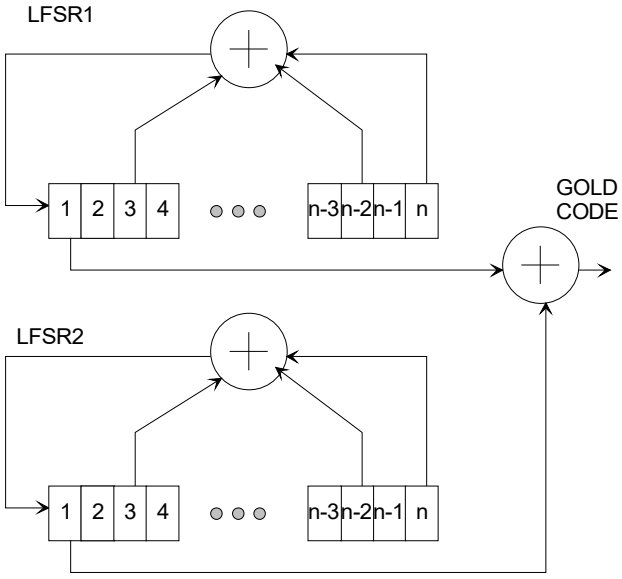
- Gold sequences, for best autocorrelation properties
- Maximal length sequences
- Barker codes (length 11, 13)
- GPS C/A codes.

The same spreading code is used on both the in-phase (I) and quadrature (Q) channels.

Limitation: short-length codes (< 127) may not lock at chip rates above 35 Mchips/s.

Gold sequences

Gold sequences are generated using two linear feedback shift registers LFSR1 and LFSR2 as illustrated below:



The code period is 2^n-1, where n is the number of taps in the shift register. The LFRSa are initialized to all 1's at the start of each period. The LFRSs will generate all possible n-bit combinations, except the all zeros combination.

Each sequence is uniquely described by its two generator polynominals. The highest order is n. The generator polynominals are user programmable.

A few commonly used Gold sequences are listed below:

n = 5 (length 31):
G1 = $1 + x^2 + x^5$ (0x000012)
G2 = $1 + x + x^2 + x^4 + x^5$ (0x00001B)

n = 6 (length 63):
G1 = $1 + x^5 + x^6$ (0x000030)
G2 = $1 + x + x^4 + x^5 + x^6$ (0x000039)

n = 7 (length 127):
G1 = $1 + x^3 + x^7$ (0x000044)
G2 = $1 + x + x^2 + x^3 + x^4 + x^5 + x^7$ (0x00005F)

n = 9 (length 511):
G1 = $1 + x^5 + x^9$ (0x000110)
G2 = $1 + x^3 + x^5 + x^6 + x^9$ (0x000134)

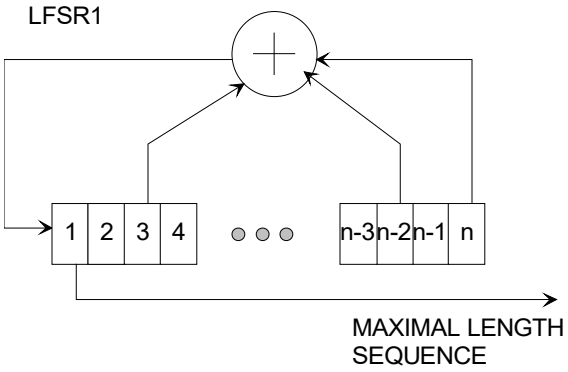
n = 10 (length 1023):
G1 = $1 + x^7 + x^{10}$ (0x000240)
G2 = $1 + x^2 + x^7 + x^8 + x^{10}$ (0x0002C2)

n = 11 (length 2047):
G1 = $1 + x^9 + x^{11}$ (0x000500)
G2 = $1 + x^3 + x^6 + x^9 + x^{11}$ (0x000524)

n = 17 (length 131071):
G1 = $1 + x^3 + x^6 + x^7 + x^9 + x^{10} + x^{14} + x^{16} + x^{17}$ (0x01A364)
G2 = $1 + x^9 + x^{13} + x^{14} + x^{17}$ (0x013100)

Maximal length sequences

Maximal length sequences are generated using one linear feedback shift register LFSR1 as shown below:



The code period is 2^n-1, where n is the number of taps in the shift register. The LFRSa are initialized to all 1's at the start of each period. The LFRSs will generate all possible n-bit combinations, except the all zeros combination.

Each sequence is uniquely described by its generator polynominal. The highest order is n. The generator polynominal is user programmable.

A few commonly used maximal length sequences are listed below:

n = 4 (length 15):
G1 = $1 + x + x^4$ (0x000009)
n = 5 (length 31):
G1 = $1 + x^2 + x^5$ (0x000012)
n = 6 (length 63):
G1 = $1 + x + x^6$ (0x000021)
n = 7 (length 127):
G1 = $1 + x + x^7$ (0x000041)
n = 8 (length 255):
G1 = $1 + x^2 + x^3 + x^4 + x^8$ (0x00008E)
n = 9 (length 511):
G1 = $1 + x^4 + x^9$ (0x000108)
n = 10 (length 1023):
G1 = $1 + x^3 + x^{10}$ (0x000204)

Barker Codes

11 bit Barker code: 101 1011 1000, or 0x5B8
13 bit Barker code: 1 1111 0011 0101, or 0x1F35

The length (11 or 13) must be entered as spreading factor in REG4/5.

GPS C/A Codes

GPS C/A codes are modified Gold codes of length 1023 with generator polynomials:
G1 = $1 + x^3 + x^{10}$
G2 = $1 + x^2 + x^3 + x^6 + x^8 + x^9 + x^{10}$

The G2 generator output is slightly modified so as to create a distinct code for each satellite. The G2 output is generated by summing two specific taps of the shift register. In the case of Satellite ID 1 for example, taps 2 and 6 are summed.

The G2 output taps are listed below:

Satellite ID / GPS PRN Signal Number	G2 output taps selection	Satellite ID / GPS PRN Signal Number	G2 output taps selection
1	2 xor 6	21	5 xor 8
2	3 xor 7	22	6 xor 9
3	4 xor 8	23	1 xor 3
4	5 xor 9	24	4 xor 6
5	1 xor 9	25	5 xor 7
6	2 xor 10	26	6 xor 8
7	1 xor 8	27	7 xor 9
8	2 xor 9	28	8 xor 10
9	3 xor 10	29	1 xor 6
10	2 xor 3	30	2 xor 7
11	3 xor 4	31	3 xor 8
12	5 xor 6	32	4 xor 9
13	6 xor 7	33	5 xor 10
14	7 xor 8	34	4 xor 10
15	8 xor 9	35	1 xor 7
16	9 xor 10	36	2 xor 8
17	1 xor 4	37	4 xor 10
18	2 xor 5		
19	3 xor 6		
20	4 xor 7		

Compliant with “Navstar GPS Space Segment / Navigation User Interfaces” specifications, ICD-GPS-200, Revision C. IRN-200C-004, 12 April 2000.

Symbol Rate

The symbol rate refers to the coded stream. The symbol rate is independent of the chip rate and code period. The demodulator includes an autonomous symbol tracking loop, separate from the code tracking loop.
However, the full spread-spectrum processing gain can only be achieved if the code period is greater than the symbol period.

Frequency acquisition & tracking

The demodulator comprises a phase locked loop (PLL) and FFT-based frequency acquisition circuit. Once the code is locked, the frequency acquisition circuit detects and corrects a maximum initial frequency error of +/- chip_rate / 256.

Once locked, the carrier tracking loops tracks the carrier phase over a very wide frequency range.

Note: the minimum practical symbol rate is such that (symbol_rate/200) > (chip_rate/(256*2048)). Reason: the Costas carrier tracking loop must be able to acquire any frequency error remaining after the initial frequency acquisition.

Demodulator acquisition time

Examples of acquisition times are given below:

PRBS-11 test sequence., BPSK, 6.914 Mchips/s, 192 Ksymbols/s, spreading factor 36
Code period 63, maximal length sequence, G1 = 0x39. E/No = 3.5dB (uncoded) or 4.5dB (coded)
Settings: signal amplitude: 1300, noise amplitude: 18432, calibrated using the spectrum analyzer.
Min: 28 ms
Max: 72 ms
Note: BERT shows bursts of errors approximately every 3s in the average (or 2.2E-3 BER)

PRBS-11 test sequence., BPSK, 345 Kchips/s, 15 Ksymbols/s, spreading factor 23
Code period 63, maximal length sequence, G1 = 0x30, 2.175 GHz, E/No = 3.6dB (uncoded) or 4.6dB (coded)
Min: 20 ms
Max: 920 ms

Modulation

BPSK or QPSK
The same spreading code is used on both I and Q channels.

Error Correction

Two error correction techniques are available, depending on the loaded firmware:

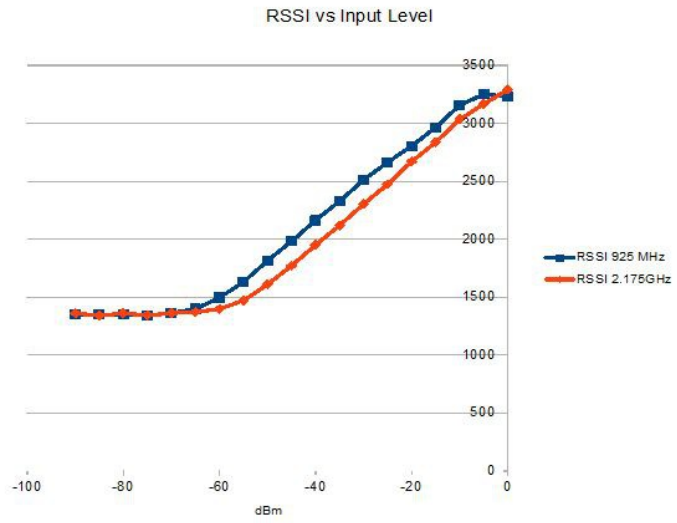
- Convolutional FEC K=7 rate ½, or
- Turbo Code

Check the GUI or status register SREG19(7: 4) to verify which codec is currently active.

The convolutional FEC is only available for rate ½ (one redundancy bit for each information bit), whereas the turbo code codec is flexible in its rate configuration.

RSSI

The RSSI measurements (as reported in status registers SREG5/6) versus the receiver input level is plotted below for the two extreme operational frequencies. The measurements are monotonous between -70 dBm and -5 dBm.



Note: RSSI measurement below –50Bm is affected by the presence of 10 MHz frequency reference when supplied to an external LNB (see control register REG46(2)).

Customization

The transceiver design can be customized to meet alternate customer requirements. The customizable features are

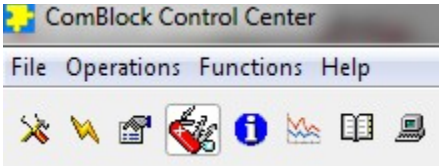
- Custom radio-frequency bands within 400 MHz– 3GHz at no extra charge.

Customization has to be specified and quoted at the time of order.

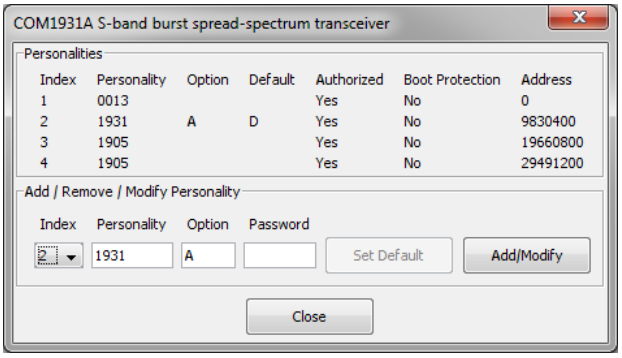
Load Software Updates

From time to time, ComBlock software updates are released.

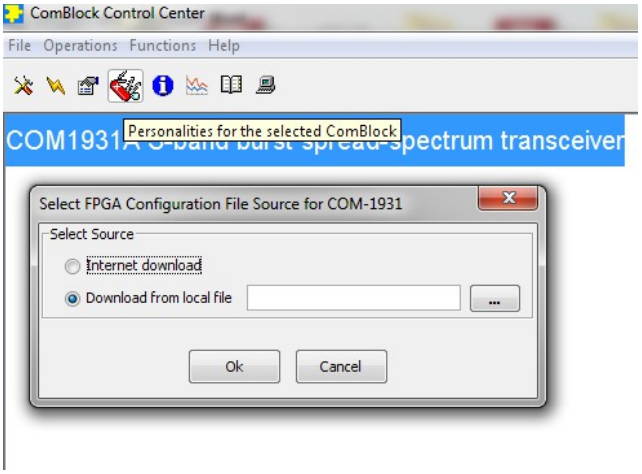
To manually update the software, highlight the ComBlock and click on the Swiss army knife button.



The receiver can store multiple personalities. The list of personalities stored within the ComBlock Flash memory will be shown upon clicking on the Swiss army knife button.



The default personality loaded at power up or after a reboot is identified by a 'D' in the Default column. Any unprotected personality can be updated while the Default personality is running. Select the personality index and click on the "Add/Modify" button.



The software configuration files are named with the .bit extension. The bit file can be downloaded via the Internet, from the ComBlock CD or any other local file.

The option and revision for the software currently running within the FPGA are listed at the bottom of the advanced settings window.

Two firmware options are available for this receiver:
-A firmware uses an internal VCTCXO frequency reference.
-B firmware option requires an external 10 MHz frequency reference.

Recovery

The toggle button under the backpanel can be used to

(a) prevent the FPGA configuration at power up. This can be useful if a bad FPGA configuration was loaded which resulted in loss of communication with the user.
(b) reset the LAN1 IP address to 172.16.1.128.

To prevent the FPGA configuration at power up, turn off power. Toggle the button. Turn on power, wait 1 second, then toggle the button a second time.

To reset the LAN1 IP address to a factory default of 172.16.1.128: Turn on power. Toggle the button, wait at least 30 seconds, during which time the red led blinks, then toggle the button a second time. Wait another 10 seconds, then cycle power off/on.

Interfaces

10/100/1000 Ethernet LAN for data, monitoring and control	Two RJ45 connectors Supports auto MDIX to alleviate the need for crossover cable. LAN1 is for monitoring and control only LAN2 is for IP routing
10 MHz frequency reference input	10 MHz frequency reference input for frequency synthesis. Sinewave, clipped sinewave or squarewave. SMA female connector Input is AC coupled. Minimum level 0.6Vpp. Maximum level: 3.3Vpp.
10 MHz frequency reference output	10 MHz frequency reference output generated either from the 10 MHz frequency reference input (**-B** firmware option) or from the internal TCXO (**-A** firmware option)
RF Rx	Receiver input. 50 Ohm, SMA female connector. Operating range: -60 to -10 dBm Maximum no damage input level: + 20 dBm Two other signals can be multiplexed onto the same coaxial connection between the COM-1918 transceiver and an external LNB: • 10 MHz frequency reference (software enabled) Level: -2 dBm typ. • 13/18V supply (software enabled)
RF Tx	Transmitter output. 50 Ohm, SMA female connector. Transmit level: -30 to 0 dBm, user selectable. One other signal can be multiplexed onto the same coaxial connection between the COM-1918 transceiver and an external BUC: • 10 MHz frequency reference (software enabled) Level: 0 dBm typ.

Operating input voltage range

Supply voltage	+18V min, +36V max 350mA typ. under +28VDC
Supply voltage (when no LNB 13/18V supply needed)	+5.6V min, +36V max

The positive voltage is on the center pin, the ground on the outer barrel.

Absolute maximum ratings

Supply voltage	+45 V max
RF input	+20dBm max

Mechanical Interface

Aluminum enclosure with rubberized end caps.
L x W x H: 168.5mm x 138.96 mm x 40.98 mm.
Includes two optional 40mm mounting flanges for mounting to a flat support plate.

Schematics

The board schematics are available on-line at
http://comblock.com/download/com_1900schematics.pdf

Configuration Management

This specification is to be used in conjunction with:

ComBlock control center revision 3.12j and above.

ARM processor firmware version:
CB1900_1_6.hex 5/4/16

FPGA/VHDL version:
COM-1918_002d 10/3/16

It is possible to read back the option and version of the FPGA configuration currently active. Using the ComBlock Control Center, highlight the COM-1918 module, then go to the advanced settings. The option and version are listed at the bottom of the configuration panel.

Troubleshooting Checklist

Excessive power consumption:

- The receiver input is capable of supplying 13/18V DC to an external LNB. When using RF attenuators at the input in a RF loopback

test, please make sure to use a DC block between the RFin and the attenuator.

Demodulator can't achieve lock even at high signal-to-noise ratios:

- Make sure the modulator baseband I/Q signals do not saturate, as such saturation would strongly distort the modulation phase information. (this is a phase demodulator!)

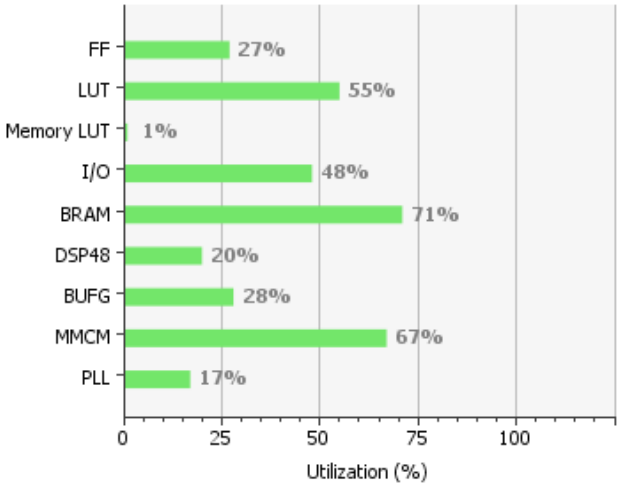
IP router does not forward IP frames to the WAN (Tx led not blinking):

- Make sure the sending PC has declared the LAN/IP2 address as "gateway"
- Verify that the modulator is configured in "IP router WAN interface" and is not in test mode.

VHDL code / IP core

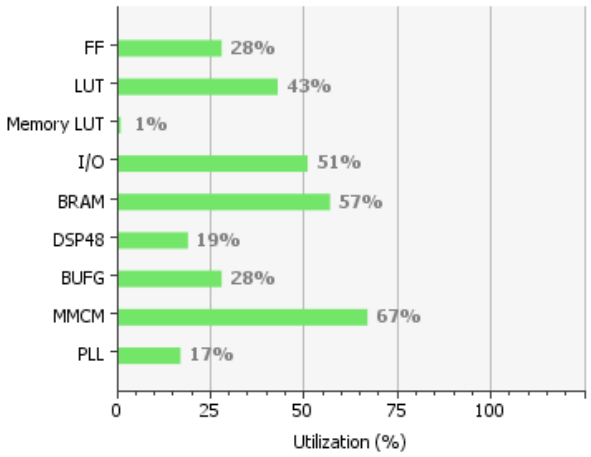
The FPGA code is written in VHDL. It does not use any third-party software. It occupies the following FPGA resources:

TC codec case:



Resource	Utilization	Available	Utilization %
FF	33972	126800	26.79
LUT	35150	63400	55.44
Memory LUT	110	19000	0.58
I/O	137	285	48.07
BRAM	95.5	135	70.74
DSP48	48	240	20.00
BUFG	9	32	28.12
MMCM	4	6	66.67
PLL	1	6	16.67

Convolutional codec case:



Resource	Utilization	Available	Utilization %
FF	35129	126800	27.70
LUT	27310	63400	43.08
Memory LUT	98	19000	0.52
I/O	146	285	51.23
BRAM	77	135	57.04
DSP48	46	240	19.17
BUFG	9	32	28.12
MMCM	4	6	66.67
PLL	1	6	16.67

The maximum chip rate is limited by

- the FPGA technology. For example nearly 80 Mchips/s for Xilinx Artix 7 –1 speed (XC7A100T-1)
- the receiver IF band-pass filter (40 MHz bandwidth)

The IP core, which includes all VHDL source code, can be purchased separately. It is not needed to operate the ready-to-use COM-1918 transceiver. See http://www.comblock.com/download/com1818soft.pdf

ComBlock Ordering Information

COM-1918 L/S-band continuous-mode spread-spectrum transceiver

ECCN: 5A001.b.3

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