COM-2001
DIGITAL-TO-ANALOG CONVERSION
(I & Q COMPLEX BASEBAND)

Key Features

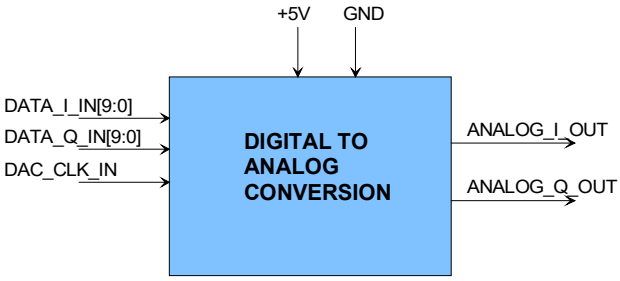
- Converts the complex baseband digital signal to two analog baseband signals.
- Dual 125 Msamples/s 10-bit D/A converters.
- 6-pole Butterworth clock rejection filters Maximum bandwidth: +/- 13 MHz @±0.4dB ripple.
- A/D clock rejection @40 MHz > 84 dBc.
- Output voltage: 1Vpp with 0.85V DC bias.
- Single 5V supply
- Connectorized 3"x 3" module for ease of prototyping.
- Analog: SMA connectors
- Digital: standard 40 pin 2mm dual row connectors (left)

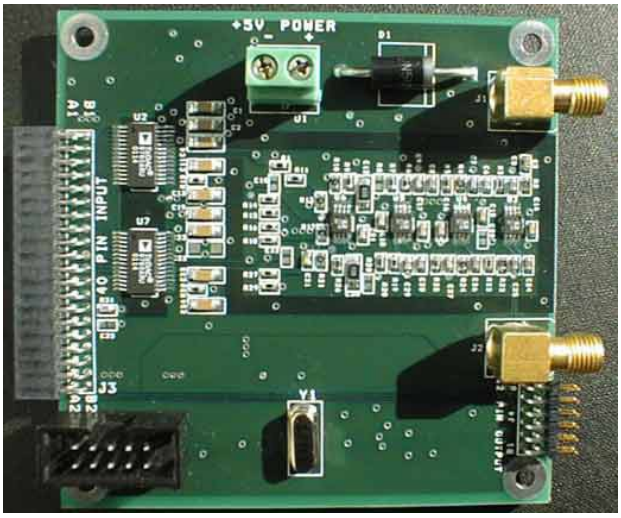
For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com2001.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .

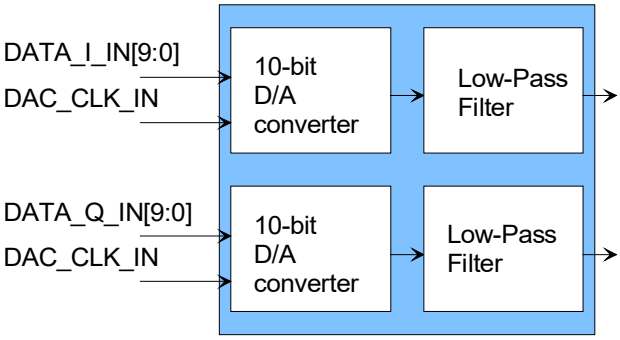
Electrical Interface

Inputs / Outputs





Block Diagram



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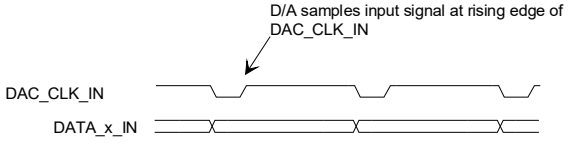
Input Module Interface	Definition
DATA_I_IN[9:0]	Modulated input signal, digital, baseband, real axis. 10-bit unsigned format. 0x000 for maximum output level 0x3FF for minimum output level 0x1FF or 0x200 for near center level. This data word is read at the rising edge of DAC_CLK_IN, and ignored at all other times.
DATA_Q_IN[9:0]	Modulated input signal, digital, baseband imaginary axis. Same format as DATA_I_IN.
DAC_CLK_IN	Input signal sampling clock. The input samples are stable at the rising edge of DAC_CLK_IN. Maximum sampling rate is 125 MHz.
Analog Output Signals	**Definition**
ANALOG_I_OUT	Analog output, baseband, real-axis. Peak amplitude: 1.0Vpp DC bias: 0.85V. SMA female connector.
ANALOG_Q_OUT	Analog output, baseband, imaginary-axis. Peak amplitude: 1.0Vpp DC bias: 0.85V. SMA female connector.
Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is 120mA.

Timing

The input signals DATA_x_IN are read at the rising edge of the DAC_CLK_IN sampling clock on pin A13 of the J3 connector. The maximum sampling clock frequency is 125 MHz.

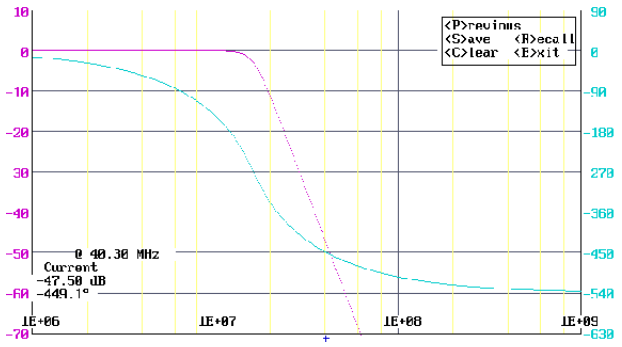
Input



Performance

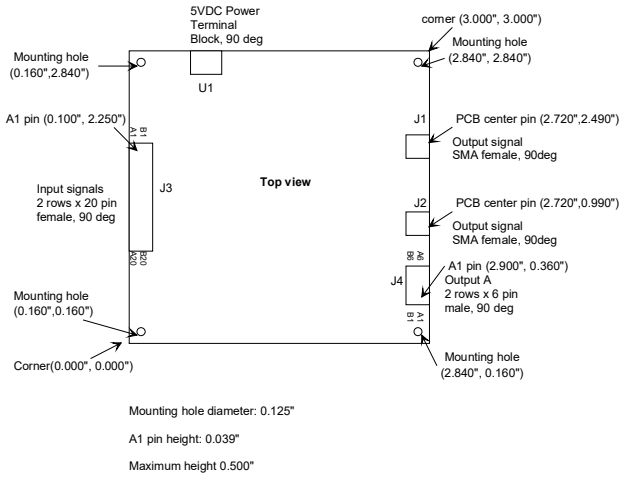
Low Pass Filter

Each D/A converter is followed by a 6-pole Butterworth low-pass filter to suppress harmonics. The filter response is as follows:



Out of band spectral spurious lines: < -84dBc in any 3 KHz band.

Mechanical Interface



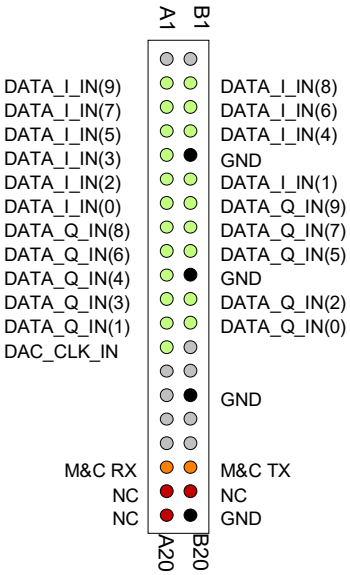
Mounting hole diameter: 0.125"

A1 pin height: 0.039"

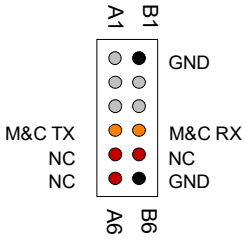
Maximum height 0.500"

Pinout

Input Connector J3



Output Connector J4



This connector is to forward JTAG, GND and other monitoring and control signals to subsequent analog modules.

I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-1002 BPSK/QPSK/OQPSK Modulator	COM-4001/2/3/5/6/7 RF Quadrature Modulators
COM-1012/1019 DSSS Modulator	
COM-1028 FSK/MSK/GFSK/GMSK Modulator	
COM-8001 Arbitrary Waveform Generator	

ComBlock Ordering Information

COM-2001
DIGITAL TO ANALOG CONVERSION, BASEBAND

ECCN: 3A001.a.5.a

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