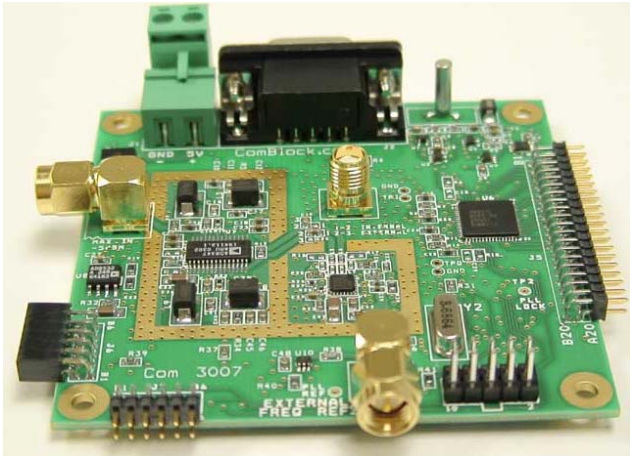
COM-3007
[2.3 – 2.8 GHz] RECEIVER

Key Features

- [2.3 – 2.8 GHz] receiver[1], software selectable. Designed for use in the 2.3GHz SDARS band, in the 2.4 GHz unlicensed band and in the Multichannel Multipoint Distribution Service (MMDS) band.
- Sensitivity: -51 dBm RF input for full scale 10-bit output samples.
- Built-in RF AGC, 70 dB dynamic range.
- Low-noise frequency synthesizer can be tuned over entire range by steps of 1 MHz, 200 KHz or 100 KHz.
- 8 preset frequencies for fast (<6ms) local oscillator frequency tuning.
- Automatic selection of internal / external 10 MHz frequency reference for the frequency synthesizer.
- Optional operation over extended frequency range [800 MHz – 2.8 GHz] by suppling an externally-generated RF carrier for frequency downconversion via SMA connector.
- True PLL: multiple COM-3007s can be phase locked onto the same external 10 MHz frequency reference. The LO phase difference among the multiple modules is fixed at power-up.
- Dual 10-bit Analog-to-Digital converters.
- User-selectable variable (105 Msamples/s max) ADC sampling rate when using external clock or fixed 40 Msamples/s internal clock.
- Multiple receivers can be synchronized in terms of (a) the ADC sampling rate, and (b) the synthesized RF carrier phase by using external frequency references:
    - External ADC sampling clock
    - External 10 MHz RF frequency synthesizer PLL reference.
- Two baseband filtering options:
    - Narrow-band applications (<300 KHz)
    - Wideband applications (< 26 MHz).
- SMA connectors. Single 5V supply. Connectorized 3”x 3” module for ease of prototyping.



(shown without shield)

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com3007.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .

[1] Also able to tune in the 1150-1400 MHz range.

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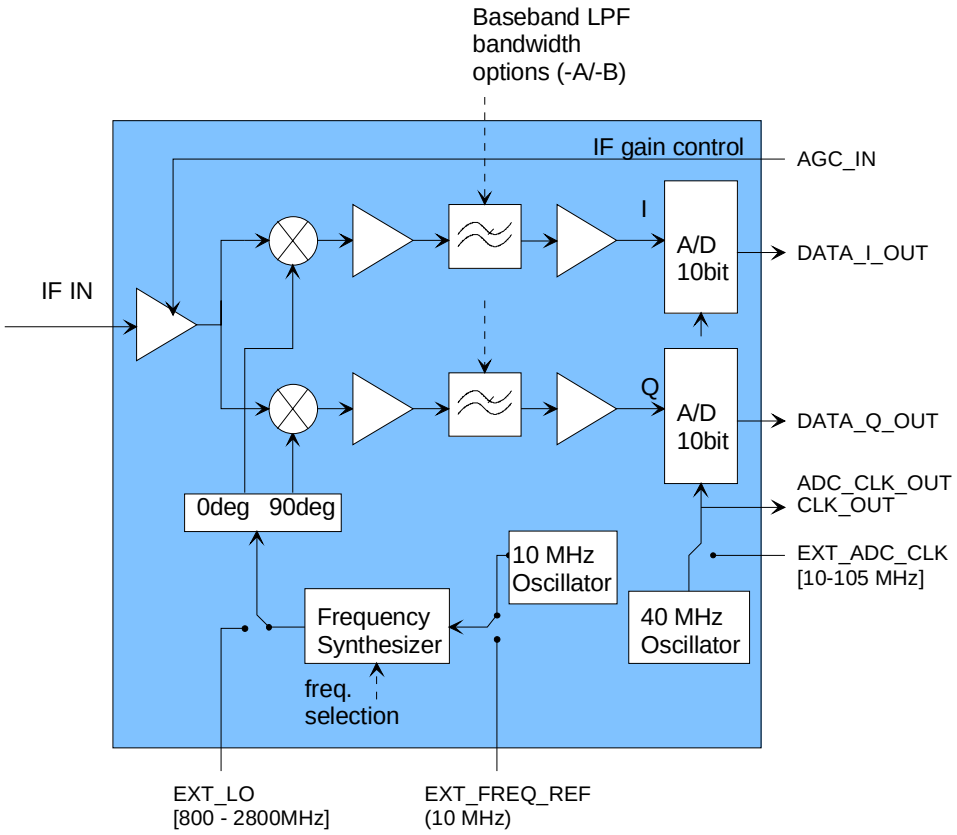


Electrical Interface

Inputs / Outputs

Inputs	Definition
RF_IN	2.3 – 2.8 GHz [2]when using the internal frequency synthesizer or 0.8 – 2.8 GHz when using an externally-generated RF carrier for frequency downconversion. J3 SMA male connector. 50 Ohm impedance. Receiver sensitivity: -51 dBm at RF input for full scale signal at A/D converter. Maximum input (operating): -5 dBm Maximum input (no damage): +10 dBm AGC range: 70 dB.
EXT_FREQ_REF	Optional input. External 10 MHz frequency reference for frequency synthesis. Sinewave, clipped sinewave or squarewave. J8 SMA male connector. 50 Ohm. Minimum level: 2Vpp. Maximum level: 3.3Vpp.
EXT_ADC_CLK	Optional input. Externally supplied Analog-to-Digital converter sampling clock. Enabled or disabled by software control. LVTTL 0 – 3.3V. Selecting sampling rates less than half the baseband filter bandwidth may result in aliasing. Supply this clock at J4/A14. Sampling frequency: Min: 10 Msamples/s Max: 105 Msamples/s
EXT_LO	Optional input. Externally generated RF carrier for frequency down-conversion, thus bypassing the internal frequency synthesizer. Enabled or disabled by moving two SMT capacitors soldered on the board. AC coupled, 50 Ohm impedance. Input level: 0 dBm max, -10 dB min.
Digital Output Signals	**Definition**
DATA_I_OUT[9:0]	In-phase baseband signal. 10-bit digital samples.

[2] Also able to tune in the 1150-1400 MHz range.

	Unsigned. See timing diagram.
DATA_Q_OUT[9:0]	Quadrature baseband signal. Same characteristics as above.
CLK_OUT	Analog-to-digital converter sampling clock. 40 Msamples/s if internal selection, otherwise EXT_ADC_CLK's frequency. Read the samples at the rising edge of CLK_OUT.
AGC_IN	Input signal to control the analog gain prior to A/D conversion. Can be digital (pulse-width modulated) or analog. The purpose is to use the maximum dynamic range while preventing saturation at the A/D converter. 0 is the maximum gain, +3V is the minimum gain. Without any subsequent module, the COM-3007's gain is set at its maximum and may thus saturate. See the AGC section for more details.
Control Lines	**Definition**
PLL_STROBE	Low-voltage (3.3V / 0V) TTL input control. Used to increment the modulo- N_{freq} frequency pointer (where N_{freq} is defined in Register 35) in a round-robin sequence. Rising edge triggered. Minimum pulse width: 10 µsec. Connector J6 Pin A3.
Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is 250mA typ.

Important: digital I/O signals are 0-3.3V LVTTL. Inputs are NOT 5V tolerant!

Configuration

Complete assemblies can be monitored and controlled centrally over a single asynchronous serial connection or, when available through adjacent ComBlocks, LAN/TCP-IP , USB, or CardBus connection.

The module configuration is stored in non-volatile memory.

Configuration (Basic)

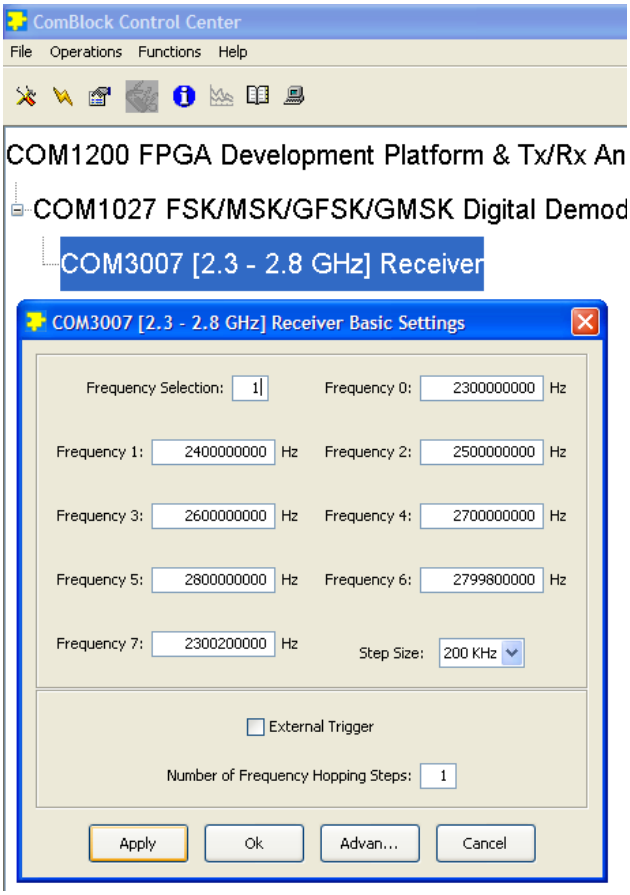
The easiest way to configure the COM-3007 is to use the ComBlock Control Center software supplied with the module(s). After detecting the ComBlock modules (2nd button from left), highlight the COM-3007 module to be configured. Then press the settings button (3rd button from the left).

Up to eight frequencies can be stored within each module at any given time. The current frequency is selected by an index in the range 0 to 7. Frequencies must be integer multiples of the RF synthesizer step size.

A basic frequency hopping scheme can be enabled by

(a) enabling the external trigger
(b) entering the number of frequency hopping steps in the round-robin arrangement.

For example, by specifying 4 steps, the receiver center frequency will follow the following index sequence: 0,1,2,3,0,1,2,3,0,1, etc., the index being incremented at the rising edge of each external PLL_STROBE pulse.



Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write.

Undefined control registers or register bits are for backward software compatibility and/or future use. They are ignored in the current firmware version.

Programmers developing custom applications (using the ComBlock API instead of the supplied ComBlock control center graphical user interface) should know that frequency changes are enacted upon (re-)writing to the last register (REG35).

Parameters	Configuration
RF frequency 0	Preselected frequency 0. Range 2.3GHz to 2.8GHz and 1.15 to 1.4 GHz, by steps 1 MHz, 200 KHz or 100 KHz, expressed in Hz. REG0: bit 7:0 (LSB) REG1: bit 15:8
	REG2: bit 23:16 REG3: bit 31:24 (MSB)
External/Internal RF carrier generation	Enable or disable the RF frequency synthesizer. 0 = internal RF carrier generation. 1 = external. An unmodulated RF signal must be supplied, the frequency of which determines the receiver center frequency. The RF frequency settings are thus ignored. REG5: bit 7
External controls enabled/disabled	Enable or disable the PLL_STROBE external control on the J6 connector. 0 = external control disabled 1 = external control enabled REG6: bit 1
External/Internal ADC sampling clock	Select the external ADC sampling clock EXT_ADC_CLK or the internal 40 MHz sampling clock. Selecting sampling rates less than half the baseband filter bandwidth may result in aliasing. 0 = internal 40 MHz ADC clock 1 = external ADC clock. REG6 bit 2
Step size selection	Chose the RF frequency synthesizer step size. The selected RF frequency must be an integer multiple of the step size. 200 KHz is recommended for best overall phase noise performance. 00 = 1 MHz step 01 = 200 KHz step 10 = 100 KHz step 11 = undefined REG6 bits 4-3.
Frequency selection	Use to switch local oscillator frequency among preselected values. Range 0 through 7 REG6 bits 7-5.
RF frequency 1	Preselected frequency 1. Same format as RF frequency 0. REG7: bit 7:0 (LSB) REG8: bit 15:8 REG9: bit 23:16 REG10: bit 31:24 (MSB)
RF frequency 2	Preselected frequency 2. Same format as RF frequency 0. REG11: bit 7:0 (LSB) REG12: bit 15:8 REG13: bit 23:16 REG14: bit 31:24 (MSB)
RF frequency 3	Preselected frequency 3. Same format as RF frequency 0. REG15: bit 7:0 (LSB) REG16: bit 15:8 REG17: bit 23:16

	REG18: bit 31:24 (MSB)
RF frequency 4	Preselected frequency 4. Same format as RF frequency 0. REG19: bit 7:0 (LSB) REG20: bit 15:8 REG21: bit 23:16 REG22: bit 31:24 (MSB)
RF frequency 5	Preselected frequency 5. Same format as RF frequency 0. REG23: bit 7:0 (LSB) REG24: bit 15:8 REG25: bit 23:16 REG26: bit 31:24 (MSB)
RF frequency 6	Preselected frequency 6. Same format as RF frequency 0. REG27: bit 7:0 (LSB) REG28: bit 15:8 REG29: bit 23:16 REG30: bit 31:24 (MSB)
RF frequency 7	Preselected frequency 7. Same format as RF frequency 0. REG31: bit 7:0 (LSB) REG32: bit 15:8 REG33: bit 23:16 REG34: bit 31:24 (MSB)
Number of RF frequencies N_{freq} in the scanning list	Each time a PLL_STROBE pulse is received, the frequency pointer increments modulo N_{freq}. N_{freq} is in the range 1 – 8. REG35: bit 7:0.

Note: Fine frequency tuning (down to Hz precision) is typically implemented digitally at the demodulator. See demodulators specifications (COM-1001, COM-1011/1018, COM-1027, COM-1008 etc) for details.

Monitoring

Parameters	Monitoring
PLL lock status (PLL_LOCK)	Indicates the RF synthesizer lock status: locked to the frequency reference (1) or unlocked (0). SREG0 bit 0

Test Points

Test points are provided for easy access by an oscilloscope probe.

Test Point	Definition
TPI	Baseband signal, I-channel, at A/D converter input. The nominal amplitude is 1Vpp when the AGC loop is closed with the following demodulators (COM-1001, COM-1011/1018, COM-1027, COM-1008 or equivalent).
TPQ	Baseband signal, Q-channel, at A/D converter input. Same type as above.
PLL_LOCK	Frequency synthesizer PLL lock status. Active low: '1' when locked. This information is also available in status register SREG0
PLL_REF	Internal / External reference clock Note: do not connect any permanent test cable to this test point as it is likely to cause a significant degradation in phase noise performance.

Operations

Internal vs External frequency reference for frequency synthesizer

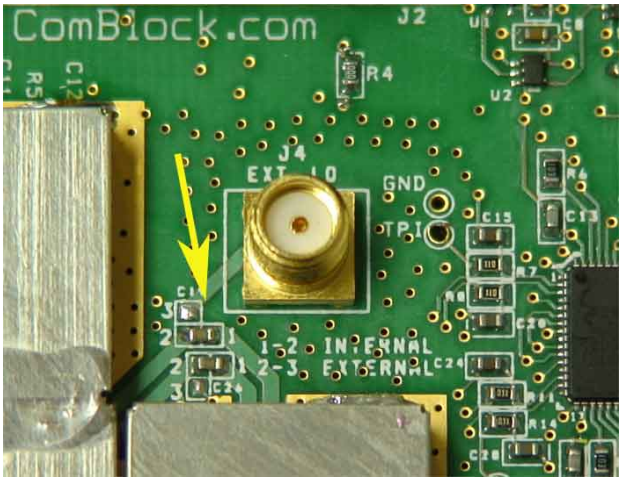
An external 10 MHz frequency reference can be used when the user application requires high frequency stability. In this case, simply connect a 10 MHz sinewave, clipped sinewave or square wave to the J8 EXTERNAL FREQ REF SMA connector. Detection is automatic, thus no configuration change is needed. Upon removal of the external 10 MHz frequency reference signal, the COM-3007 reverts to the internal frequency reference.

Internal vs External ADC sampling clock

The source for the Analog to Digital converter clock can be selected to be internal (fixed 40 Msamples/s) or external (105 Msamples/s max, 10 Msamples min) by software command. The external clock EXT_ADC_CLK is to be supplied at J4/A14.

External RF carrier

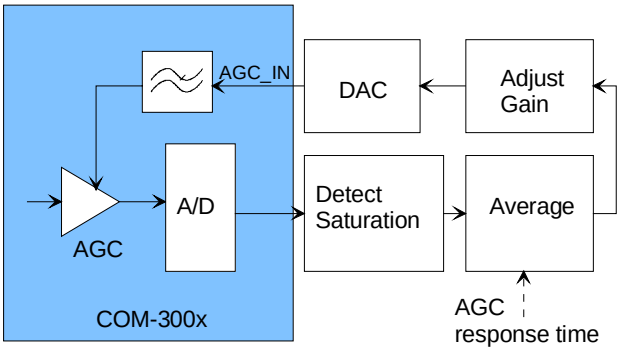
Operation over extended frequency range [700 MHz – 2.8 GHz] is possible by suppling an externally-generated RF carrier for frequency upconversion via the J4 EXT LO SMA connector. This configuration is <u>not</u> software configurable: the RF carrier path is altered by moving the C19 and C26 capacitors 90 degrees from the 1-2 position to the 2-3 position as illustrated below:



In order to minimize noise when an external RF carrier is used, it is recommended to switch off the built-in RF frequency synthesizer by software (see control register REG5, bit 7).

AGC

The default Automatic Gain Control (AGC) mechanism assumes than an external circuit (a demodulator for example) detects saturation conditions at the Analog-to-Digital converter and adjusts the receiver gain AGC_IN accordingly, as illustrated below:



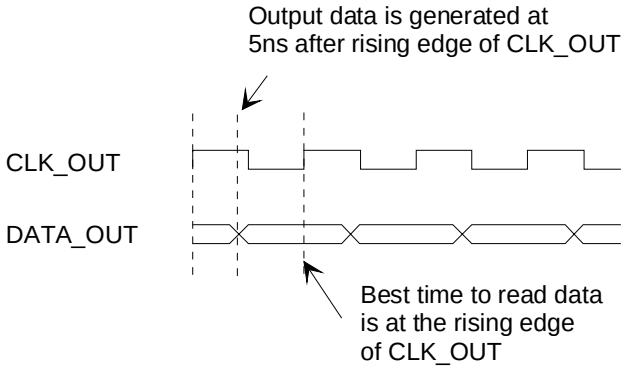
AGC principle

The AGC_IN signal can be a simple pulse-width modulated (PWM) digital signal or an analog signal from a DAC. The AGC_IN signal undergoes low-pass filtering within the COM-3007 in order to average out a PWM control signal. By default, the AGC response time is limited to approximately 1 second by the two RC low-pass filters where R = 100KΩ and C = 1µF.

Where applications require faster AGC response time, a few µseconds in the case of burst receivers for example, the RC low-pass filter bandwidth can be greatly increased by changing two resistors and/or capacitors. The COM-3007 AGC response time can be specified at the time of order.

Timing

Timing for the digital samples is illustrated below. The user should read the digital samples at the rising edge of CLK_OUT.



Schematics

The schematics are available on the ComBlock CD shipped with every module.

Performance

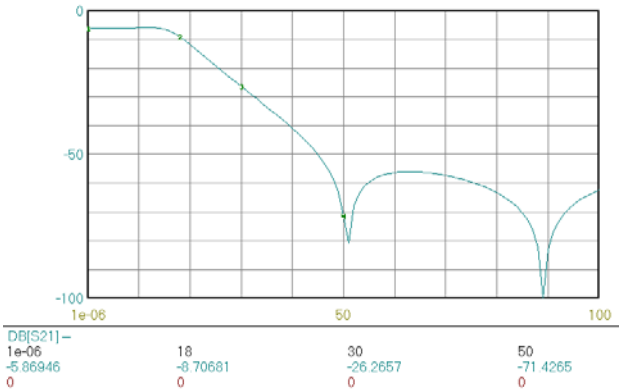
Internal Clock Reference

The internal crystal performance is as follows:

- tolerance: [-10 to +30] ppm max @25C
- temperature stability (-10C to +60C): ± 50 ppm max
- aging: ±5ppm/year max (1st year) @25C

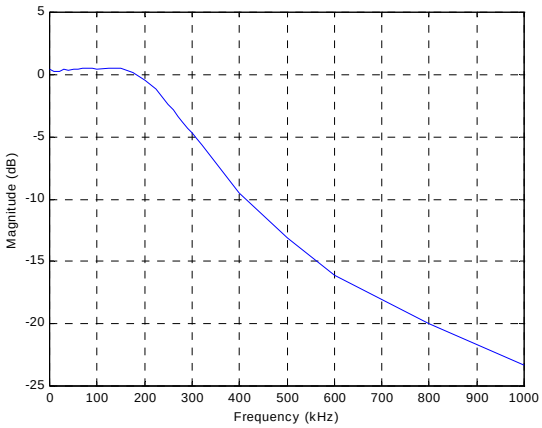
Low Pass Filter

Each A/D converter is preceeded by a 4th order elliptic low-pass filter. The 3 dB cutoff frequency for model COM-3007-B (wideband applications) is 20 MHz.



COM-3007-B baseband low-pass filter frequency response. Span 100 MHz, 10dB/div.

The 3 dB cutoff frequency for model COM-3007-A (narrow band applications) is 265 KHz. In-band ripple within +/- 150 KHz is less than +/- 0.1 dB.



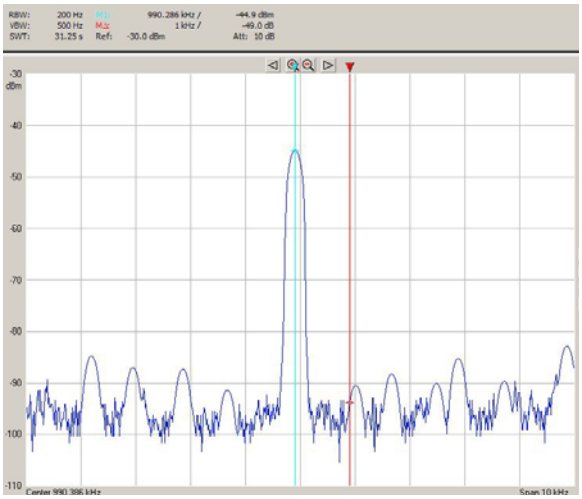
COM-3007-A baseband low-pass filter frequency response. Span 1 MHz, 5dB/div.

Custom low-pass filters can be designed upon request for bandwidths up to 65 MHz.

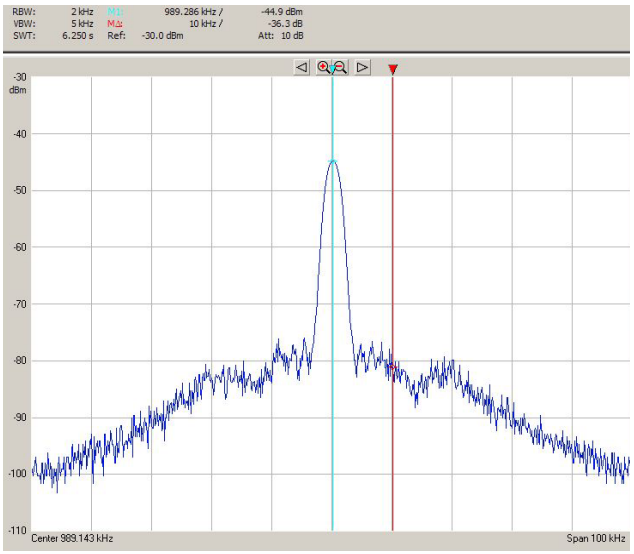
A 4 Hz high-pass filter is used to block the DC bias caused by LO leakage through the input connector.

Phase noise

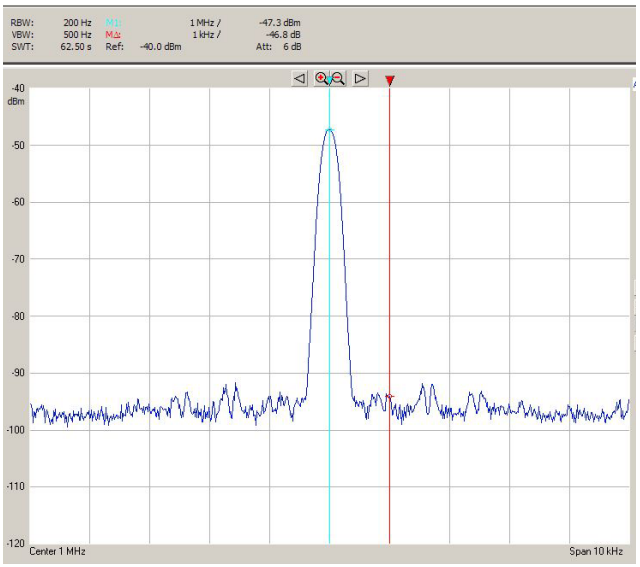
Typical phase noise performances are:
-71 dBc @1 KHz away from the carrier
-67 dBc @10 KHz
-92 dBc @ 100 KHz



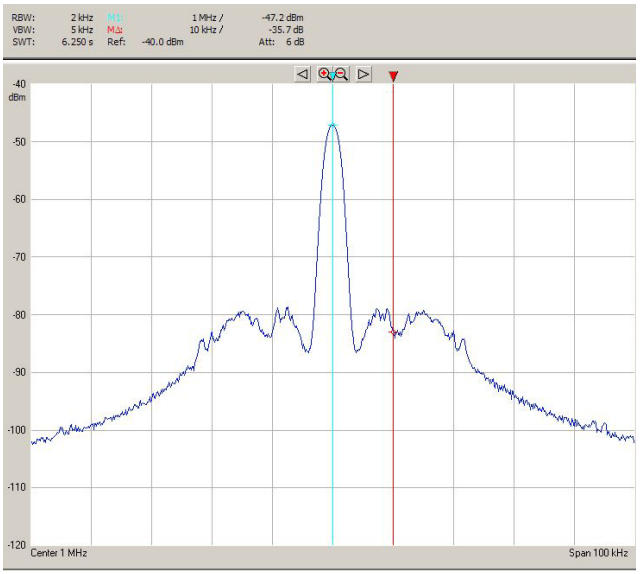
Phase noise @ 2.3 GHz, 200 KHz RF synthesizer step size, minimum input power, internal frequency reference. (includes impairements from adjacent digital demodulator).
10 KHz span, 200 Hz resolution bandwidth.



Phase noise @ 2.3 GHz, 200 KHz RF synthesizer step size, minimum input power, internal frequency reference. (includes impairements from adjacent digital demodulator).
100 KHz span, 2 KHz resolution bandwidth.

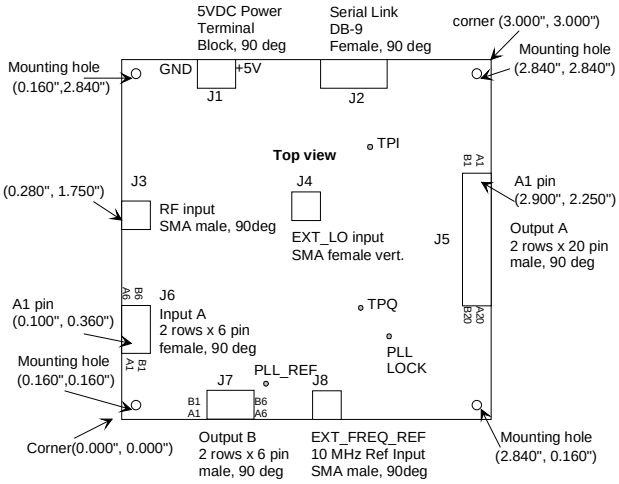


Phase noise @ 2.8 GHz, 200 KHz RF synthesizer step size, minimum input power, external frequency reference. (includes impairements from adjacent digital demodulator).
10 KHz span, 200 Hz resolution bandwidth.



Phase noise @ 2.8 GHz, 200 KHz RF synthesizer step size, minimum input power, external frequency reference. (includes impairements from adjacent digital demodulator).
100 KHz span, 2 KHz resolution bandwidth.

Mechanical Interface



Mounting hole diameter: 0.125"

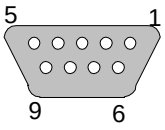
A1 pin height: 0.039"

Maximum height 0.500"

Pinout

Serial Link J2

The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.

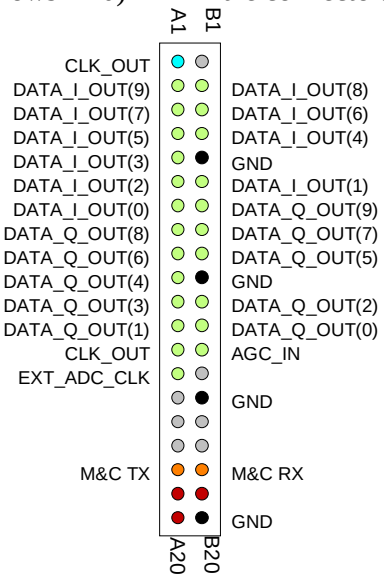


DB-9 Female

2 Transmit
3 Receive
5 Ground

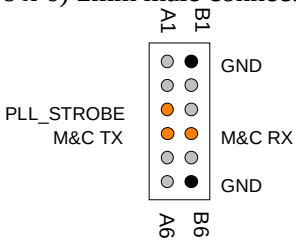
Output Connector J5

40-pin (2 rows x 20) 2mm male connector.



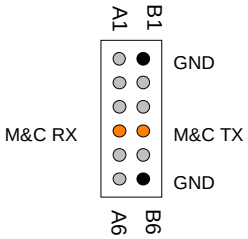
M&C Connector J7

12-pin (2 rows x 6) 2mm male connector.



M&C Connector J6

12-pin (2 rows x 6) 2mm female connector.



I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-4102 2.4 GHz transceiver, 25 dBm power / 3.5 dB noise figure.	COM-1008 Variable decimation
	COM-1001 BPSK/QPSK/OQPSK demodulator
	COM-1011/1018 Direct-sequence spread-spectrum demodulator
	COM-1027 FSK/MSK/GFSK/GMSK demodulator
	COM-8002 High-speed data acquisition. 256MB, 1Gbit/s, 50 Msamples/s.
	COM-2001 Dual D/A converter (baseband)

Configuration Management

This specification is to be used in conjunction with Atmel microcontroller software revision 4.

ComBlock Ordering Information

COM-3007-A [2.3 – 2.8 GHz] Receiver. Narrow-band Applications.

COM-3007-B [2.3 – 2.8 GHz] Receiver. Wideband Applications.

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