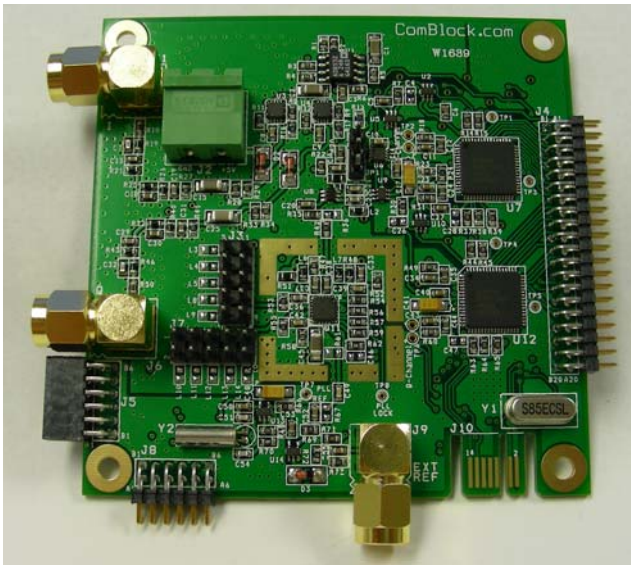
COM-3008/3009
DUAL ANALOG-TO-DIGITAL CONVERSION

Key Features

- COM-3008: 210 MSamples/s dual 10-bit
  COM-3009: 130 MSamples/s dual 12-bit
- Built-in 24 dB gain control to increase the effective ADC dynamic range.
- Sensitivity: -26 dBm / 31mVpp minimum input level for full scale output samples.
- Input bandwidth: 200 MHz
- Sampling rate is user-selectable in the range from 40 to 210 Msamples/s.
- Sampling clock can be:
  - External
  - Programmable locked onto an internal frequency reference.
  - Programmable locked onto an external (ultra-stable) frequency reference.
- Multiple receivers can be synchronized in terms of the ADC sampling rate by using external frequency references.
- One of several anti-aliasing filter bandwidth options –B can be selected at the time of ordering:
  - 50 MHz bandpass (default)
  - no filtering (for flexible IF undersampling)
  - custom 70 MHz or 140 MHz centered filters.
- SMA connectors. Single 5V supply. Connectorized 3”x 3” module for ease of prototyping.



For the latest data sheet, please refer to the **ComBlock** web site: http://www.comblock.com/download/com3008.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .

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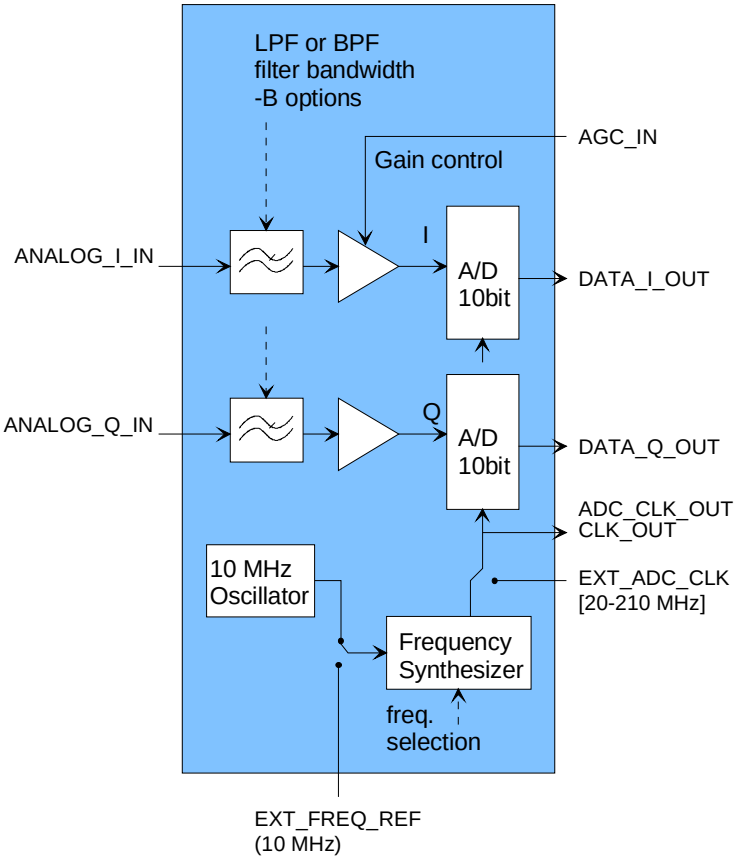


Electrical Interface

Inputs / Outputs

Inputs	Definition
ANALOG_I_IN ANALOG_Q_IN	0 – 200 MHz bandwidth. Receiver sensitivity: 63mVpp at input for full scale signal at A/D converter when AGC_IN = 0V (maximum gain). Maximum input (operating): 1Vpp when AGC_IN = 3.3V (minimum gain). Maximum input (no damage): 3.6Vpp A DC block with a 20 Hz (-3dB) cutoff frequency is installed by default. It can be removed upon request at the time of order (Option – A), in which case the common mode voltage is 2.25V. SMA male connectors.50Ohm impedance.
EXT_FREQ_REF	Optional input. External 10 MHz frequency reference for frequency synthesis. Sinewave, clipped sinewave or squarewave. J8 SMA male connector. 50 Ohm. Minimum level: 2Vpp. Maximum level: 3.3Vpp.
EXT_ADC_CLK	Optional input. Externally supplied Analog-to-Digital converter sampling clock (when DDR is enabled) or double frequency ADC sampling clock (when DDR is disabled). Enabled or disabled by jumper JP1 selection. LVTTL 0 – 3.3V. Selecting sampling rates less than half the baseband filter bandwidth may result in aliasing. Supply this clock at J4/A14. Sampling frequency: Min: 20 MHz Max: 210 MHz
Digital Output Signals	**Definition**
DATA1_OUT[9:0] DATA2_OUT[9:0]	10-bit digital samples. Unsigned format: 0x200 represents a zero, 0x000 the most negative signal, 0x3FF the most positive signal. At lower sampling rates, DATA1_OUT conveys the In-phase samples while DATA2_OUT conveys the Quadrature samples.

	At higher sampling rates a dual data rate (DDR) interface is used and the in-phase and quadrature samples are interlaced. See timing diagram for details.
CLK_OUT	Analog-to-digital converter sampling clock. 40 Msamples/s if internal selection, otherwise EXT_ADC_CLK's frequency. Read the samples at the rising edge of CLK_OUT.
AGC_IN	Input signal to control the analog gain prior to A/D conversion. Can be digital (pulse-width modulated) or analog. The purpose is to use the maximum dynamic range while preventing saturation at the A/D converter. 0 is the maximum gain, +3V is the minimum gain. Without any subsequent module, the COM-3008's gain is set at its maximum and may thus saturate. See the AGC section for more details.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is 500mA typ. when sampling at the maximum rate of 210 MSamples/s.

Absolute Maximum Ratings

Supply voltage	-60V min, +6.6V max
Digital inputs, EXT_FREQ_REF **Important: Digital I/O signals are 0-3.3V LVTTL. Inputs are NOT 5V tolerant!**	-0.5V min, +3.6V max

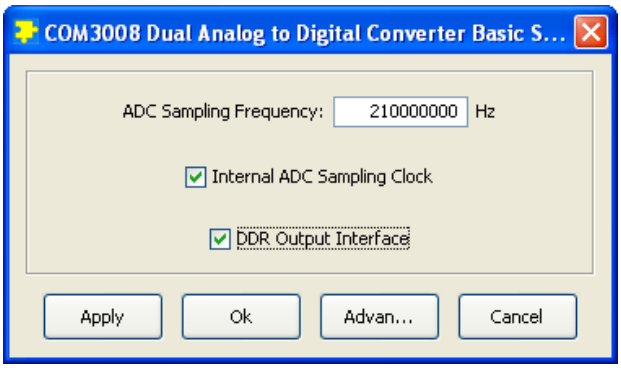
Configuration

Complete assemblies can be monitored and controlled centrally through adjacent ComBlocks' asynchronous serial, LAN/TCP-IP , USB, or CardBus connection.

The module configuration is stored in non-volatile memory.

Configuration (Basic)

The easiest way to configure the COM-3008 is to use the ComBlock Control Center software supplied with the module. After detecting the ComBlock modules (2nd button from left), highlight the COM-3008 module to be configured. Then press the settings button (3rd button from the left).



Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write.

Undefined control registers or register bits are for backward software compatibility and/or future use. They are ignored in the current firmware version.

Programmers developing custom applications (using the ComBlock API instead of the supplied ComBlock control center graphical user interface) should know that frequency changes are enacted upon (re-)writing to the last register (REG4).

Parameters	Configuration
ADC sampling frequency	Sampling frequency can be programmed over the range 40 Msamples/s to 210 Msamples/s. Step size is 0.5 MHz or 1MHz when the double data rate output is enabled (see REG4 bit1). The programmed frequency must be consistent with the jumpers. Always check that the PLL_LOCK status test point is high after changing this parameter. Data rates above 105 MSamples/s require the use of the double data rate output. See REG4 bit 1. Expressed in Hz. REG0: bit 7:0 (LSB) REG1: bit 15:8 REG2: bit 23:16 REG3: bit 31:24 (MSB)
Internal ADC sampling clock ON/OFF	Selection of the external ADC sampling clock EXT_ADC_CLK or the internal sampling clock is done primarily by Jumper. This control bit allows the user to switch off the internal sampling clock generation when using the external clock, so as to minimize noise. 0 = OFF 1 = ON REG4 bit 0
DDR output interface	Depending on the sampling speed, the output format can be interlaced double data rate or simple I/Q. 0 = simple output can be used for sampling rates in the range [40-105MHz]. 1 = Interlaced, double data rate (DDR) output format. See Timing . Can be used for sampling rates in the range [80–210 MHz] REG4 bit 1

Configuration example:

40 Msamples/s internal clock configuration
REG0/1/2/3/4 = 00 5A 62 02 01
Jumper JP1 in position 1-2
Frequency selection jumpers in positions: 1A + 2A

Monitoring

Parameters	Monitoring
PLL lock status (PLL_LOCK)	Indicates the clock frequency synthesizer lock status: locked to the frequency reference (1) or unlocked (0). SREG0 bit 0

Test Points

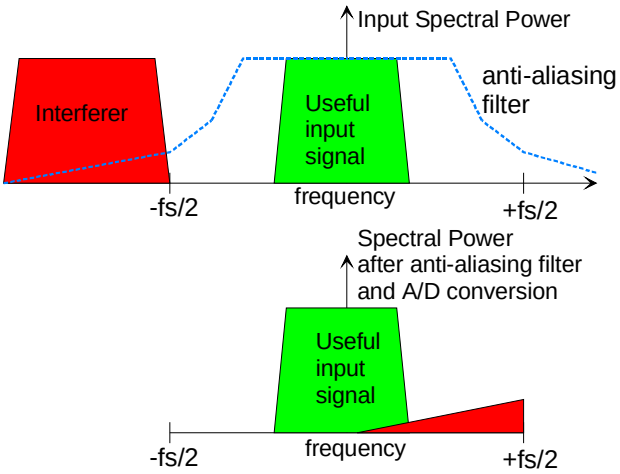
Test points are provided for easy access by an oscilloscope probe.

Test Point	Definition
TPI	Baseband signal, I-channel, at A/D converter input. The nominal amplitude is 1Vpp when the AGC loop is closed with the following demodulators (COM-1001, COM-1011/1018, COM-1027, COM-1008 or equivalent).
TPQ	Baseband signal, Q-channel, at A/D converter input. Same type as above.
PLL_LOCK	Frequency synthesizer PLL lock status. Active low: '1' when locked. This information is also available in status register SREG0
PLL_REF	Internal / External reference clock Note: do not connect any permanent test cable to this test point as it is likely to cause a significant degradation in phase noise performance.

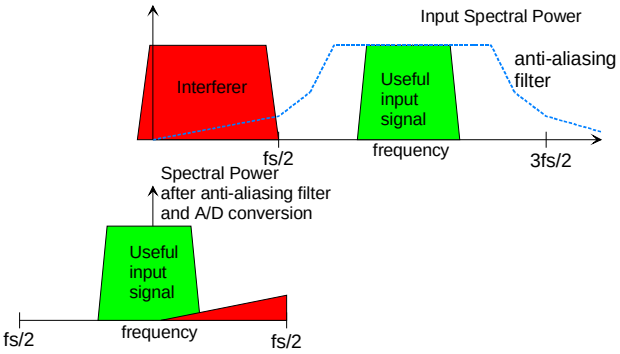
Operations

Select the sampling frequency

One of the unique feature of the COM-3008 is the ability to select the best sampling frequency for a given application. The COM-3008 can thus be configured for baseband sampling or for IF undersampling. The figures below illustrate the spectral relationship between analog input and sampled output.



Input/Output Spectrum. Baseband Input.



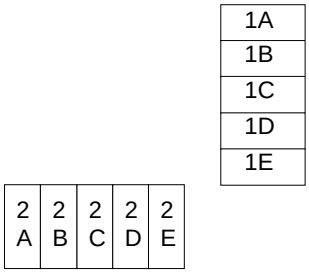
Input/Output Spectrum. Input centered around non-zero frequency. IF undersampling.

Programming the Sampling Clock

The sampling frequency is programmable over a range of [40 -210 Msamples/s] This range is segmented into jumper-selectable regions:

Sampling rate range (Msamples/s)	**Jumpers J3/J7**
40-46 or 80-92 (when DDR)	1A+2A
45-52 or 90-104 (when DDR)	1A+2B
52-58 or 104-116 (when DDR)	1B+2B
55-65 or 110-130 (when DDR)	1C+2C
61-72 or 122-144 (when DDR)	1C+2A+ 2C
69–86 or 138-172 (when DDR)	1D+2C
85–91 or 170-182 (when DDR)	1D+2D
90–97 or 180–194 (when DDR)	1B+1D + 2D
98–118 or 196–236 (when DDR)	1E+2D

Within each region, the sampling frequency is software programmable by steps of 0.5MSamples/s (1MSamples/s when DDR output) under user control.



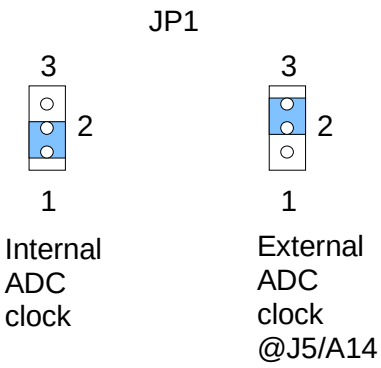
Jumper locations

Internal vs External frequency reference for sampling clock.

An external 10 MHz frequency reference can be used when the user application requires high frequency stability. In this case, simply connect a 10 MHz sinewave, clipped sinewave or square wave to the J8 EXTERNAL FREQ REF SMA connector. Detection and switching is automatic, thus no configuration change is needed. Upon removal of the external 10 MHz frequency reference signal, the COM-3008 reverts to the internal frequency reference.

Internal vs External ADC sampling clock

The source for the Analog to Digital converter clock can be selected to be internal (programmable) or external by changing the JP1 jumper.

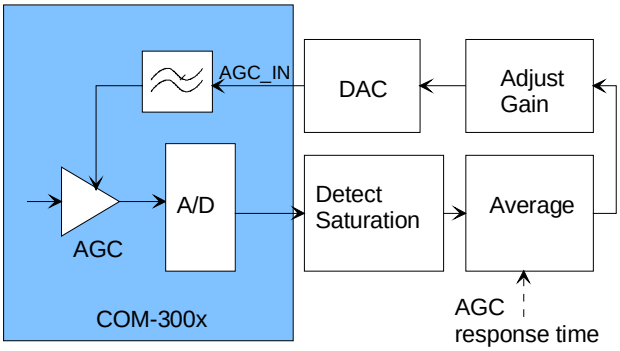


The external clock EXT_ADC_CLK is to be supplied at J5/A14 and must be in the range 210 Msamples/s max, 20 Msamples min.
In addition, the internal sampling clock generation can be switched off by software so as to minimize noise. See control REG4 bit 0.

Warning: selecting sampling rates less than half the baseband filter bandwidth may result in aliasing.

AGC

The default Automatic Gain Control (AGC) mechanism assumes than an external circuit (a demodulator for example) detects saturation conditions at the Analog-to-Digital converter and adjusts the receiver gain AGC_IN accordingly, as illustrated below:



AGC principle

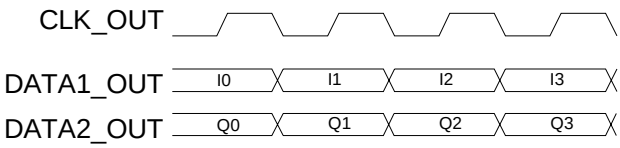
The AGC_IN signal can be a simple pulse-width modulated (PWM) digital signal or an analog signal from a DAC. The AGC_IN signal undergoes low-pass filtering within the COM-3008 in order to average out a PWM control signal. By default, the AGC response time is limited to approximately 1 second by the two RC low-pass filters where R = 100KΩ and C = 1µF.

Where applications require faster AGC response time, a few µseconds in the case of burst receivers for example, the RC low-pass filter bandwidth can be greatly increased by changing two resistors and/or capacitors. The COM-3008 AGC response time can be specified at the time of order.

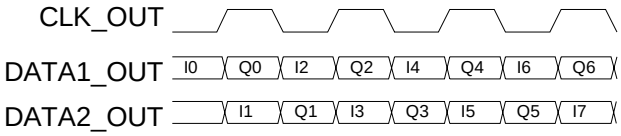
Timing

The COM-3008 interface depends on the sampling rate (see control register REG4 bit 1)

When REG4(1) = '0', the DATA1_OUT and DATA2_OUT signals are dedicated to I and Q samples respectively. Users should reclock these signals at the rising edge of CLK_OUT.



When REG4(1) = '1', a dual data rate (DDR) scheme is used whereby I and Q samples are interlaced as illustrated by the timing diagram below. Users should reclock these signals at the rising and falling edges of CLK_OUT.



Schematics

The schematics are available on the ComBlock CD shipped with every module. See the "Hardware Schematics" folder.

Interfacing with FPGA development platforms

In order to facilitate the (DDR) interface between the COM-3008 and FPGA development platforms such as the COM-1400, ComBlock has developed a VHDL project which is available on the ComBlock website and on the ComBlock CD-ROM.

Performance

Internal Clock Reference

The internal crystal performance is as follows:

- tolerance: [-20 to +5] ppm max @25C
- temperature stability (-10C to +60C): ± 50 ppm max
- aging: ±5ppm/year max (1st year) @25C

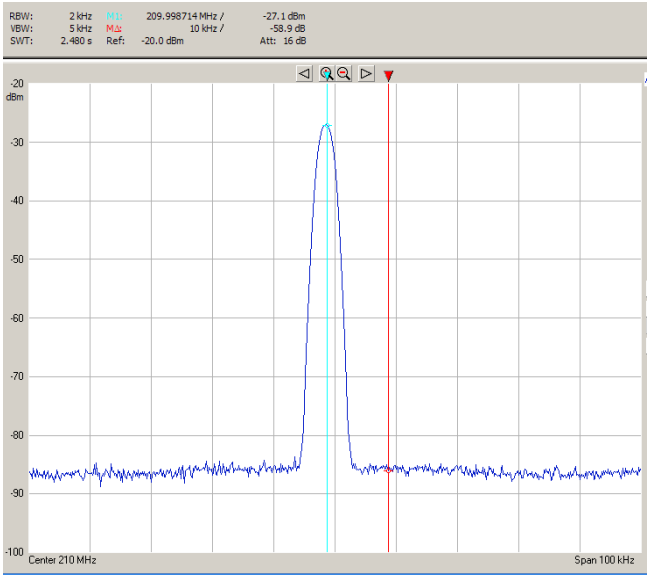
Receiver Sensitivity

The receiver sensitivity is defined at the minimum input level yielding a full-range (1Vpp) baseband signal at the analog-to-digital converter.
Sensitivity @ 1 MHz: -26 dBm.

Sampling Clock Phase Noise

When using the internal clock, the typical phase noise is:

- - 85 dBc @ 1 KHz
- - 90 dBc @ 10 KHz



Internal sampling clock phase noise:
210 MSamples/s. 100 KHz span, 2 KHz resolution bandwidth.

Low Pass Filter

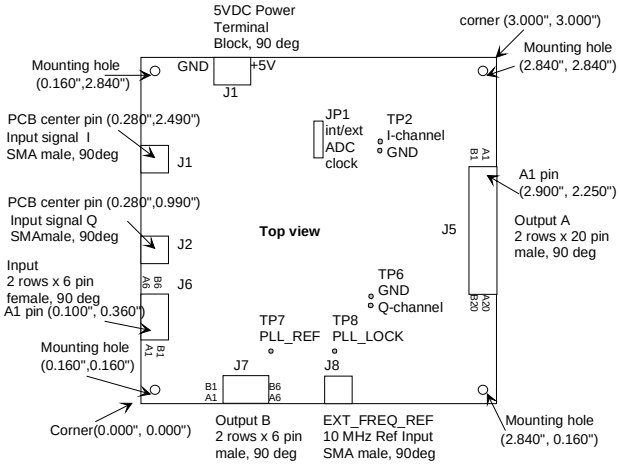
Each A/D converter is preceeded by a low-pass filter so as to reduce the input signal bandwidth and avoid aliasing at the A/D converter.

The baseline (-B0) filter response is
Cutoff frequency: (@-1dB): 80 Hz to 46 MHz
Cutoff frequencies (@-3dB): 20 Hz, 50 MHz
Rejection @100MHz: > 30 dB.

Other filters can be selected at the time of order.
List options here.

A 20 Hz (@-3 dB) high-pass filter is used to block the DC bias caused by LO leakage through the input connector.

Mechanical Interface



Mounting hole diameter: 0.125"

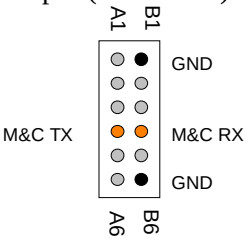
A1 pin height: 0.039"

Maximum height 0.500"

Pinout

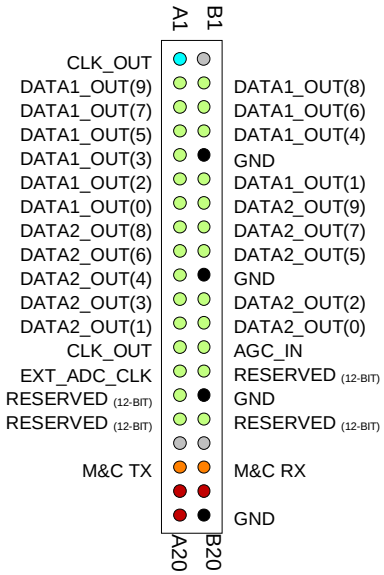
M&C Connector J7

12-pin (2 rows x 6) 2mm male connector.



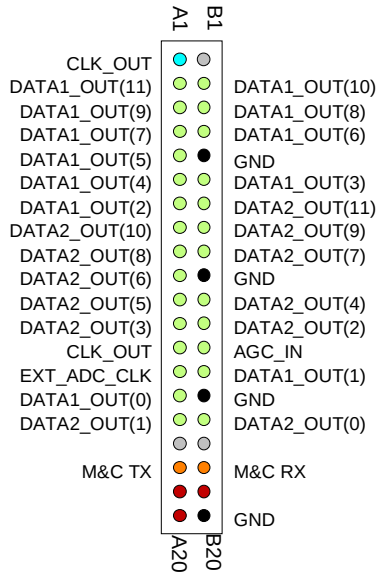
Output Connector J5 (COM-3008)

40-pin (2 rows x 20) 2mm male connector.



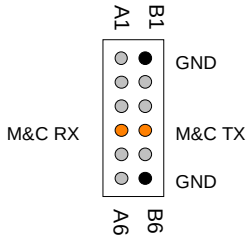
Output Connector J5 (COM-3009)

40-pin (2 rows x 20) 2mm male connector.



M&C Connector J6

12-pin (2 rows x 6) 2mm female connector.



I/O Compatibility List

(not an exhaustive list)

Input	Output
	COM-1001, COM-1018, COM-1027 demodulators (@ 40 MSamples/s)
	COM-8002 High-speed data acquisition. 256MB, 1Gbit/s, 40 Msamples/s.
	COM-1023 AWGN noise generator (@ 40 MSamples/s)
	COM-1024 Multipath generator (@ 40 MSamples/s)
	COM-1200, COM-1400 FPGA development platforms (full 210 Msamples/s)
	COM-2001 Dual D/A converter (baseband) (40-105 MSamples/s)
	COM-1501 Arbitrary Waveform Signal Generator

Configuration Management

This specification is to be used in conjunction with Atmel microcontroller software revision 8.

ComBlock Ordering Information

COM-3008	Dual Analog-To-Digital Conversion, 10-bit 210 Msamples/s.
COM-3009	Dual Analog-To-Digital Conversion, 12-bit 130 Msamples/s.

Select one or several of the options below:

Option –A: Input DC block:

- -A1: on (default)
- -A0: removed

Option B: anti-aliasing filter:

- -B1: 50 MHz LPF (default)
- -B2: no filter;

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