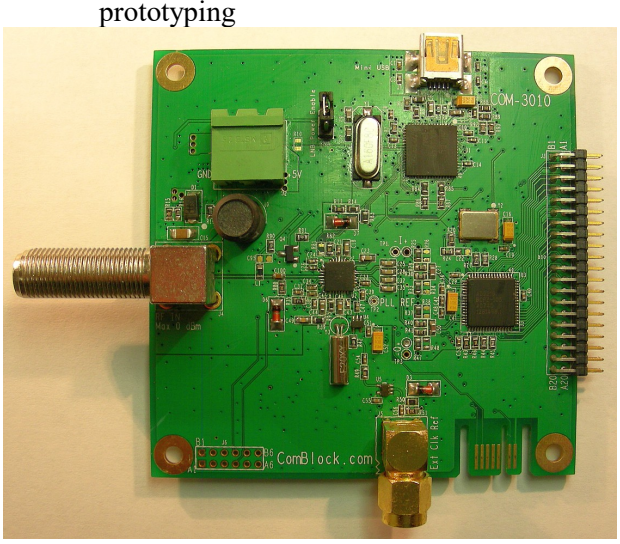
COM-3010 [925 – 2175 MHz] RECEIVER

Key Features

- [925 – 2175 MHz] Receiver for direct broadcast satellite applications or other broadband I/Q demodulator applications
- Designed for direct connection to K_a band, K_u band and C band LNBs
  - Type F female connector
  - 75 Ω input impedance
  - –63 dBm to 0 dBm input level
  - +13 / +18V LNB supply provided
  - bidirectonal DiSEqC control
- Built-in IF/baseband AGC, 73 dB dynamic range
- Low phase-noise frequency synthesizer can be tuned over entire range by steps of 19Hz
- Optional external 10 MHz frequency reference for the frequency synthesizer
- Fixed 40 Msamples/s (option -A) , 100Msamples/s (-B) or 104Msamples/s (-C) internal or variable external sampling clock
- Dual 10-bit Analog-to-Digital converter, up to 105 $^{Msamples}/_{second}$ (MSPS)
- Programmable baseband filtering bandwidth between 4 and 40 MHz
- USB Monitoring & Control Interface
- Only single +5V_{DC} supply required
- Connectorized 3”x 3” module for ease of prototyping



Typical Applications

- Direct to home satellite TV set-top box
  - DVB-S, DVB-S2

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com3010.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm

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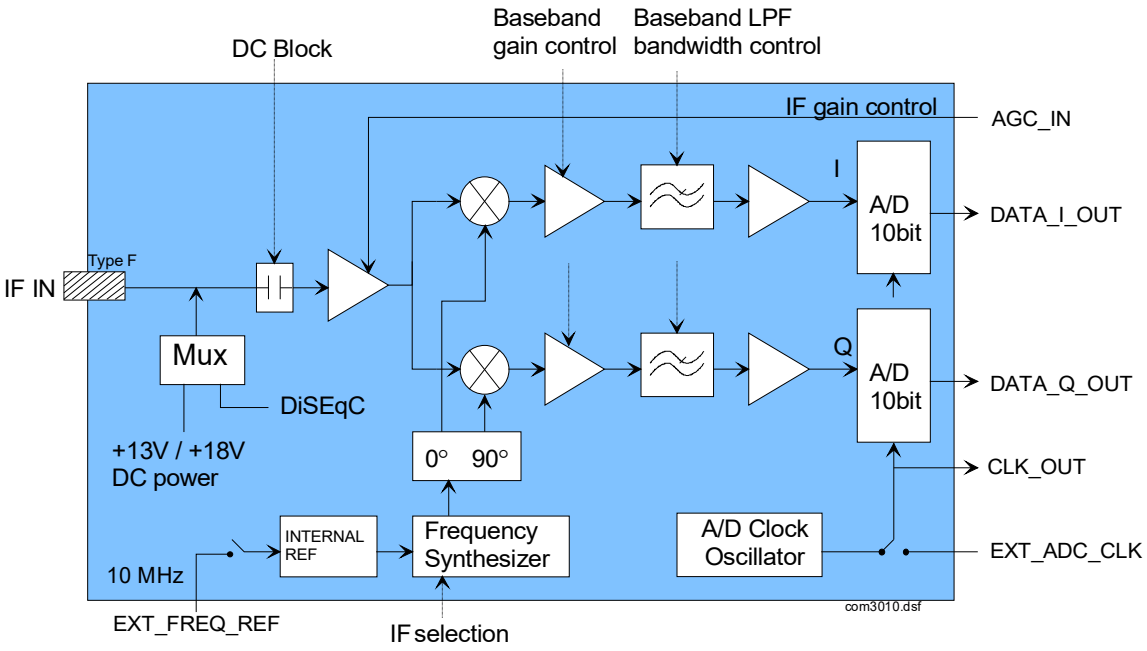


Block Diagram

Electrical Interface

Inputs / Outputs

Inputs	Definition
IF_IN	925 - 2175 MHz; Type F connector, female, 75 Ω impedance; Receiver sensitivity (worst case): -63 dBm at IF input for full scale signal ($1V_{pp}$) at A/D converter; Maximum input (operating): 0 dBm Maximum input (no damage): +10 dBm IF AGC range: 73 dB typ. Baseband AGC range: 15 dB Multiple signals are sent in the reverse direction (from the COM-3010 receiver to the external LNB) over the same coaxial cable: • LNB power supply • 22 KHz control commands (DiSEqC)
EXT_REF_CLK	Input. External 10 MHz frequency reference for frequency synthesis; Sine wave, clipped sine wave or square wave; J5 SMA male connector. 50 Ohm. Minimum level: 2Vpp. Maximum level: 3.3Vpp
Digital I/Os	**Definition**
DATA_I_OUT[9:0]	In-phase baseband signal; 10-bit digital samples. Unsigned format: 0x200 represents a zero, 0x000 the most negative signal, 0x3FF the most positive signal. 40/100 MSPS Unsigned
DATA_Q_OUT[9:0]	Quadrature baseband signal. Same characteristics as above.
CLK_OUT	Digital sampling clock output; Up to 105 MSPS; Read the samples at the rising edge of CLK_OUT
AGC_IN	Input signal to control the analog gain prior to A/D conversion. Can be digital (pulse-width modulated) or analog. The purpose is to use the maximum dynamic range while preventing saturation at the A/D converter. 0 is the maximum gain, +3V is the minimum gain.
EXT_ADC_CLK	Optional input. Externally supplied Analog-to-Digital converter sampling clock. Enabled or disabled by software control. LVTTL 0 – 3.3V. Selecting sampling rates less than half the baseband filter bandwidth may result in aliasing. Supply this clock at J3/A14. Sampling frequency: Min: 10 Msamples/s Max: 105 Msamples/s
USB Monitoring & Control	Mini-USB connector (type AB); Full speed / Low Speed
Power Interface	4.75 – 5.25V_{DC}; Terminal block; Power consumption is 300mA typ. (*excluding* internal LNB supply)

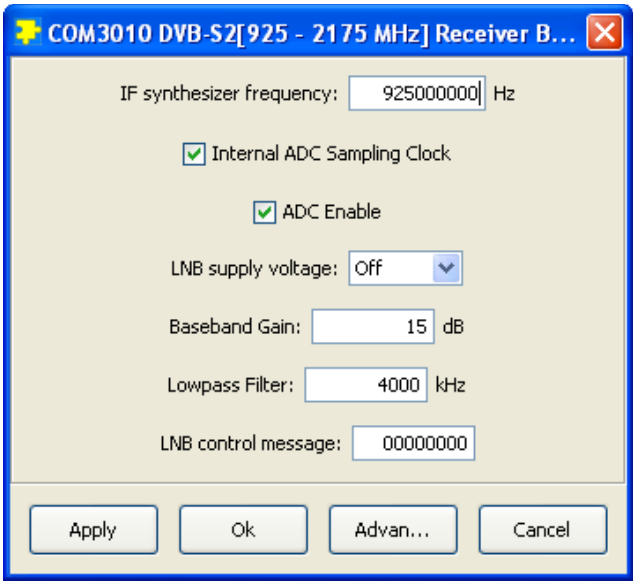
Electrical Interface

Configuration (via USB)

Complete ComBlock assemblies can be monitored and controlled centrally over a USB connection using the **ComBlock Control Center** software. A mini USB cable is required.

Configuration (Basic)

The easiest way to configure the COM-3010 is to use the **ComBlock Control Center** software supplied with the module on CD. In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-3010 module to be configured, next click the *Settings* button to display the *Settings* window shown below.



Settings Window

Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

The module configuration parameters are stored in non-volatile memory. All control registers are read/write. Undefined control registers or register bits are for backward software compatibility and/or future use. They are ignored in the current firmware version.

Programmers developing custom applications (using the ComBlock API instead of the supplied ComBlock control center graphical user interface) should know that frequency changes and DiSEqC are enacted upon (re-)writing to the last register (REG10).

Parameters	Configuration
IF synthesizer frequency	Valid range: 925– 2175 MHz; Steps of ~19 Hz[1]; Expressed in Hz; REG0: bit 7:0 (LSB) REG1: bit 15:8 REG2: bit 23:16 REG3: bit 7:0 (MSB)
External/Internal ADC sampling clock	0 = internal 1 = external REG4: bit 0
ADC Enable	0 = Disable 1 = Enable REG4: bit 1
LNB supply voltage Warning: Enabling LNB supply may cause damage to test equipment.	00 = off 01 = +13V_{DC} 10 = +18V_{DC} 11 = off REG4: bits 3-2
Baseband Gain Setting	Gain range 0 – 15 dB Expressed in dB REG4: bits 7-4
Lowpass Filter: –3 dB cutoff frequency	Valid range: 4 – 39.96 MHz; Steps of 290 kHz; Expressed in kHz; REG5: bits 7-0 (LSB) REG6: bit 15-8 (MSB)
LNB control message (DiSEqC)	4 bytes: frame sync, family of devices, command byte Bytes are transmitted MSB 1st The sequence is sent upon writing to REG10 and at power up. REG7: bits 7-0: byte 1 REG8: bits 7-0: byte 2 REG9: bits 7-0: byte 3 REG10: bits 7-0: byte 4

Configuration Registers

Note: [1] REG3:0 is a whole number *Hertz* approximation, using an internal step size of

$$19.0735\ Hz \text{ or } \frac{20\times10^6}{2^{20}}\ Hz$$

Monitoring (via USB)

Monitoring the status of the COM-3010 is performed by clicking the *status* button in ComBlock Control Center. A description of those registers and their meanings are described in the table below.

Programmers developing custom applications wishing to monitor module status can do so again by using the ComBlock API.

Parameters	Monitoring
reserved	SREG0: bit 0
Internal Power Supply Fault *(see schematics for reference)*	0 = Normal Operation 1 = Fault Condition Bit 7: ADC_+2.5V Bit 6: ADCA_+3.0V Bit 5: TUNER_+3.3V Bit 4: CLK_+3.3V Bit 3: D_+4.5V SREG0: bit 7-3
LNB supply voltage monitor	$V_{LNB} = SREG1_{10} * \frac{49.5}{255} V_{DC}$ SREG1: bit 7-0
AGC voltage monitor	$V_{AGC} = SREG2_{10} * \frac{4.5}{255} V_{DC}$ SREG2: bit 7-0
reserved	SREG3: bit 7-0
LNB response message (DiSEqC)	2 bytes: OK, status byte(s) Bytes are received MSB 1st SREG4: bits 7-0: byte 1 SREG5: bits 7-0: byte 2

Monitoring Registers

Operations

LNB power supply

The COM-3010 is capable of supplying either +13V_{DC} or +18V_{DC} to the low-noise block down-converter (LNB). In addition to the software control, the provided JP1 jumper must also be populated to enable the supply. JP1 is labeled "LNB Power Enable," located near the +5V terminal block. The maximum supply current is 500 mA.
Warning: Enabling the LNB supply may cause damage to test equipment such as a signal generator.

LNB control

The COM-3010 is capable of controlling the RF front-end polarity, satellite and frequency band over a single coaxial cable. The control method is compliant with the Digital Satellite Equipment Control, DiSEqC, an industry standard.

The polarization is selected by supplying either +13V_{DC} or +18V_{DC}. The LNB frequency bands and/or LNBs on a multi-feed system are selected by generating a binary DiSEqC message in the form of a modulated 22 KHz tone.

Internal vs. External frequency reference for frequency synthesizer

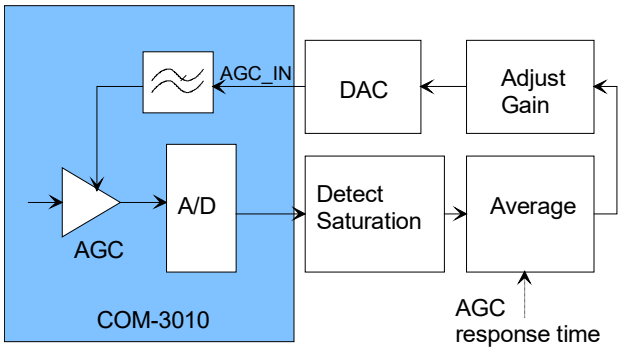
An external 10 MHz frequency reference can be used when the user application requires precise frequency stability. In this case, simply connect a 10 MHz sine wave, clipped sine wave or square wave to the J5 EXTERNAL_FREQ_REF male SMA connector. Detection is automatic, thus no configuration change is needed. Upon removal of the external 10 MHz frequency reference signal, the module reverts to the internal frequency reference.

Internal vs. External ADC sampling clock

The source for the Analog to Digital converter clock can be selected to be internal (fixed: 40 or 100MSPS) or external (variable: 10 min. to 105 max. MSPS) . External clock is enabled by software command and connecting an external clock to EXT_ADC_CLK supplied at the J3 connector, pin A14.

AGC

The default Automatic Gain Control (AGC) mechanism assumes that an external circuit (a demodulator for example) detects saturation conditions at the Analog-to-Digital converter and adjusts the receiver gain AGC_IN accordingly, as illustrated below:



AGC principle

The AGC_IN signal can be a simple pulse-width modulated (PWM) digital signal or an analog signal from a DAC. The AGC_IN signal undergoes low-pass filtering within the COM-3010 in order to average out a PWM control signal. By default, the AGC response time is limited to approximately 16 seconds by the RC low-pass filter where R = 1kΩ and C = 10µF.

Where applications require faster AGC response time, a few microseconds in the case of burst receivers for example, the RC low-pass filter bandwidth can be greatly increased by changing the R35 resistor and/or C85 capacitor. The COM-3010 AGC response time can be specified at the time of order.

Test Points

Test points are provided for easy access by an oscilloscope probe.

Test Point	Definition
I+ (TP1)	Baseband signal, I-channel, at A/D converter input; The nominal amplitude is $1V_{pp}$ (single ended) when the AGC loop is closed by a following demodulator (COM-1203 or equivalent)
Q+ (TP3)	Baseband signal, Q-channel, at A/D converter input. Nominal amplitude is $1V_{pp}$ (single ended) when the AGC loop is closed
PLL REF (TP2)	10 MHz synthesizer reference clock

Hardware Test Points

Performance

Internal clock reference

The internal crystal performance is as follows:

- Tolerance: [-10 to +10] ppm max. @25˚C
- Temperature stability (-10˚ to +60˚C): ± 50 ppm max.
- Aging: ±5ppm/year max. (1st year) @25˚C

I/Q frequency down-conversion

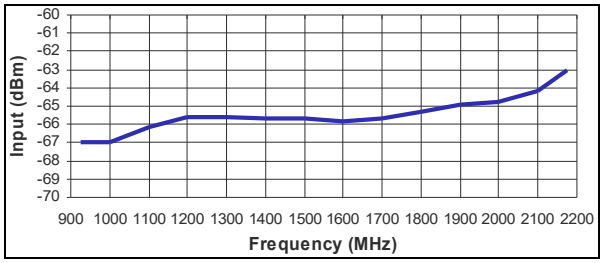
Quadrature phase error: 3.5˚ (Max.)
Quadrature gain error: ±1.0 dB (Max.)

Baseband low-pass filters

The 7th order Butterworth baseband lowpass filters are programmable. The filters' –3 dB (single sided) cutoff frequencies can be adjusted from 4 to 39.96 MHz in steps of 290 kHz. The power consumption is a function of the filter bandwidth setting, the higher the bandwidth, the higher the current.

Input Sensitivity

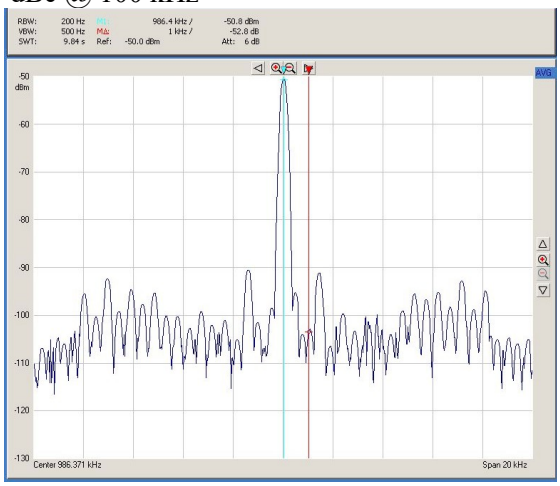
Measured for 1 V_{pp} (Single ended) from Q+ test point.



Input Sensitivity at 1 V_{pp}

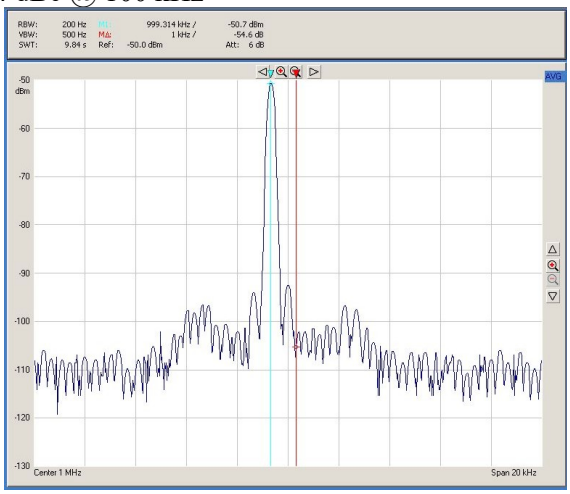
Phase noise

Typical phase noise performance at 2.175 GHz are:
-76 dBc @ 1 kHz away from the carrier
-82 dBc @ 10 kHz
-94 dBc @ 100 kHz



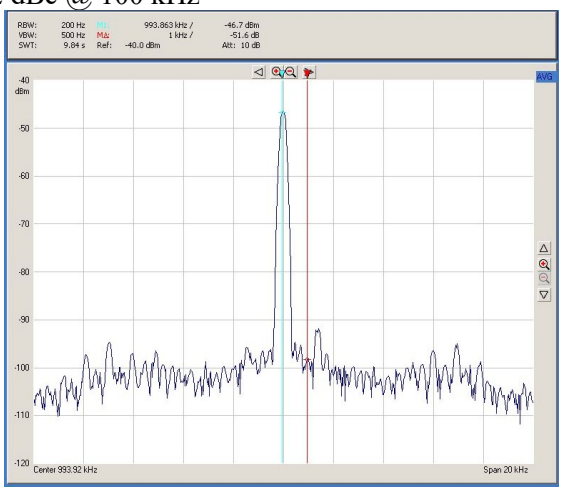
F_{IN} = 2176 MHz F_{LO} = 2175 MHz

Typical phase noise performance at 2.175 GHz **with** 10 MHz reference are:
-78 dBc @ 1 kHz away from the carrier
-85 dBc @ 10 kHz
-94 dBc @ 100 kHz



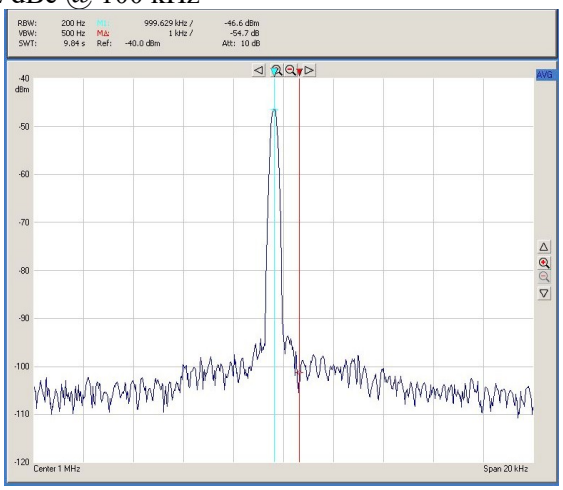
F_{IN} = 2176 MHz F_{LO} = 2175 MHz w/ Ext. Ref.

Typical phase noise performance at 925 MHz are:
-75 dBc @ 1 kHz away from the carrier
-82 dBc @ 10 kHz
-92 dBc @ 100 kHz



F_{IN} = 926 MHz F_{LO} = 925 MHz

Typical phase noise performance at 925 MHz **with** 10 MHz reference are:
-70 dBc @ 1 kHz away from the carrier
-82 dBc @ 10 kHz
-92 dBc @ 100 kHz



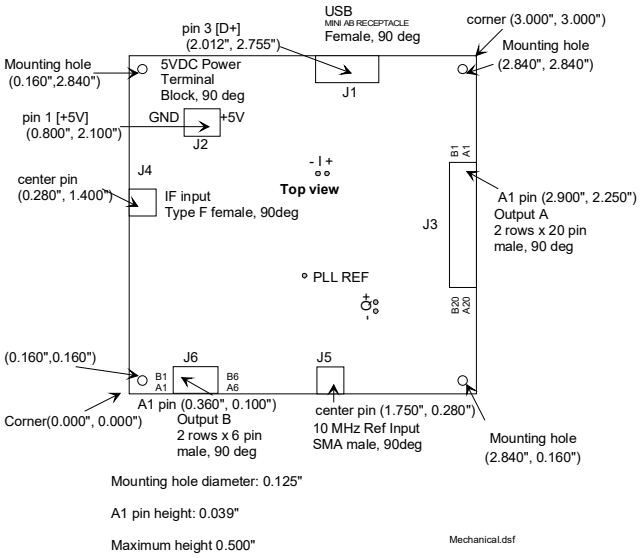
F_{IN} = 926 MHz F_{LO} = 925 MHz w/ Ext. Ref.

Spectral spurious lines are at -60 dBc or lower. (TBC)

Noise Floor

Measured at +25˚C and maximum IF & baseband gains.
-159 dBm/Hz @ F_{LO} = 925 MHz
-154 dBm/Hz @ F_{LO} = 2175 MHz

Mechanical Interface

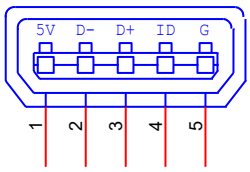


Mechanical Specification

Pinout

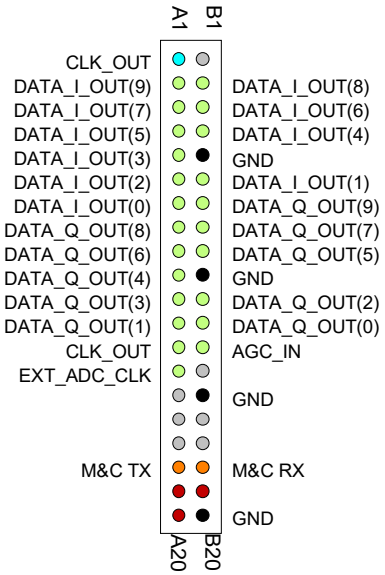
Mini USB Connector J1

The COM-3010 is a USB device with a mini type AB connector. (G = GND)



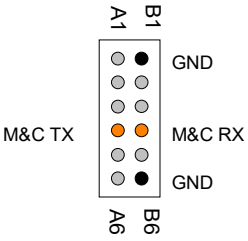
Output Connector J3

40-pin (2 rows x 20) 2mm male connector.



Output Connector J6

12-pin (2 rows x 6) 2mm male connector
[Not Populated]



I/O Compatibility List

(not an exhaustive list)

Input	Output
C / K_u / K_a bands LNBs	COM-1800 VHDL/FPGA development platform, Xilinx Artix7, DDR3 SODIMM socket, gigabit Ethernet
	COM-1802 PSK burst-mode modem
	COM-1831 Burst-mode DSSS modem
	COM-1505 PSK Modem
	COM-1518 Direct sequence spread-spectrum demodulator
	COM-1027 FSK Demodulator
	COM-1008 Variable Decimation

Input and ComBlock Compatibility List

ComBlock Ordering Information

COM-3010-A [925 – 2175 MHz] Receiver, AGC, A/D converters (40 Msamples/s)

COM-3010-B [925 – 2175 MHz] Receiver , AGC, A/D converters (100 Msamples/s)

COM-3010-C [925 – 2175 MHz] Receiver , AGC, A/D converters (104 Msamples/s)

ECCN 5A991.b.1

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