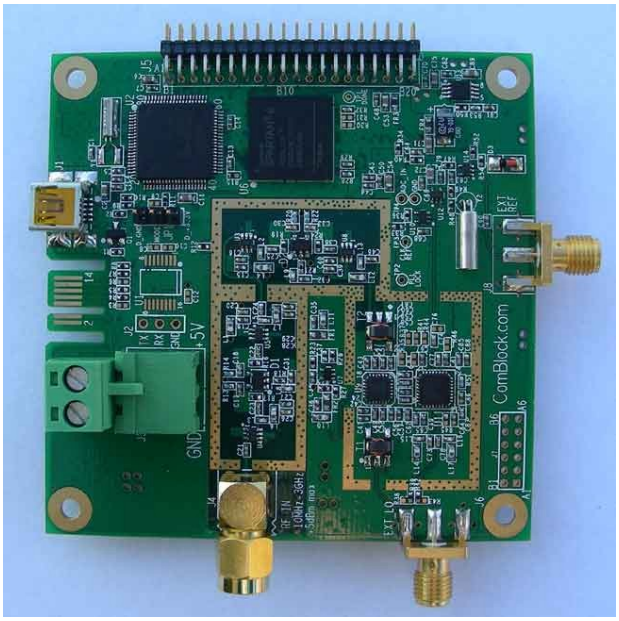
COM-3011 [20 MHz –3 GHz] Receiver / SDR Platform

Key Features

- [20-3000 MHz] receiver
- Input level:
  -65 dBm to –20 dBm (<200 MHz)
  -60 dBm to –20 dBm (<1 GHz)
  -55 dBm to –20 dBm (<3 GHz)
- Frequency synthesizer can be tuned over entire range by steps of 1Hz or less.
- External 10 or 20 MHz frequency reference can be used to achieve higher frequency stability.
- 8 preset frequencies for fast (<2ms) local oscillator frequency tuning.



COM-3011 *(shown without shield)*

- Selectable internal 100 MHz / external ADC sampling clock (to synchronize multiple receivers).
- Software-programmable channel filter bandwidth: 2 KHz to 40 MHz
- ARM processor and FPGA can be used for custom software-defined radio applications.
  - LPC1759 120 MHz 32-bit ARM Cortex-M3.
  - Xilinx Spartan-6 LX16 FPGA.
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.
- SMA connectors. Single 5V supply. Connectorized 3”x 3” module for ease of prototyping.

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com3011.pdf.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to http://www.comblock.com/product_list.html .

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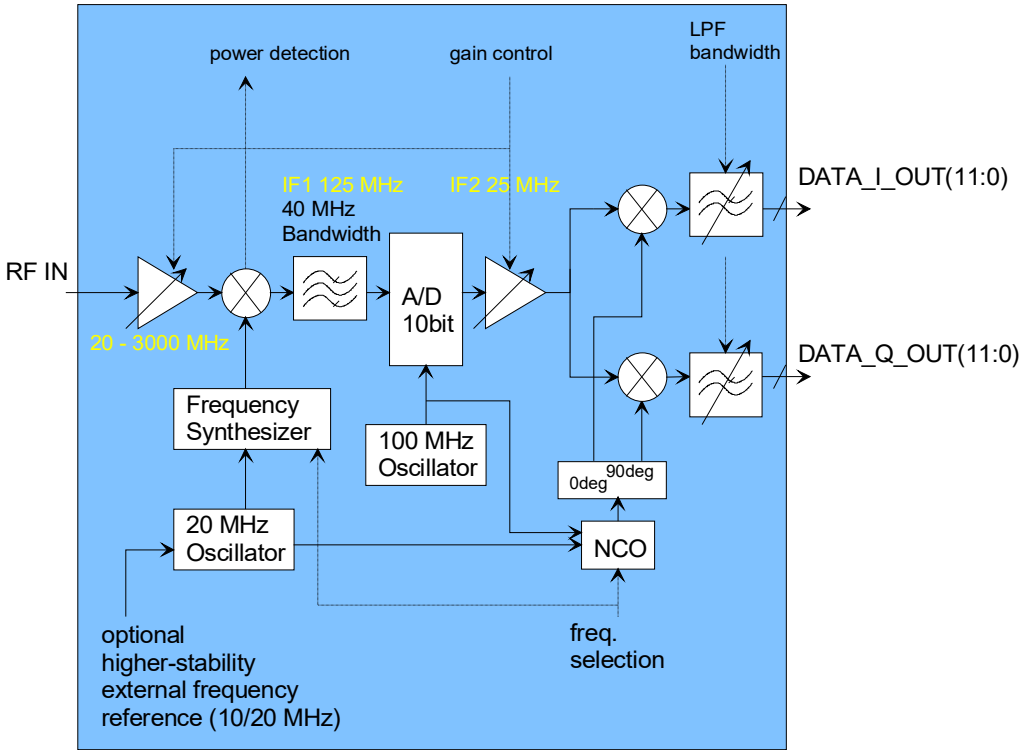
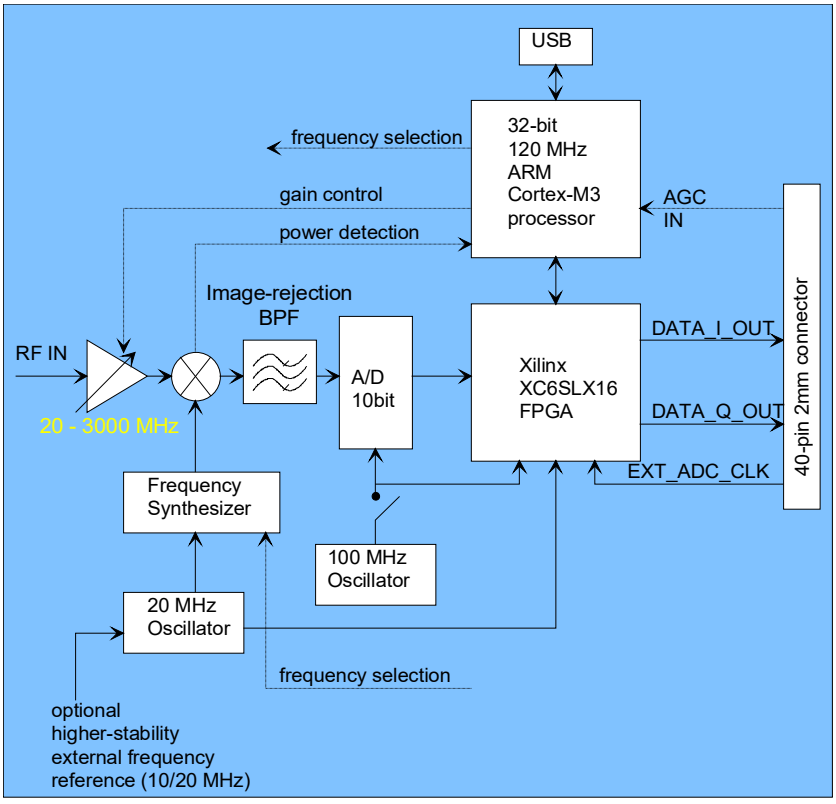
 Issued 7/24/2017



Functional block diagram



Hardware block diagram

Electrical Interface

Inputs / Outputs

Inputs	Definition
RF_IN	20 - 3000 MHz. SMA male connector (J3). 50 Ohm impedance. Receiver sensitivity: -65 dBm (< 200 MHz) -60 dBm (< 1 GHz) -55 dBm(<3 GHz) Maximum input (linear): -20 dBm Maximum input (no damage): +10 dBm
EXT_FREQ_REF	Optional input. External 10 or 20 MHz frequency reference for frequency synthesis. Sinewave, clipped sinewave or squarewave. SMA male connector (J8). Input is AC coupled. Minimum level 0.6Vpp. Maximum level: 3.3Vpp.
EXT_ADC_CLK	Optional input. Externally supplied Analog-to-Digital converter sampling clock. Enabled or disabled by software control. LVTTL 0 – 3.3V. Selecting sampling rates less than half the baseband filter bandwidth may result in aliasing.
EXT_LO	Optional input. Externally generated RF carrier for frequency down-conversion, thus bypassing the internal frequency synthesizer. Enabled or disabled by moving two SMT capacitors soldered on the board. AC coupled, 50 Ohm impedance. Input level: -10 to + 10 dBm.
Digital Output Signals	**Definition**
DATA_I_OUT[11:0]	In-phase baseband signal. 12-bit digital samples. Unsigned (straight offset binary) 0x800 = 0V value 0xFFF= most positive value 0x000 = most negative value
DATA_Q_OUT[11:0]	Quadrature baseband signal. Same format as DATA_I_OUT.
CLK_OUT	Digital clock. 40 or 100 Msamples/s if internal selection, otherwise EXT_ADC_CLK's frequency. Read the samples at the rising edge of CLK_OUT.
ADC_CLK_OUT	ADC clock (100 MHz when using internal ADC clock)
AGC_IN	Input signal to control the analog gain prior to A/D conversion. Can be digital (pulse-width modulated) or analog. The purpose is to use the maximum dynamic range while preventing saturation at the A/D converter. 0 is the maximum gain, +3V is the minimum gain. Without any subsequent module, the COM-3011's gain is set at its maximum and may thus saturate.
Control Lines	**Definition**
PLL_STROBE	Low-voltage (3.3V / 0V) TTL input control. Used to increment the modulo-N_{freq} frequency pointer (where N_{freq} is defined in Register 67) in a round-robin sequence. Rising edge triggered. Minimum pulse width: 10 µsec. Connector J6 Pin A3.
USB Monitoring & Control	Mini-USB connector Type AB Full speed / Low Speed
Power Interface	4.9 – 5.25VDC. Terminal block. Power consumption is 700 mA.

Absolute Maximum Ratings

Supply voltage	-8V min, +6.5V max
EXT_FREQ_REF, PLL_PROBE, EXT_ADC_CLK, AGC_IN	-0.3V min, +3.6V max
RF_IN, EXT_LO	+10 dBm

Configuration

An entire ComBlock assembly comprising several ComBlock modules can be monitored and controlled centrally over a single connection with a host computer. Connection types include built-in types:

- USB (requires a mini-USB cable)

or connections via adjacent ComBlocks:

- USB
- TCP-IP/LAN,
- Asynchronous serial (DB9)
- PC Card (CardBus, PCMCIA).

The module configuration is stored in non-volatile memory.

Configuration (Basic)

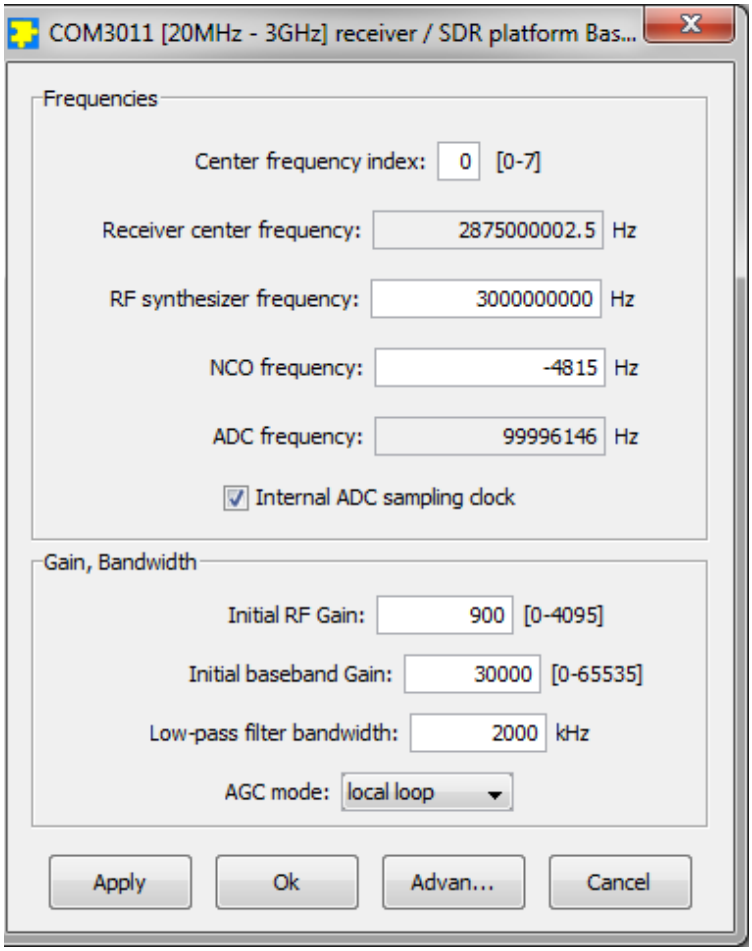
The easiest way to configure the COM-3011 is to use the **ComBlock Control Center** software supplied with the module on CD. In the ComBlock Control Center window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-3011 module to be configured and click the *Settings* button to display the *Basic Settings* window shown below.

Up to eight frequencies can be stored within each module at any given time. The current frequency is selected by an index in the range 0 to 7. Frequencies are expressed in Hz.

A basic frequency hopping scheme can be enabled by

(a) enabling the external trigger
(b) entering the number of frequency hopping steps in the round-robin arrangement.

For example, by specifying 4 steps, the receiver center frequency will follow the following index sequence: 0,1,2,3,0,1,2,3,0,1, etc., the index being incremented at the rising edge of each external PLL_STROBE pulse.



Basic Settings Window

Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write.

Undefined control registers or register bits are for backward software compatibility and/or future use. They are ignored in the current firmware version.

Programmers developing custom applications (using the ComBlock API instead of the supplied ComBlock control center graphical user interface) should know that frequency changes are enacted upon (re-)writing to the last register (REG71).

Parameters	Configuration
RF to IF1 frequency translation f_0	Preselected frequency translation 0. Valid range 137.5 MHz – 4.4 GHz, expressed in Hz. Select a frequency f_0 such that either $f_{RF} - f_0 = 125$ MHz (approxim.) or $f_{RF} + f_0 = 125$ MHz where f_{RF} is the RF input signal center frequency. 125 MHz is the IF1 band-pass filter center frequency. This only includes the RF frequency synthesizer. An additional frequency translation is performed digitally by an NCO, as specified by control registers REG36 and above. REG0: bit 7:0 (LSB) REG1: bit 15:8 REG2: bit 23:16 REG3: bit 31:24 (MSB)
LPF bandwidth	Programmable low-pass filter (one-sided) bandwidth expressed in KHz. Valid range 1KHz – 20 MHz. Double this value to get the total bandwidth. REG4: (LSB) REG5: (MSB)
Internal/External RF carrier generation	Enable or disable the RF frequency synthesizer. 0 = internal RF carrier generation. 1 = external RF carrier . An unmodulated RF signal must be supplied through J6. The RF frequency settings are thus ignored. A minor hardware modification must be performed prior to using the external RF carrier. See below for details. REG6(0)
Internal/External ADC sampling clock f_{clk}	Select the external ADC sampling clock EXT_ADC_CLK or the internal 100 MHz sampling clock. Selecting sampling rates less than half the baseband filter bandwidth may result in aliasing. 0 = internal 100 MHz ADC clock 1 = external ADC clock. REG6(1)
External controls enabled/disabled	Enable or disable the PLL_STROBE external control on the J6 connector. 0 = external control disabled 1 = external control enabled REG6(2)
Output sampling rate	Output sampling rate at the 40-pin connector. 0 = 40 MSamples/s 1 = ADC sampling rate (100 Msamples/s typ.) REG6(3)
Frequency selection	Use to switch local oscillator frequency among preselected values. Range 0 through 7 REG6(7:5)
RF to IF1 frequency translation f_x	Seven additional preselected frequency translations from RF to IF1. x = 1 through 7 Same format as f_0. REG(3+4*x): bits 7:0 (LSB) REG(4+4*x): bits 15:8 REG(5+4*x): bits 23:16 REG(6+4*x): bits 31:24 (MSB)
Number of RF frequencies N_{freq} in the scanning list	Each time a PLL_STROBE pulse is received, the frequency pointer increments modulo N_{freq}. N_{freq} is in the range 1 – 8. REG35: bit 7:0.
IF2 to Baseband frequency translation f_{ncox}	Eight preselected NCO frequency translations from IF2 to baseband.. x = 0 through 7 Format: $f_{ncox} * 2^{32} / f_{ADC}$ where f_{ADC} is the f_{ADC} sampling clock frequency (100 MHz internal or TBD external) REG(36+4*x): bits 7:0 (LSB) REG(37+4*x): bits 15:8 REG(38+4*x): bits 23:16 REG(39+4*x): bits 31:24 (MSB)
AGC loops	0 = open loops. RF and baseband gains are fixed. 1 = local RF and baseband AGC loops. Out-of-range conditions at the RF mixer, A/D converter and digital output are detected and corrected locally, without involving any external module. 2 = external baseband AGC loop. Follow-on module (demodulator for example) detects out-of-range conditions and adjusts the baseband gain accordingly using the AGC_IN pin. The RF AGC loop is still local as per 1. REG69(7:6)
RF Gain	Initial receiver RF gain (before the AGC takes over). 12-bit. 0 for the minimum gain, 4095 for the maximum gain. REG68: bits 7:0 (LSB) REG69(3:0): bits 11:8
Baseband Gain	Initial receiver baseband gain (before the baseband AGC takes over). 16-bit. 0 for the minimum gain, 0xFFFF for the maximum gain. REG70: (LSB) REG71: (MSB)

Monitoring

Parameters	Monitoring
PLL lock status (PLL_LOCK)	Indicates the RF synthesizer lock status: locked to the frequency reference (1) or unlocked (0). SREG0 bit 0
FPGA programmed	'1' when the FPGA is programmed with a valid configuration file. SREG0 bit 1
Power good for various internal supply voltages	'1' when the supply voltage is within a normal range. See schematics for supply voltages names. SREG0 bit 3: D_+3.3V SREG0 bit 4: AMP1_+3V SREG0 bit 5: A_+4.75V (unreliable) SREG0 bit 6: CLK_+3.3V SREG0 bit 7: SYNTH_+3.3V
Current receiver RF gain (RF AGC loop)	Range 0 – 4095 SREG1: bits 7:0 LSB SREG2(3:0): bits(11:8)
Current receiver baseband gain (baseband AGC loop)	Range 0 – 65535 SREG3: LSB SREG4: MSB
RF power detection at the RF mixer	Range 0 – 4095 SREG5: bits 7:0 LSB SREG6(3:0): bits(11:8)
Sampling clock frequency	Sampling clock frequency f_{clk} in Hz, measured every second using the internal 20 MHz or external 10/20 MHz frequency reference. SREG7: LSB SREG8 SREG9 SREG10: MSB

Test Points

Test points are provided for easy access by an oscilloscope probe.

Test Point	Definition
PLL_LOCK	Frequency synthesizer PLL lock status. Active low: '1' when locked. This information is also available in status register SREG0
CLK_REF	20 MHz frequency reference clock (after doubling when supplying a 10 MHz external frequency reference)
ADC_IN	IF1 (125 MHz intermediate frequency) signal prior to A/D conversion. The nominal amplitude is 0.5Vpp when the AGC loop is closed with the following demodulator (COM-1001,1202,1418,1027 or equivalent).
TP1 / ADC_CLK	Selected ADC sampling clock.
DONE	'1' indicates proper FPGA configuration.

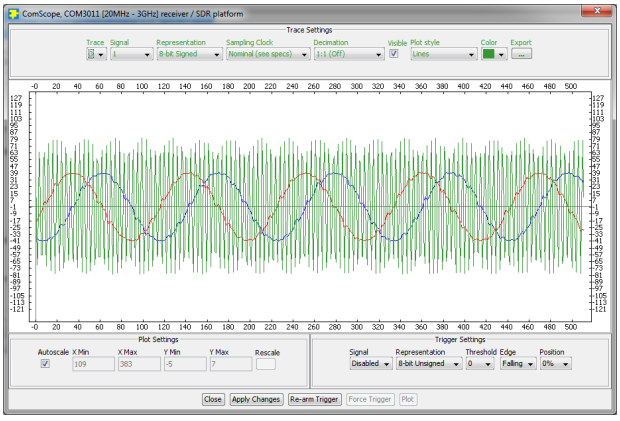
ComScope Monitoring

Key FPGA internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. The COM-3011 signal traces and trigger are defined as follows:

Trace 1 signals	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: I signal after frequency translation to baseband and image-rejection filtering	8-bit signed	f_{clk}	512
Trace 2 signals	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: Q signal after frequency translation to baseband and image-rejection filtering	8-bit signed	f_{clk}	512
Trace 3 signals	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: Input signal (Intermediate frequency IF2 25 MHz) A/D converter output	8-bit signed	f_{clk}	512

Trigger Signal	**Format**
N/A	1-bit

The sampling rate f_{clk} is the ADC sampling rate. The ComScope user manual is available at www.comblock.com/download/comscope.pdf.



ComScope Window Sample: showing ADC samples (green), and output samples after final frequency down-conversion to baseband (blue = I, red = Q)

Operations

Receiver Center Frequency

The receiver translates the received signal frequency to (near-zero) baseband in three steps:

1) A programmable RF frequency synthesizer fed to a RF mixer translates the signal center frequency from RF to a + or - 125 MHz intermediate frequency (IF1).
2) The IF1 signal undergoes IF undersampling at the Analog-to-Digital converter, in effect translating the center frequency to a 25 MHz intermediate frequency (IF2). The frequency translation equals the ADC sampling clock frequency (100 MHz when using the internal ADC sampling clock).
3) A programmable numerically controlled oscillator further translates the IF2 signal frequency to baseband.

Internal vs External Frequency Reference

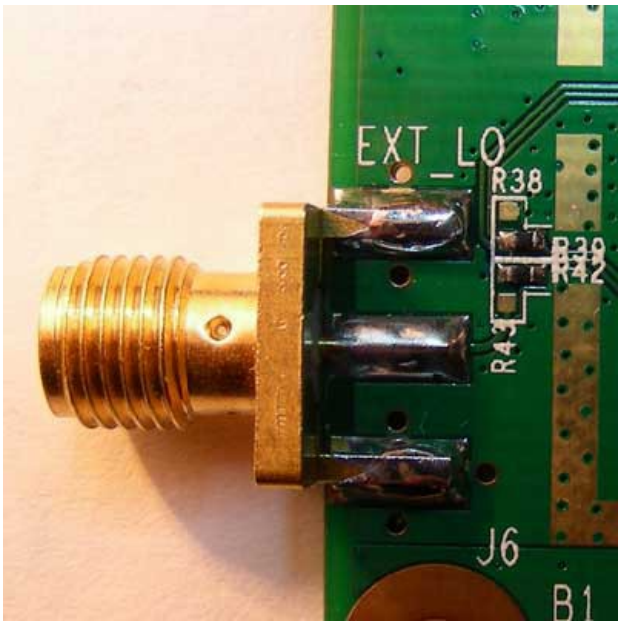
An external 10 or 20 MHz frequency reference can be used when the user application requires high frequency stability. In this case, simply connect a 10 or 20 MHz sinewave, clipped sinewave or square wave to the J8 connector. Detection is automatic, thus no configuration change is needed. Upon removal of the external frequency reference signal, the COM-3011 reverts to the internal frequency reference.

Internal vs External ADC sampling clock

The source for the Analog to Digital converter clock can be selected to be internal (fixed 100 Msamples/s) or external (up to 105 Msamples/s) by software command.

External RF carrier

Phase-synchronized operation of multiple units is possible by suppling an externally-generated RF carrier for frequency upconversion via the J6 EXT_LO SMA connector. This configuration is not software configurable: the RF carrier path is altered by moving the R42 and R39 resistors 90 degrees to the R43 and R38 pads respectively, as illustrated below:



In order to minimize noise when an external RF carrier is used, it is recommended to switch off the built-in RF frequency synthesizer by software (see control register REG6(0)).

AGCs

The COM-3011 comprises two independent AGC loops:

- The **RF AGC** loop's objective is to prevent any saturation up between the RF input and the A/D converter. It automatically adjusts the RF gain based on two sensors: power detection at the RF mixer (i.e. before the IF bandpass filter) and out-of-range condition at the A/D converter (i.e after the IF bandpass filter).
- The **baseband AGC** loop's objective is to maximize the amplitude of the digital output samples while avoiding saturation. It automatically adjusts the digital baseband gain based on out-of-range condition at the digital output (i.e. after the baseband low-pass filters).

FPGA Customization (optional)

The FPGA can be reprogrammed with user-specific code. Use of the FPGA is at the user's discretion. The FPGA is pre-programmed with all basic functions described in this specification document.

FPGA: Xilinx Spartan-6 XC6SLX.

When generating the bit file using Xilinx ISE, the bitstream compression option (-g Compress) must be enabled.

Flash memory size limitation: one FPGA configuration, maximum size 425984 bits.

FPGA configuration time at power up: < 150 ms

Performance

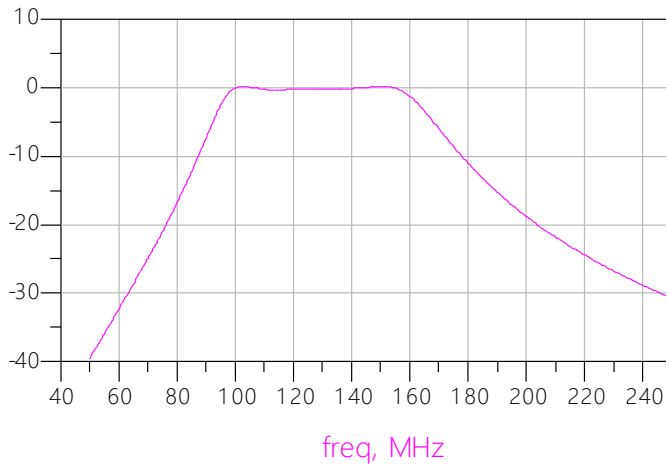
Internal Clock Reference

The internal crystal performance is as follows:

- tolerance: ± 10 ppm max @25C
- temperature stability (-10C to +60C): ± 50 ppm max
- aging: ±5ppm/year max @25C

Band Pass Filter

The A/D converter is preceeded by a band-pass filter centered at 125 MHz. The one-sided -3 dB cutoff frequency is 25 MHz. Within the [0-20 MHz] band, the maximum in-band ripple ± 0.2 dB.



COM-3011 anti-aliasing bandpass

Phase Noise

Typical phase noise of the RF synthesizer is:

f_{RF} =300 MHz

-76 dBc/Hz @ 1 KHz, typ.

-84 dBc/Hz @ 10 KHz, typ.

f_{RF} =3 GHz

-67 dBc/Hz @ 1 KHz, typ.

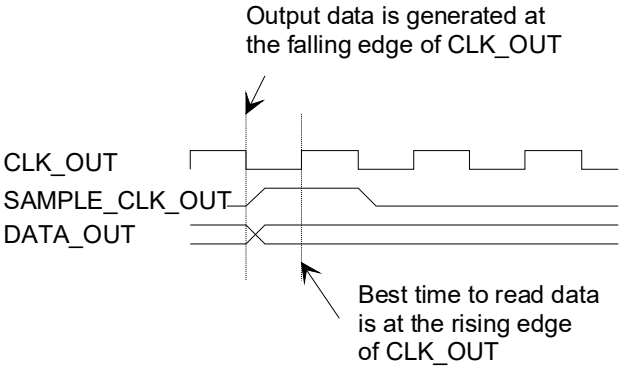
-73 dBc/Hz @ 10 KHz, typ.

Other Specifications

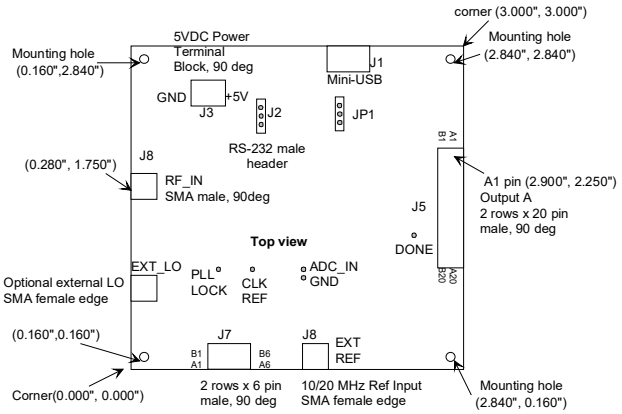
Input noise figure: 7 dB typ.
LO Out-of-band spectral spurious lines: < - 55 dBc.
Spurious signals at RF_IN input (other than LO):
< -80 dBm

Timing

Output



Mechanical Interface



Mounting hole diameter: 0.125"

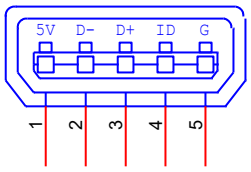
A1 pin height: 0.039"

Maximum height 0.500"

Pinout

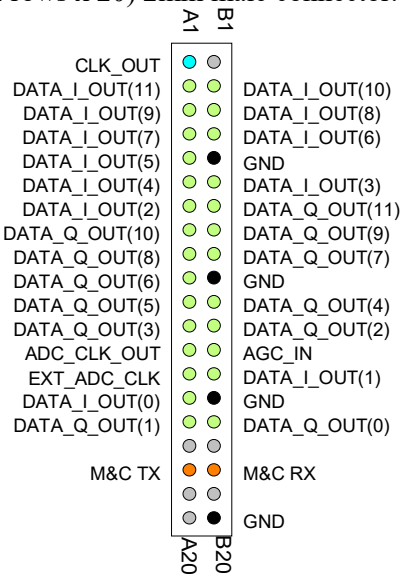
Mini USB Connector, J1

The COM-3011 is a USB device with a mini type AB connector. (G = GND)



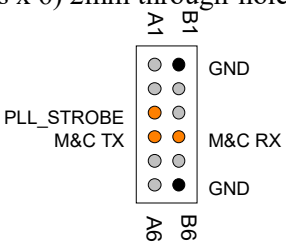
Output Connector J5

40-pin (2 rows x 20) 2mm male connector.



Connector J7

12-pin (2 rows x 6) 2mm through-hole connector.



I/O Compatibility List

(not an exhaustive list)

Output
COM-1800 FPGA (XC7A100T) + ARM + DDR3 SODIMM socket + GbE DEVELOPMENT PLATFORM [1]
COM-1806 Wideband signal capture and playback[2]
COM-1202 PSK/QAM/APSK modem
COM-1518 DS Spread-Spectrum demodulator 22 Mchips
COM-1827 Continuous phase demodulator (MSK, etc)
COM-2001 Dual D/A converter (baseband)
COM-1524 Channel emulator

Configuration Management

This specification is to be used in conjunction with
FPGA VHDL software revision 4.
ARM microcontroller software revision 3.01.

ComBlock Ordering Information

COM-3011 [20-3000 MHz] receiver / SDR platform

ECCN: 5A991.g

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[1] 98-pin to 40-pin adapters to interface with other Comblocks are supplied free of charge. Please let us know about your interface requirements at the time of order.

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