COM-3501 UHF Transceiver

Key Features

- Half-duplex UHF transceiver: 225 to 400 MHz, tunable by steps of 100 KHz. The transmitter and receiver operate at the same frequency.
- Receiver sensitivity: -89 dBm RF input for 1Vpp baseband output.
  Noise figure: < 6 dB.
- Output power P_{sat} = 26 dBm at antenna port.
- Receiver gain control:
  50 dB dynamic range control at IF.
  25 dB dynamic range at RF LNA.
- Transmitter gain control:
  17 dB dynamic range control IF
- 3.5 µs Tx/Rx switch.

- Selectable internal / external 10 MHz frequency reference for the frequency synthesizer.
- 8 preset frequencies for fast (<2ms) local oscillator frequency tuning.
- Baseband filtering options:
  - Narrowband applications (**-A**) (< 400 KHz)
- SMA RF connector. Single 5V supply. Connectorized 3"x 3" module for ease of prototyping.

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com3501.pdf.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .

MSS • 845 Quince Orchard Boulevard Ste N • Gaithersburg, Maryland 20878-1676 • U.S.A.
Telephone: (240) 631-1111 Facsimile: (240) 631-1676 www.ComBlock.com
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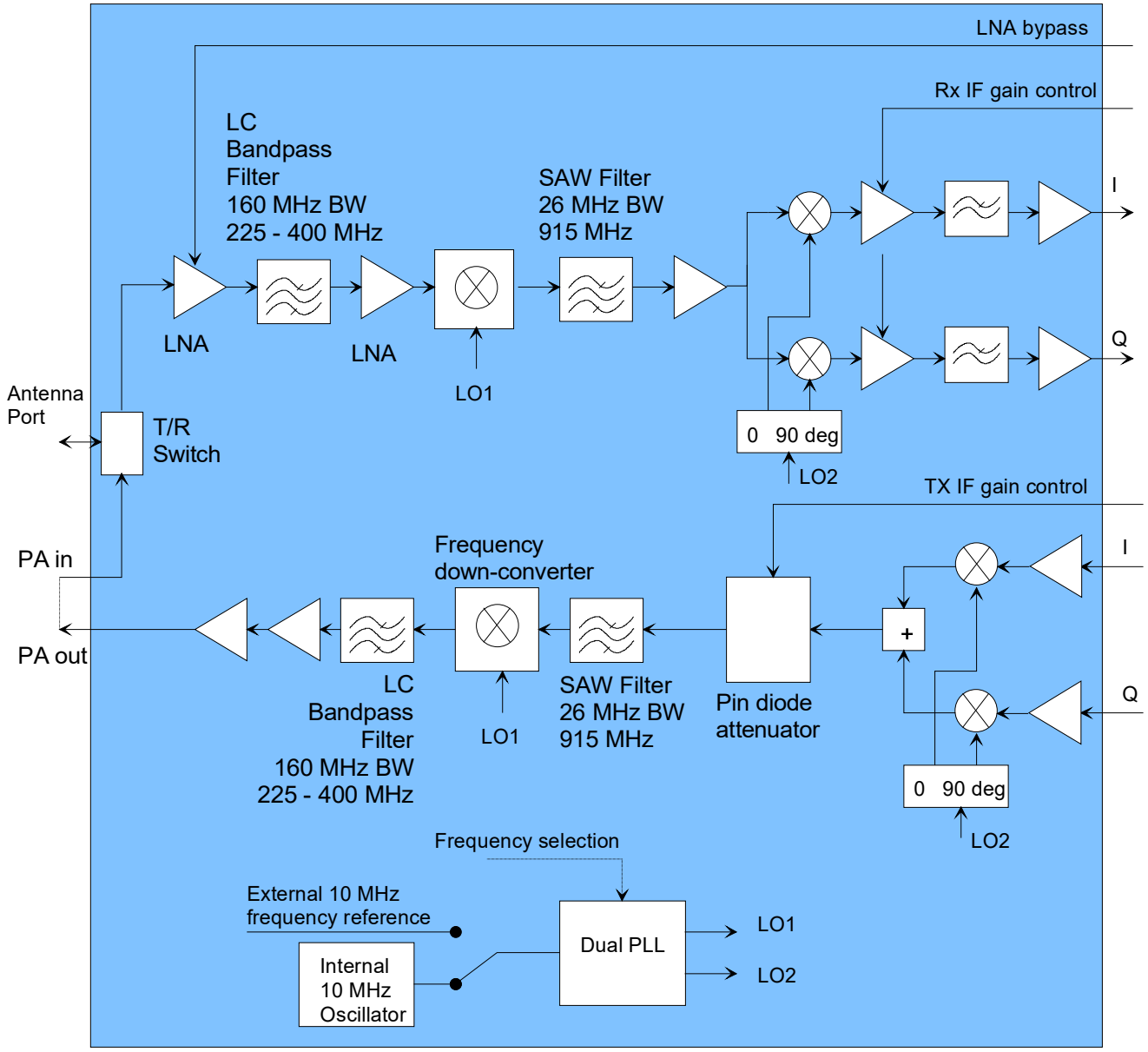


Electrical Interface

Inputs / Outputs

RF I/O	Definition
ANT	Antenna port. SMA female connector (J2) 50 Ohm impedance. Receiver in-band sensitivity: -89 dBm for 1Vpp at baseband. Maximum input (operating): TBD Maximum input while in receive mode (no damage): + 15 dBm

Analog Baseband I/O	Definition
EXT_FREQ_REF	Optional input. External 10 MHz frequency reference for frequency synthesis. Sinewave, clipped sinewave or squarewave. SMA male connector (J9). Input is AC coupled. Minimum level 0.6Vpp. Maximum level: 3.3Vpp. Note: when selecting external reference clock, the local oscillator phase noise depends on the input signal level: the larger the signal, the better the phase noise.

RX_I_P RX_I_N	Received baseband In-phase (I) output signal. Maximum range 2Vpp differential (1Vpp on each RX_I_P and RX_I_N signal). AC coupling. Common mode voltage set externally.
RX_Q_P RX_Q_N	Received baseband Quadrature (Q) output signal. Maximum range 2Vpp differential (1Vpp on each RX_Q_P and RX_Q_N signal). AC coupling. Common mode voltage set externally.
RX_AGC1	Receiver IF gain control. Analog input in the range 0 – 3.3V. Range: 40 dB. Non-linear scale. 0V yield the maximum gain.
TX_I_P TX_I_N	Transmit baseband In-phase (I) input signal. Full range 2Vpp differential (1Vpp on each TX_I_P and TX_I_N signal). Input impedance 250 Ohm.
TX_Q_P TX_Q_N	Transmit baseband Quadrature (Q) input signal. Full range 2Vpp differential (1Vpp on each TX_Q_P and TX_Q_N signal). Input impedance 250 Ohm.
TX_GAIN_CNTRL1	Transmitter IF gain control. Analog input in the range 0 – 3.3V. Controls the transmitter PIN diode attenuator. Typically 18 dB gain control is achievable. Non-linear scale., see calibration curve. 0V yield the minimum gain.
TX_POWER_DET	Transmitter power detection. Analog output in the range 0 – 3.3V. dB scale. See power measurement calibration curves.
Digital Output Signals	**Definition**
CLK_OUT	10 MHz frequency reference output. This signal can be used by external signal processing modules to calibrate the RF frequency references. LVTTL 0 – 3.3V.
Control Lines	**Definition**
RX_AGC2	Binary receiver gain control in the form of LNA first stage bypass. '0' when LNA is bypassed, '1' when LNA provides full gain. Gain step: 25 - 28 dB typ. Digital input. LVTTL (0-3.3V) This discrete gain control is primarily used to desensitize the receiver and prevent saturation in presence of strong input signals. No latency.
RX_AGC3	Binary receiver gain control in the form of LNA second stage bypass. '1' when LNA is bypassed, '0' when LNA provides full gain. Gain step: 25 - 28 dB typ. Digital input. LVTTL (0-3.3V) Please note that the control signals are reversed with respect to RX_AGC2.
TX_ENB	Transmitter enable. LVTTL input signal. '1' when the transmitter is active, '0' otherwise. The primary goal of this signal is to reduce the transceiver power when in receive-only (standby) mode. TX_ENB's response is slow due to the power supplies' large capacitors.
RX_TXN	Receive/Transmit# selection. '0' = transmit '1' = receive. Controls the T/R switch. LVTTL input. Guard time for the power amplifier to ramp up is 3.5usec.
PLL_STROBE	Low-voltage (3.3V / 0V) TTL input control. Used to increment the modulo- N_{freq} frequency pointer (where N_{freq} is defined in Register 35) RF frequency 0 -> RF frequency 1 -> RF frequency 2 -> RF frequency 0 > etc… Rising edge triggered. Minimum pulse width: 10 µsec.
Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4V – 5.25V DC. Terminal block. Best performance when supply voltage is 5.0V. Power consumption is 1.0A typ. when receive-only operation. < 2.0A when half-duplex operation (depends on the duty cycle).

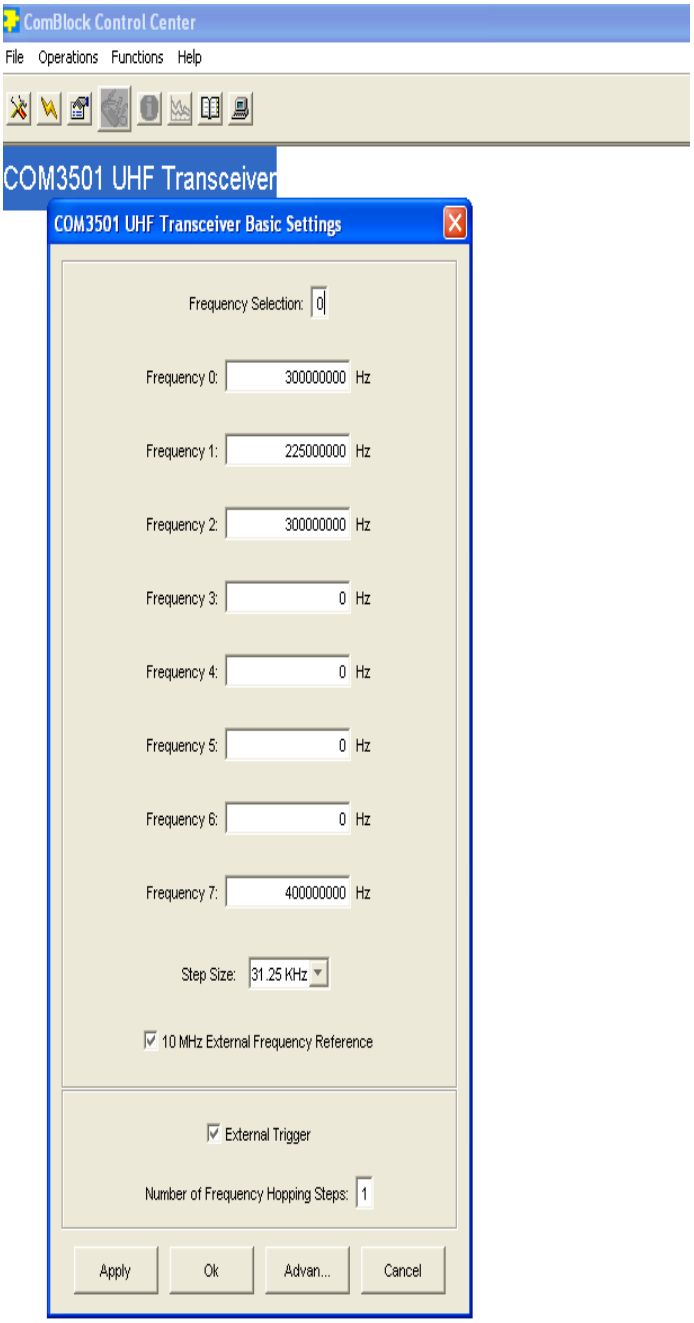
Absolute Maximum Ratings

ANT input	+15 dBm
DC voltage	+6V / -400VDC
Digital inputs	[-0.3V, +3.6V]
Analog baseband inputs	[-0.3V, +3.6V]

Configuration

Complete assemblies can be monitored and controlled centrally over a single serial or, when available through adjacent ComBlocks, LAN/TCP-IP, USB 2.0 or CardBus/PCMCIA connection.

The module configuration is stored in non-volatile memory.



Configuration (Basic)

The easiest way to configure the COM-3501 is to use the ComBlock Control Center software supplied with the module(s). After detecting the ComBlock modules (2nd button from left), highlight the COM-3501 module to be configured. Then press the settings button (3rd button from the left).
Users can store up to 8 frequencies within a COM-3501. The preset RF frequencies are expressed in Hz but must be integer multiple of the selected step size: 100 KHz, 31.25 KHz or 25 KHz.

There are two methods for switching between the preset frequencies:

- Manually through the basic settings window: change the frequency selection index (a number in the range 0 through 7) and press the Apply or OK button.
- Automatically through the PLL_STROBE external trigger (when enabled). The user must first determine the number of pre-set frequencies in the frequency hopping group. For example, if the selected number of frequency hopping steps is 3, the COM-3501 center frequency will follow the frequency pattern 0, 1, 2, 0, 1, 2, 0, 1, 2, etc. every time the PLL_STROBE is activated.

Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write.

Undefined control registers or register bits are for backward software compatibility and/or future use. They are ignored in the current firmware version.

Programmers developing custom applications (using the ComBlock API instead of the supplied ComBlock control center graphical user interface) should know that frequency changes are enacted upon (re-)writing to the last register (REG35).

Parameters	Configuration
RF frequency 0 $\mathbf{f_0}$	Preselected frequency 0. Valid range 225 - 400 MHz, expressed in Hz. $\mathbf{f_0}$ must be an integer multiple of the 100 / 31.25 or 25 KHz selected frequency step. REG0: bit 7:0 (LSB) REG1: bit 15:8 REG2: bit 23:16 REG3: bit 31:24 (MSB)
External/Internal frequency reference	0 = internal 10 MHz clock. 1 = external (10 MHz typ.) frequency reference. REG4 bit 0
External controls enabled/disabled	Enable or disable the PLL_STROBE external control on the J7 connector. 0 = external control disabled 1 = external control enabled REG6: bit 1
Step size selection	Chose between 100, 31.25 or 25 KHz step size. 00 = 100 KHz step 01 = 31.25 KHz step 10 = 25 KHz step REG6 bits 4-3.
Frequency selection	Use to switch local oscillator frequency among preselected values. Range 0 through 7 REG6 bits 7-5.
RF frequency 1	Preselected frequency 1. Same format as RF frequency 0. REG7: bit 7:0 (LSB) REG8: bit 15:8 REG9: bit 23:16 REG10: bit 31:24 (MSB)
RF frequency 2	Preselected frequency 2. Same format as RF frequency 0. REG11: bit 7:0 (LSB) REG12: bit 15:8 REG13: bit 23:16 REG14: bit 31:24 (MSB)
RF frequency 3	Preselected frequency 3. Same format as RF frequency 0. REG15: bit 7:0 (LSB) REG16: bit 15:8 REG17: bit 23:16 REG18: bit 31:24 (MSB)
RF frequency 4	Preselected frequency 4. Same format as RF frequency 0. REG19: bit 7:0 (LSB) REG20: bit 15:8 REG21: bit 23:16 REG22: bit 31:24 (MSB)
RF frequency 5	Preselected frequency 5. Same format as RF frequency 0. REG23: bit 7:0 (LSB) REG24: bit 15:8 REG25: bit 23:16 REG26: bit 31:24 (MSB)
RF frequency 6	Preselected frequency 6. Same format as RF frequency 0. REG27: bit 7:0 (LSB) REG28: bit 15:8 REG29: bit 23:16 REG30: bit 31:24 (MSB)
RF frequency 7	Preselected frequency 7. Same format as RF frequency 0. REG31: bit 7:0 (LSB) REG32: bit 15:8 REG33: bit 23:16 REG34: bit 31:24 (MSB)
Number of RF frequencies N_{freq} in the scanning list	Each time a PLL_STROBE pulse is received, the frequency pointer increments modulo N_{freq}. N_{freq} is in the range 1 – 8. REG35: bit 7:0.

Monitoring

Status monitoring registers are read-only.

Parameters	Monitoring
PLL lock status	'1' = locked '0' = unlocked REG36 bit 0

Test Points

Test points are provided for easy access by an oscilloscope probe.

Test Point	Definition
PLL_LOCK	Frequency synthesizer PLL lock status. Active low: '0' when locked. PLL lock status is also available by reading status register REG36 from a host computer..
PLL_REF	Reference clock (10 MHz external or internal)

Operations

Internal vs External frequency reference for frequency synthesizer

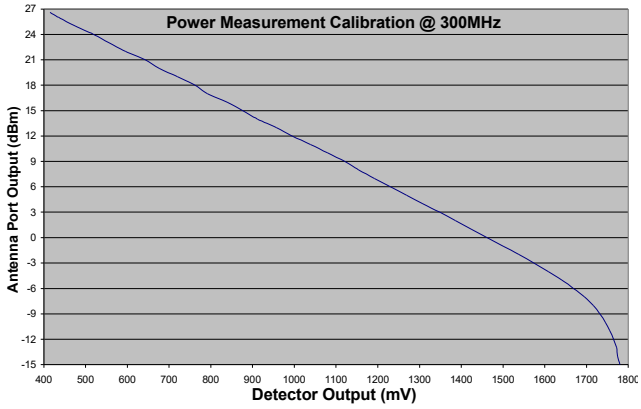
The local oscillators frequencies are frequency-locked onto a 10 MHz external or internal clock. The internal versus external frequency references are user-selected by software.

In order to use the external frequency reference, connect a 10 MHz sinewave, clipped sinewave or square wave to the SMA connector J9. Then select external frequency reference.

In order to use the internal frequency reference, either physically disconnect the external 10 MHz signal at SMA connector J9, or place the external input signal in high impedance mode. Then select internal frequency reference by software command from the ComBlock control center.

Power Measurement

Output power measurement is provided at the antenna port with an absolute accuracy (within calibration): ± 0.8dB over level, frequency and module.
Resolution: 0.1 dB.
Operational range: from –6 dBm to max output power.



Output power detection

Transmit Gain Control

The output power can be controlled in two ways: by adjusting the TX_I and TX_Q signal amplitude and/or by adjusting the TX_GAIN_CNTRL1 transmit IF gain control signal. The latter control is non-linear as shown below:

Recommendations

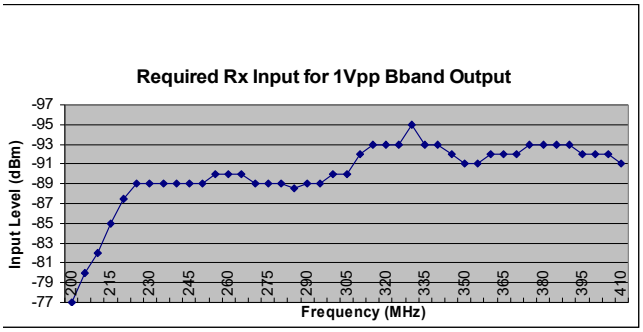
Because of the high receiver sensitivity, the following practices should be avoided:

- probing adjacent digital circuits with an oscilloscope probe (probe cable radiates and overloads receiver)
- connecting transmit/receive antenna close to the COM-3501 while operating without shield/metal case.

Performance

Receiver Sensitivity

The receiver sensitivity is defined here as the input power needed to reach a 1Vpp level at the baseband output when the receiver gain is set at its maximum value.

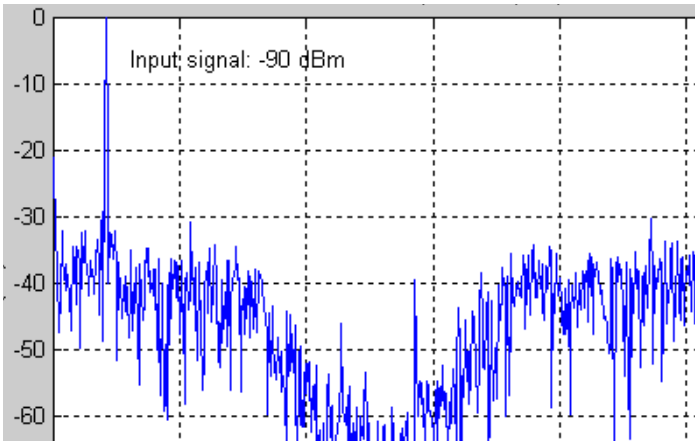


Receiver sensitivity

In practice, the receiver can operate at lower levels as demodulators generally do not require full-scale ADC conversion.

The receiver gain flatness is better than ± 1 dB in any 5 MHz band.

The spectrum analyzer capture below illustrates the signal to noise ratio at the baseband output after low-pass filtering (Option **–A** filter): the input signal is a -90 dBm pilot tone at 275.2 MHz while the receiver center frequency is 275 MHz. The overall SNR is 13 dB.



Baseband spectrum for-90 dBm input signal
Resolution bandwidth: 4.88 KHz.
512 ppt FFT span: +/- 1.25 MHz

RF Selectivity

-3 dB: 225 / 400 MHz
-20 dB: 158 / 548 M Hz
-40 dB: 103 / 843 MHz

IF Selectivity (915 MHz IF)

-3 dB: 15 MHz
-20 dB: 55 M Hz
-40 dB: 125 MHz

Internal Clock Reference

The internal crystal performance is as follows:

- tolerance: + 4 ppm average offset ± 5ppm typ. from board to board @25C
- temperature stability (-10C to +60C): ± 50 ppm max
- aging: ±5ppm/year max @25C

Baseband Receive Low Pass Filters

The purpose of this baseband low-pass filter is to reduce the signal bandwidth to prevent aliasing in a subsequent analog-to-digital conversion. A 4th order elliptic low-pass filter is used.

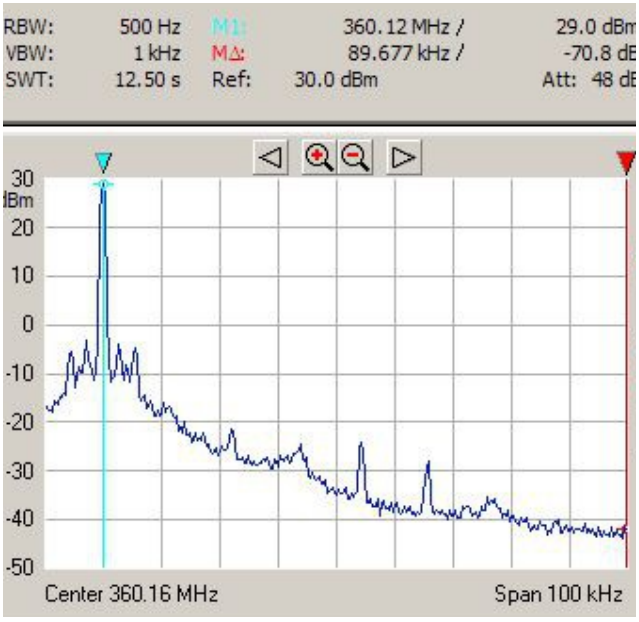
Option **–A** filter:

- one-sided -3 dB cutoff frequency of 780 KHz.
- [0-200 KHz] maximum in-band ripple <± 0. 2 dB.

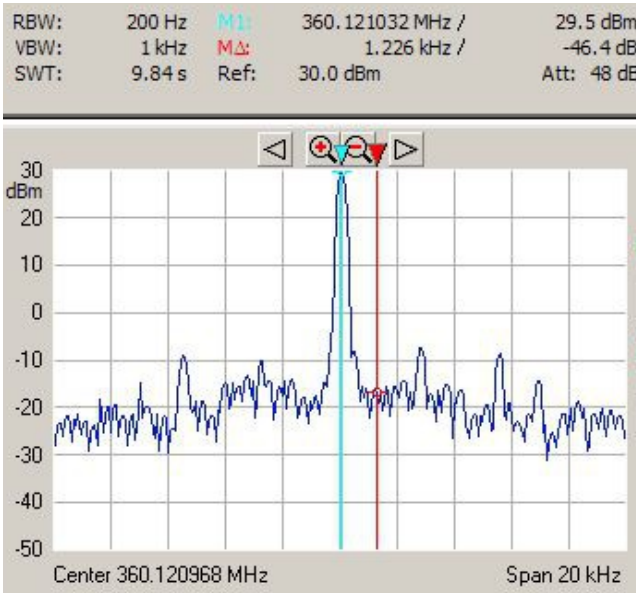
Phase Noise

The composite phase noise occurred during both frequency translations in the transmit or receive path is typically:

-68 dBc/Hz @ 1 KHz, typ. (internal ref.)
-60 dBc/Hz @ 1 KHz, typ. (external ref.)
-71 dBc/Hz @ 10 KHz, typ. (internal ref.)
-63 dBc/Hz @ 10 KHz, typ. (external ref.)
-95 dBc/Hz @ 100 KHz, typ.

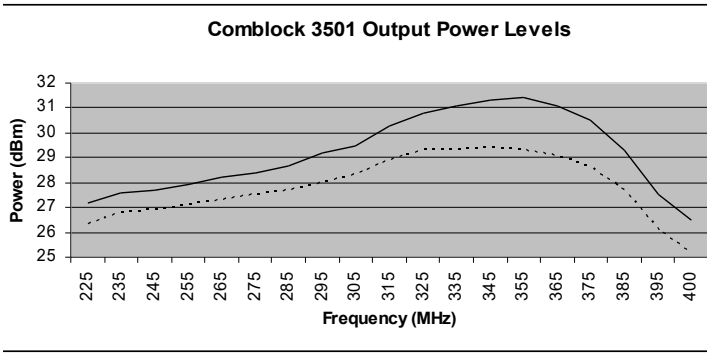


Phase noise. Internal 10 MHz frequency reference (COM-1200 – COM-3501 assembly, measured at the antenna port, maximum output power)

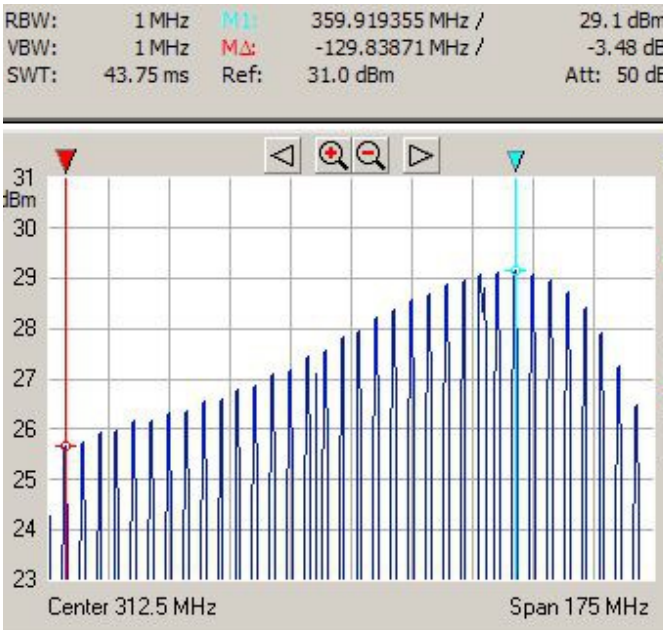


Close-in phase noise. Internal 10 MHz frequency reference. (COM-1200 – COM-3501 assembly, measured at the antenna port, maximum output power)

Transmitter Output Power



Output power at antenna port (dotted line) and power amplifier output port (solid line)

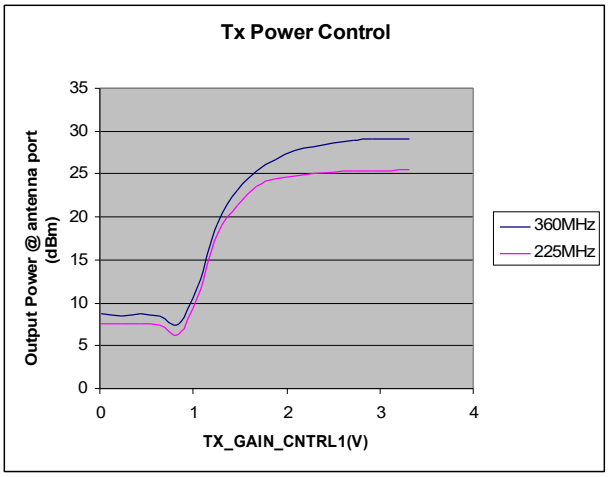


Transmitted power at antenna port 225 – 400 MHz by steps of 5 MHz. Spectrum analyzer capture. Baseband signal generated within the COM-1200 development platform.

Output power tolerance (from Board to board):
+/- 0.4 typ.
29.6 dBm +/- 0.4 dB at 360 MHz
26.0 dBm +/- 0.4 dB at 230 MHz

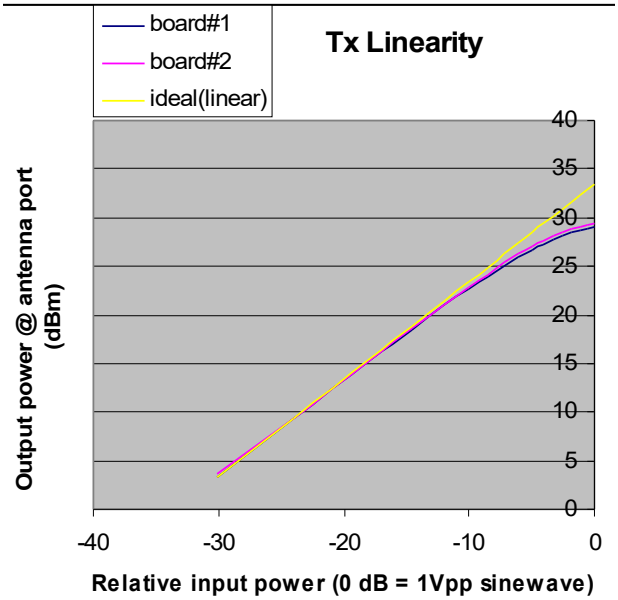
Transmitter Power Control

One method to control the output power is to use the TX_GAIN_CNTRL1 analog signal. At least 17 dB of power control is achievable, albeit in a non-linear manner. The IF pin diode attenuator attenuates both modulated signal and LO leakage. The actual output power for a given TX_GAIN_CNTRL1 level can be measured using the built-in output power measurement.

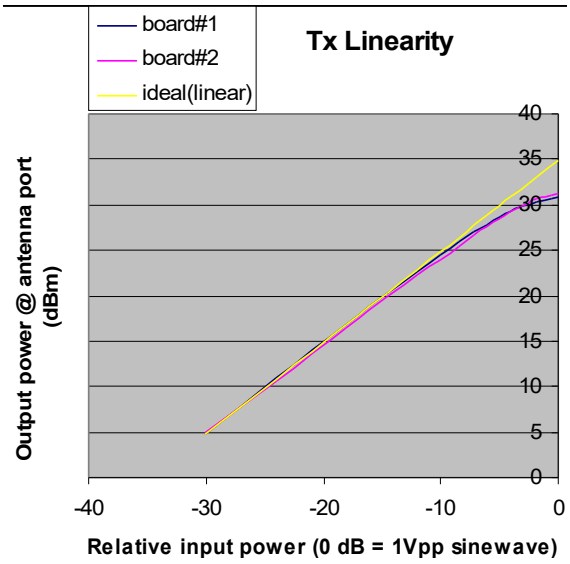


Typical transmitted gain control using TX_GAIN_CNTRL1. Power measured at antenna port.

Linearity



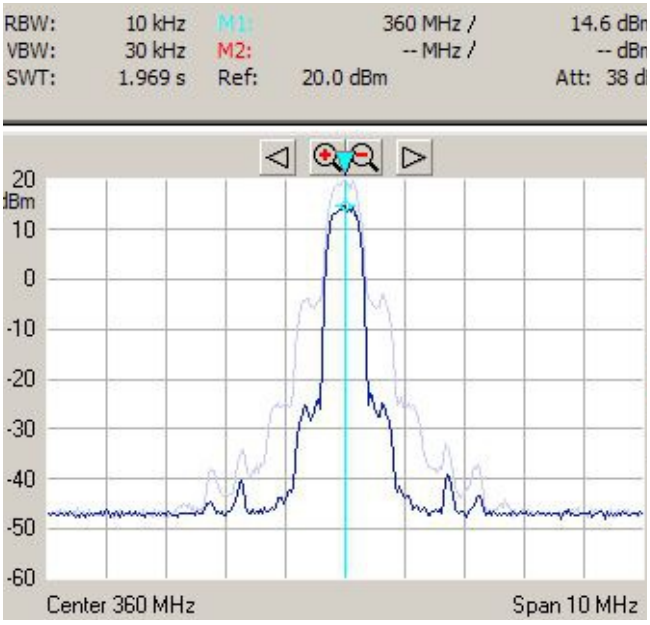
Transmitter linearity. Measured at the antenna port for a 360 MHz input sinewave (1Vpp maximum input amplitude).



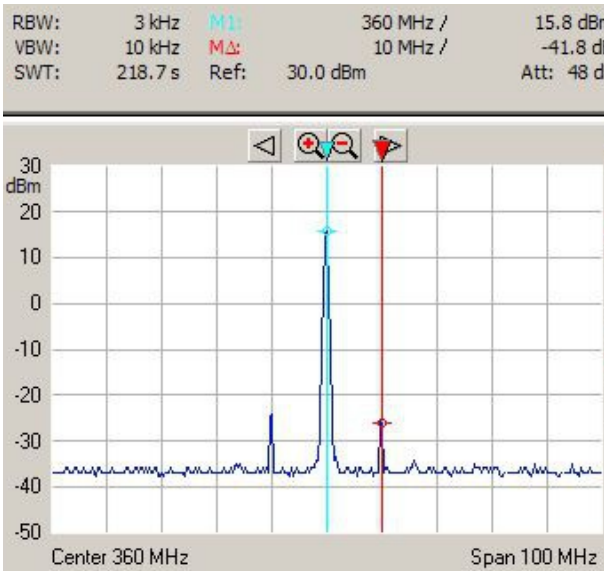
Transmitter linearity. Measured at the TX OUTPUT port for a 360 MHz input sinewave (1Vpp maximum input amplitude).

Modulated Spectrum Purity

A typical 500 Ksymbols/s QPSK modulated spectrum is shown below. The sidelobes re-growth depends on the output power backoff and the associated amplifier linearity.



Close-in transmitted output spectrum at TX_OUTPUT. 500KSymbols/s QPSK. 360 MHz.
Dark blue trace: 26.1 dBm
Light blue trace: maximum power. 31.6 dBm



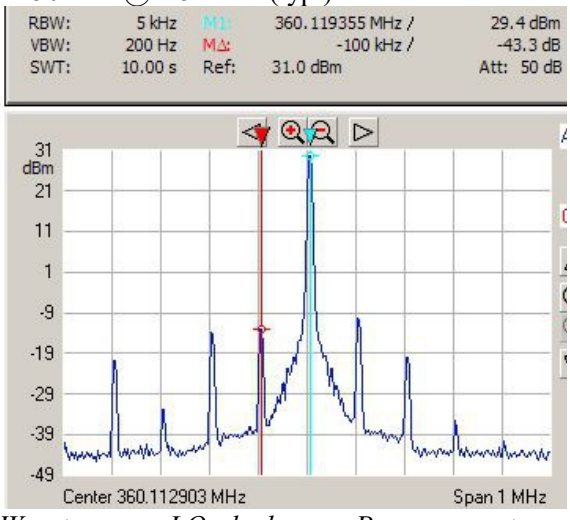
Out-of-band spectral purit. Transmitted output spectrum at TX_OUTPUT. 500KSymbols/s QPSK. 360 MHz. Maximum power. 31.6 dBm
10 MHz spectral lines at -58dBc.

2-Tone IMD

The third-order Inter-Modulation Product for a two-tone transmission is:
-20 dBc when each tone is 25.7 dBm
-30 dBc when each tone is 22.8 dBm.
The power is measured at the TX_OUTPUT port.

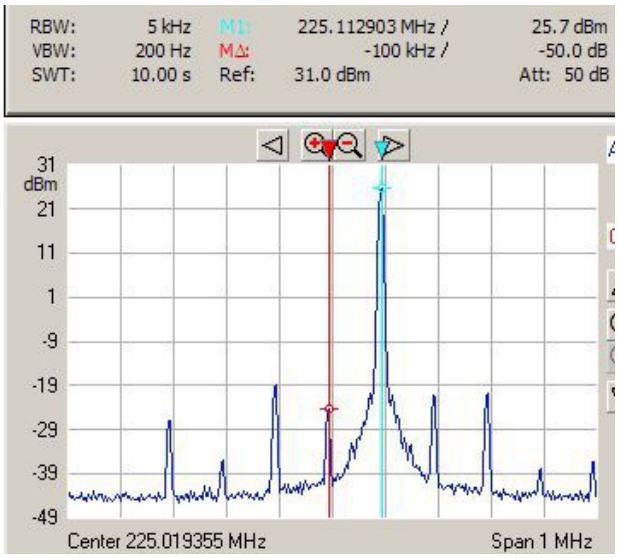
LO Leakage

< -40 dBc @360 MHz (worst case)
< -50 dBc @225 MHz (typ.).



Worst case LO leakage: Power spectrum at antenna port. 100 KHz single tone from COM-1200 development platform transmitted at 360 MHz,

maximum power. LO leakage: –43.3 dBc. Image rejection: –43.8 dBc.



Typical LO leakage: Power spectrum at antenna port. 100 KHz single tone from COM-1200 development platform transmitted at 225 MHz, maximum power. LO leakage: –50 dBc. Image rejection: –44.6 dBc.

Image Rejection

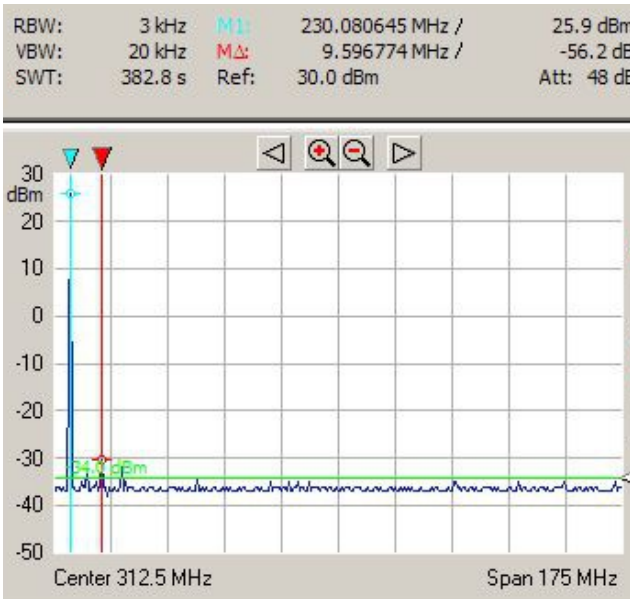
When tested in conjunction with the analog baseband signal generation in the COM-1200 platform:
-43 dBc typ. (100 KHz tone).

Emission Bandwidth

Tested in conjunction with COM-120X at 1.2 Msymbols/s QPSK.
-3 dB: ± 560 KHz
-20 dB: ± 930 KHz
-40 dB: ± 3.1 MHz
-60 dB: ± 18 MHz.

Transmitter Spurious Level

<-56 dBc in any 3 KHz band outside the modulation band.
< -65 dBc in any 3 KHz band outside +/- 13 MHz around the tuned RF center frequency.

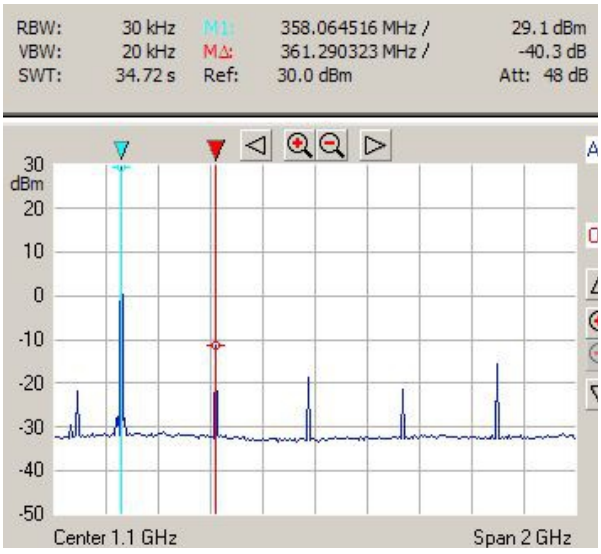


Spectrum Spurious Lines in 3 KHz resolution bandwidth. Green line is –60 dBc.

Harmonic Level

Out-of-band harmonics, measured at maximum output power

Frequency	Harmonics levels (dBc) max/min		
	2nd	3rd	4th
225 MHz	-12	-40/-42	<-60
300 MHz	-22	-50/-53	-48/-50
360 MHz	-40/<-60	-49	-51
400 MHz	-44/-49	-53/<-60	-48/<-60



Harmonics: 360 MHz pilot tone

Output Device

NEC NE5520379A

Other Specifications

Input noise figure: 6 dB typ.

Schematics

The board schematics are available on the ComBlock CD and on-line at http://www.comblock.com/download/com_3501schematics.zip

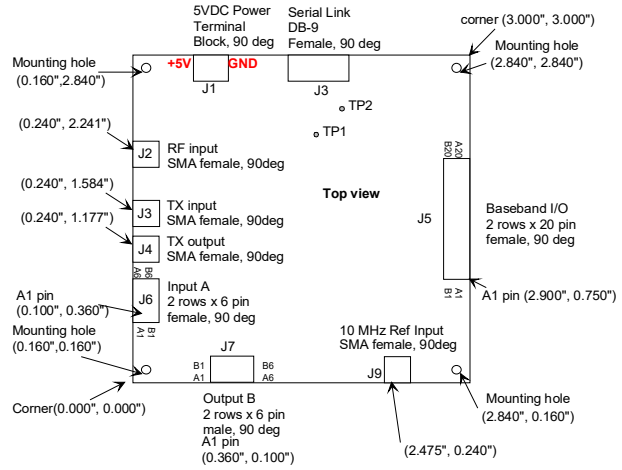
Do it yourself hardware modifications

By soldering and/desoldering a few surface-mount components, one can fairly easily implement the following modifications:

- bias the RX_I and RX_Q baseband output signals internally instead of the factory default external bias.

See the schematics for details.

Mechanical Interface



Mounting hole diameter: 0.125"

A1 pin height: 0.039"

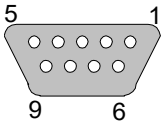
Maximum height 0.500"

Important: Please note that, on some COM-3501 units, the +5V and Ground leads at the terminal block may not be consistent with other ComBlock modules. Please follow the labeling on the board.

Pinout

Serial Link P3

The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.

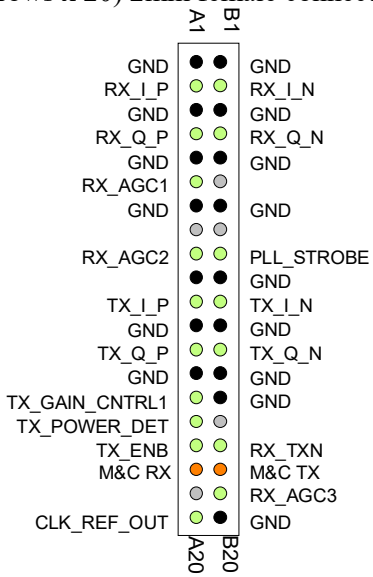


DB-9 Female

2 Transmit
3 Receive
5 Ground

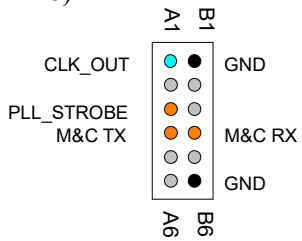
Baseband I/O Connector J5

40-pin (2 rows x 20) 2mm female connector.



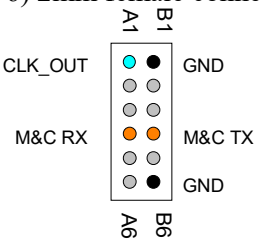
Connector J7

12-pin (2 rows x 6) 2mm male connector.



Connector J6

12-pin (2 rows x 6) 2mm female connector.



I/O Compatibility List

(not an exhaustive list)

I/O
COM-1700-A Low-power compact development Platform FPGA + ARM + DACs + ADCs + VGA + GbE LAN + USB2+ NAND + TCXO + RS422. Option –A.
COM-1705 Low-power compact PSK modem + Viterbi Convolutional FEC + IP router
COM-3504 Dual Analog <-> Digital Conversions [using 98-pin – 40 pin adapter COM-9109]
COM-1200 FPGA/VHDL development platform Xilinx Spartan3-1000 & Analog front-end

ComBlock Ordering Information

COM-3501**-A** UHF transceiver. Narrow-band applications.

ECCN: 5A991.b.1

MSS • 845 Quince Orchard Boulevard Ste N • Gaithersburg, Maryland 20878-1676 • U.S.A.
Telephone: (240) 631-1111
Facsimile: (240) 631-1676
E-mail: sales@comblock.com