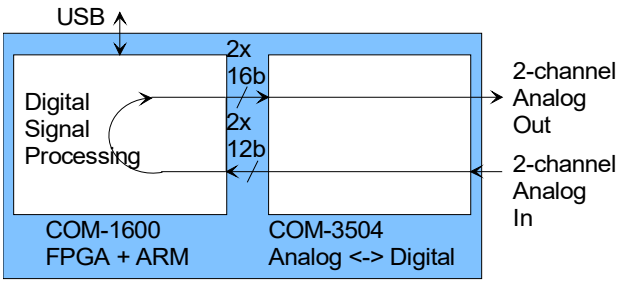
COM-3504 Dual Analog <-> Digital Conversions

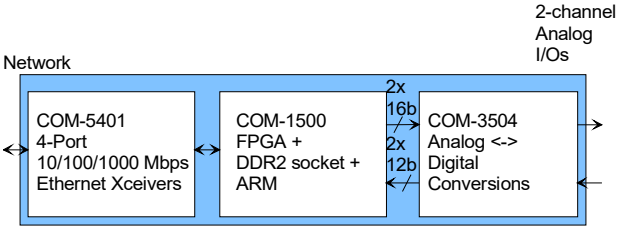
Key Features

- High-speed Digital to Analog and Analog-to-Digital Conversions:
  - Dual 16-bit 250 Msamples/s DACs
  - Dual 12-bit 150 Msamples/s ADCs
- Optimized for high-throughput interface with ComBlock FPGA/ARM/DDR2 development platforms.
- Output filtering for image rejection
- Monitoring & Control over USB.
- Only single +5V_{DC} supply required. Connectorized 3"x 3" module for ease of prototyping

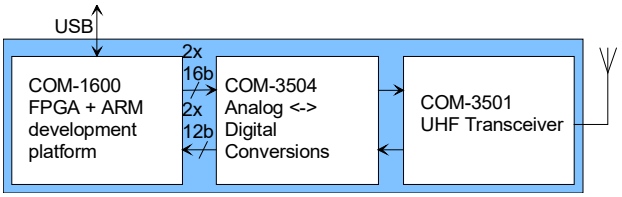
Typical Applications



Analog Signal Processing



Data acquisition / Arbitrary waveform generation



UHF Transceiver

For the latest data sheet, please refer to the **ComBlock** web site: comblock.com/com3504.html.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please referto comblock.com/product_list.html

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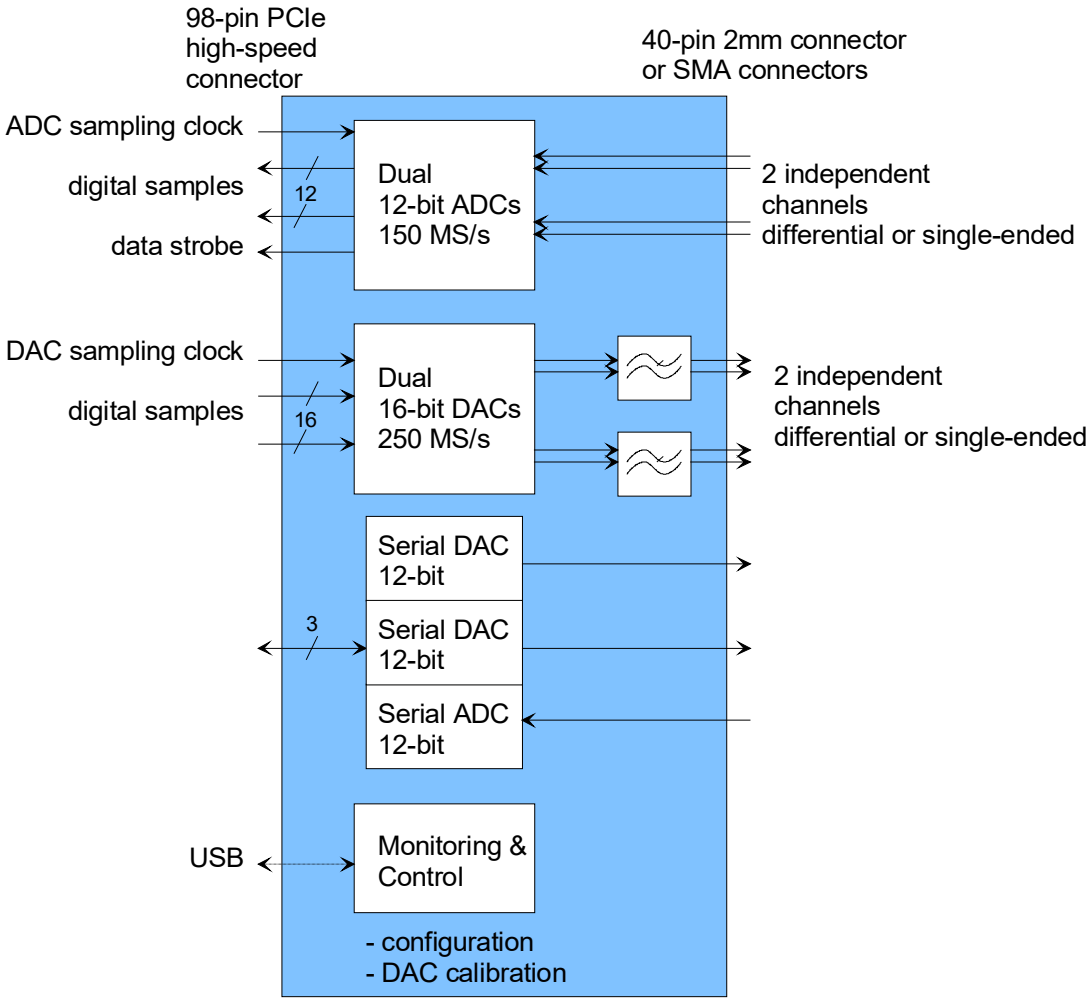
 Issued 3/29/2018

Block Diagram



Electrical Interface

Inputs / Outputs

40-pin Analog I/O	Definition
RX*x*_P / RX*x*_N	Channel*x* differential inputs. (_P for +, _N for -). 500 Ohm input impedance. Full 12-bit ADC conversion range: 1.25, 1.5, 1.75 or 2.0Vpp differential, software controlled (half on each RX*x*_P and RX*x*_N signal) . The signals are internally DC-biased at 0.9V with 1KOhm pull-up/pull-down resistors. Use AC or DC coupling. When using DC coupling, the recommended common mode voltage is 0.4 to 1.3V. Channel index *x* range: 1 to 2
TX*x*_P / TX*x*_N	Channel*x* differential outputs. (_P for +, _N for -). Full range: 2.0Vpp differential, half on each TX*x*_P and TX*x*_N signal. DC bias (common-mode voltage): $0.5V_{DC}$ Output impedance 100 Ohm differential, 50 Ohm single-ended. Channel index *x* range: 1 to 2
AUX_DAC1 AUX_DAC2	Analog output signals. Range: 0 – 3.3V. Typically used for controlling the gain of external RF front-end transmitter and/or receiver.
AUX_ADC	Analog input signals, multiplexed into two auxiliary ADCs. Range: 0 – 3.3V. Typically used for monitoring the levels of external RF front-end transmitter and/or receiver.
D_CNTRL(5:1)	Digital control signals. These signals

	are passed through between the 98-pin J6 connector and the 40-pin J5 connector. LVTTL 0 – 3.3V.
SMA Analog I/Os	**Definition**
RX*x*	Channel*x* single-ended ADC input. AC-coupled. Full-scale input: 1.25 Vpp. Maximum frequency: 200 MHz. Channel index *x* range: 1 to 2
TX*x*	Channel*x* single-ended DAC output. Full range 1.0Vpp. DC bias (common-mode voltage): $0.5V_{DC}$ Output impedance 50 Ohm. Channel index *x* range: 1 to 2

Digital Interface	Definition
ADC_CLKIN_P ADC_CLKIN_N	ADC sampling clock input. Sets the ADC sampling rate. LVCMOS/LVDS/LVPECL differential signal. 150 MHz max. 20 MHz min. In IF undersampling applications, the clock jitter must be kept significantly below 3ps. Index *x* is 1 or 2
ADC*x*_DOUT[13:2]	ADC*x* digital samples output. 12-bit unsigned (also known as "offset binary") format. The two least significant bits (1:0) are unused (reserved for future use). 0x0000: lowest output level 0x3FFF: highest output level 0x1FFF or 0x2000 ≈ center level CMOS 0 – 3.3V. Read at the rising edge of ADC*x*_SAMPLE_CLK_OUT.
ADC*x*_SAMPLE_CLK_OUT	Sampling clock output. Pinpoints the center of the ADC*x*_DOUT bits for reclocking at the receiving end. CMOS 0 – 3.3V.
DAC_CLKIN_P DAC_CLKIN_N	DAC sampling clock input. Sets the DAC sampling rate. 0-3.3V LVCMOS differential signal. 250 MHz max, no min.
DAC*x*_DIN[15:0]	DAC*x* digital samples input. 16-bit unsigned (also known as "offset binary") format. 0x0000: lowest input level 0xFFFF: highest input level 0x7FFF or 0x8000 ≈ center level CMOS 0 – 3.3V. Read at the rising edge of ADC*x*_SAMPLE_CLK_OUT.
AUX_SPI[5:1]	SPI interface to control the two auxiliary DACs and ADC in real-time. See AD5621 serial 12-bit DAC specifications. See AD7276 serial 12-bit ADC specifications.

Other Interfaces	Definition
USB Monitoring & Control	Mini-USB connector Type AB Full speed / Low Speed
Power Interface	4.75 – 5.5V_{DC}; Terminal block Power consumption is ~400mA

Absolute Maximum Ratings

Supply voltage	-8V min, +6.5V max
ADC input signals	-0.3V min, +2.1V max
Other input signals	-0.3V min, +3.6V max

Configuration

An entire ComBlock assembly comprising several ComBlock modules can be monitored and controlled centrally over a single connection with a host computer. Connection types include built-in types:

- USB (requires a mini-USB cable)

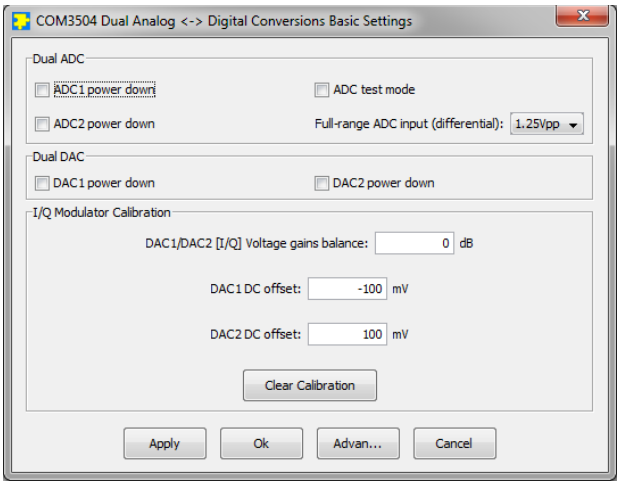
or connections via adjacent ComBlocks:

- USB
- TCP-IP/LAN,
- Asynchronous serial (DB9)
- PC Card (CardBus, PCMCIA).

The module configuration is stored in non-volatile memory.

Configuration (Basic)

The easiest way to configure the COM-3504 is to use the **ComBlock Control Center** software supplied with the module on CD. In the ComBlock Control Center window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-3504 module to be configured and click the *Settings* button to display the *Basic Settings* window shown below.



Basic Settings Window

Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

The module configuration parameters are stored in non-volatile memory. All control registers are read/write. Undefined control registers or register bits are for backward software compatibility and/or future use. They are ignored in the current firmware version.

High-speed dual ADC configuration	
Parameters	**Configuration**
ADC1 Power-down	Minimize ADC1 power consumption. 0 = normal operation 1 = ADC1 power down REG0(0)
ADC2 Power-down	Minimize ADC2 power consumption. 0 = normal operation 1 = ADC2 power down REG0(1)
ADCs Output Test Mode	0 = normal operation 1 = generate alternating checkerboard pattern at the ADCs outputs. The ADCs inputs are ignored while in test mode. REG0(2)
ADC input dynamic range	Select input dynamic range for full range ADC output: 00 = 1.25Vpp differential 01 = 1.50Vpp differential 10 = 1.75Vpp differential 11 = 2.00Vpp differential Example1: One single-ended 1.25Vpp signal at the SMA input connector -> select 00 Example 2: Two differential signals, 1Vpp each (2Vpp differential) at the 40 pin connector -> select 11 REG0(5:4)

ADC sampling clock delay adjustmentS	Delay the ADCx_SAMPLE_CLK_OUT signals by 2500 ps × register value/31. The purpose is to center the rising edge of the sampling clock at the very center of the ADC bits. REG1(4:0) ADC1__SAMPLE_CLK_OUT REG2(4:0) ADC2__SAMPLE_CLK_OUT
Direct access to AD9627 control registers (Advanced) See AD9627 specifications	
ADC control register data	Lets the user write a specific byte to the AD9627 address specified below. REG7: AD9627 command data
ADC control register address	AD9627 control register address. REG8: address bits 7:0 REG9(1): address bit 8
Enable write to AD9627 control register.	0 = write disabled 1 = write enabled The command is sent to the AD9627 upon (re-)writing to this control register. REG9(7)
High-speed dual DAC configuration	
Parameters	**Configuration**
DAC1 Power-down	Minimize DAC1 power consumption. 0 = normal operation 1 = DAC1 power down REG10(0)
DAC2 Power-down	Minimize DAC2 power consumption. 0 = normal operation 1 = DAC2 power down REG10(1)
Dual DAC fine output calibration	
DAC1 gain	DAC1 current/voltage gain. Nominal value for 20mA / 1Vpp output is 0x1F9 REG11(7:0): LSB REG12(2:0): MSbs
DAC1 DC bias correction	Adjusts the DAC1 output so as to minimize carrier feedthrough (leakage) in a subsequent IQ modulator. This calibration should be performed once in tandem with the IQ modulator. Corrections are typically less than ± 5mV. 10-bit unsigned corresponds to 0x033: 5 mV correction 0x000: 0.0 mV correction REG13(7:0): LSB REG14(2:0): MSbs
DAC1 DC bias direction	0 = current sourced (nominal) 1 = current sinked REG14(6)
DAC1 DC bias side	Correction sign: 0 = P side corrected 1 =N side corrected REG14(7)
DAC2 gain	DAC2 current/voltage gain. Nominal value for 20mA / 1Vpp output is 0x1F9 REG15(7:0): LSB REG16(2:0): MSbs
DAC2 DC bias correction	Adjusts the DAC2 output 10-bit unsigned corresponds to Same format as DAC1 DC bias correction. REG17(7:0): LSB REG18(2:0): MSbs
DAC2 DC bias direction	0 = current sourced 1 = current sinked REG18(6)
DAC2 DC bias side	0 = P side corrected 1 =N side corrected REG18(7)

Monitoring

Monitoring the status of the COM-3504 is performed by viewing the S*tatus* window in ComBlock Control Center. All register values are displayed in hexadecimal, but other formats are displayed by hovering over the hex value with the cursor.

Custom applications can monitor module status again, by using the ComBlock API.

Parameters	**Monitoring**
Internal Power Supply Fault *(see schematics for reference)*	0 = Normal Operation 1 = Fault Condition SREG0(0): D_+4.8V SREG0(1): D_+3.3V SREG0(2): DACA_+3.3V SREG0(3): D_+2.0V SREG0(4): DAC_+1.8V

Operations

Clock Distribution

Independent sampling clocks are supplied externally for the dual ADCs and dual DACs as the COM-3504 does not include any oscillator.

AD9627 ADC Configuration

The AD9627 is an intelligent ADC with many control and monitoring features. To simplify the user task, this board's software is written with three levels of controls:

a) Simple configuration of a few key parameters in control registers REG0/1/2.

b) Default setting of the other ADC parameters to the following default values:

- Output type: CMOS
- Output format: unsigned (offset binary)
- Duty cycle stabilizer enabled
- ADC outputs enabled
- Output clock polarity: rising edge
- ADC_CLKIN frequency division: 1:1
- VREF = 1V (for 2Vpp differential input)

c) Indirect access to **all** AD9627 features through the ComBlock API, using control registers REG1/2/3. For details, see www.analog.com/static/imported-files/data_sheets/AD9627.pdf

A software reset is sent to the ADC at power-up or following a user-generated @xxxRST command.

AD9747 DAC Configuration

The AD9747 is an intelligent ADC with many control and monitoring features. To simplify the user task, this board's software is written with three levels of controls:

a) Simple configuration of a few key parameters in control registers REG10/11.

b) Default setting of the other DAC parameters to the following default values:

- Dual-port mode
- Input format: unsigned
- DAC1 Gain: 20 mA full scale current
- DAC2 Gain: 20 mA full-scale current

c) Indirect access to **all** AD9747 features through the ComBlock API, using control registers REG5/6. For details, see www.analog.com/static/imported-files/data_sheets/AD9741_9743_9745_9746_9747.pdf

A software reset is sent to the DAC at power-up or following a user-generated @xxxRST command.

DACs Calibration

The dual DACs can be connected directly to an IQ modulator. In this case, minor impairments can cause large changes in Error Vector Magnitude (EVM) performance. The impairments are primarily:

- DC offset
- I/Q gain imbalance
- Phase error

This module includes features to calibrate out the first two impairments. The calibration procedure is a time-consuming iterative and frequency-dependent process that can only be justified if the out-of-the-box carrier feedthrough (LO leakage) and sideband suppression are not good enough for one's application. The calibration procedure is described in details in Analog Devices application note AN-1039. It is to be applied to each COM-3504 + IQ modulator assembly once (factory calibration).

This module is not designed to affect the phase error, which limits its ability to reduce sideband suppression [sideband suppression requires perfect phase AND I/Q gain balance].

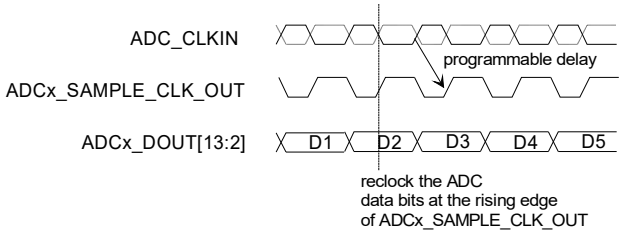
Timing

ADC Timing

The user supplies the ADC sampling clock ADC_CLK_IN in the form of a differential signal.

The ADC output samples are sent within t_{PD} = [2.2 – 6.4ns] after the rising edge of the received ADC_CLK_IN.

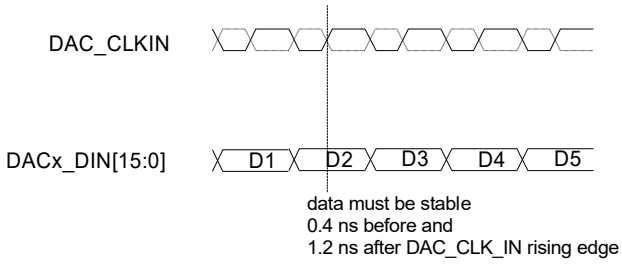
ADC*x*_SAMPLE_CLK_OUT is useful to reclock the ADC output samples at the receiving end (FPGA for example). The user can position the rising edge of the sampling clock (using control register REG1) to a window where the data is stable.



DAC Timing

The user supplies the sampling clock DAC_CLK_IN in the form of a differential LVDS signal.

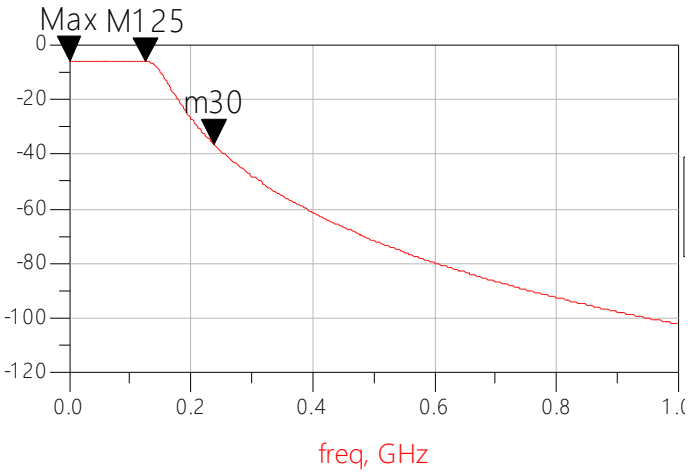
The user must supply the DAC data bits in a timely manner such that the DAC bits are stable within a [-0.4ns - +1.2ns] window around the rising edge of the sampling clock DAC_CLK_IN (when seen at the DAC).



Performance

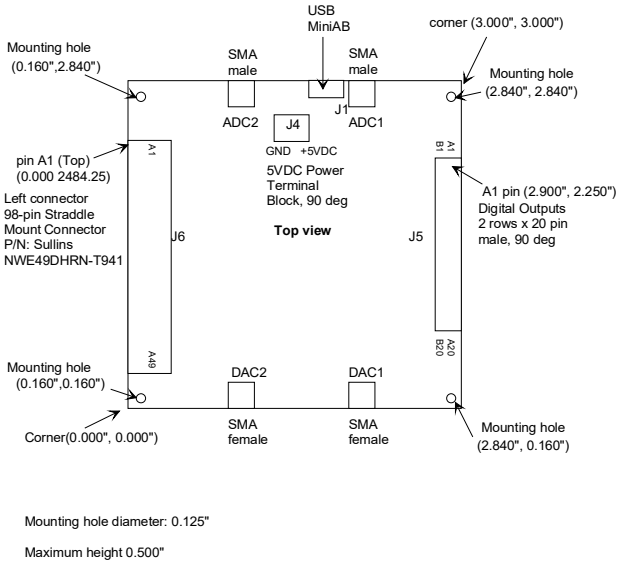
Low Pass Filter

Each D/A Converter is followed by a low-pass filter to suppress clock spectral spurious lines and aliasing. The filter response is as follows:



Passband: 0 – 125 MHz
Passband gain flatness: better than ±0.3 dB in any 100 MHz sub-band.
Rejection at 237 MHz: 30 dB
Out of band spectral spurious lines: < -84dBc in any 3 KHz band (TBC).

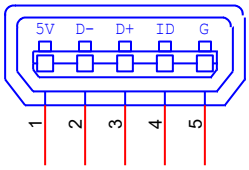
Mechanical Interface



Pinout

Mini USB Connector, J1

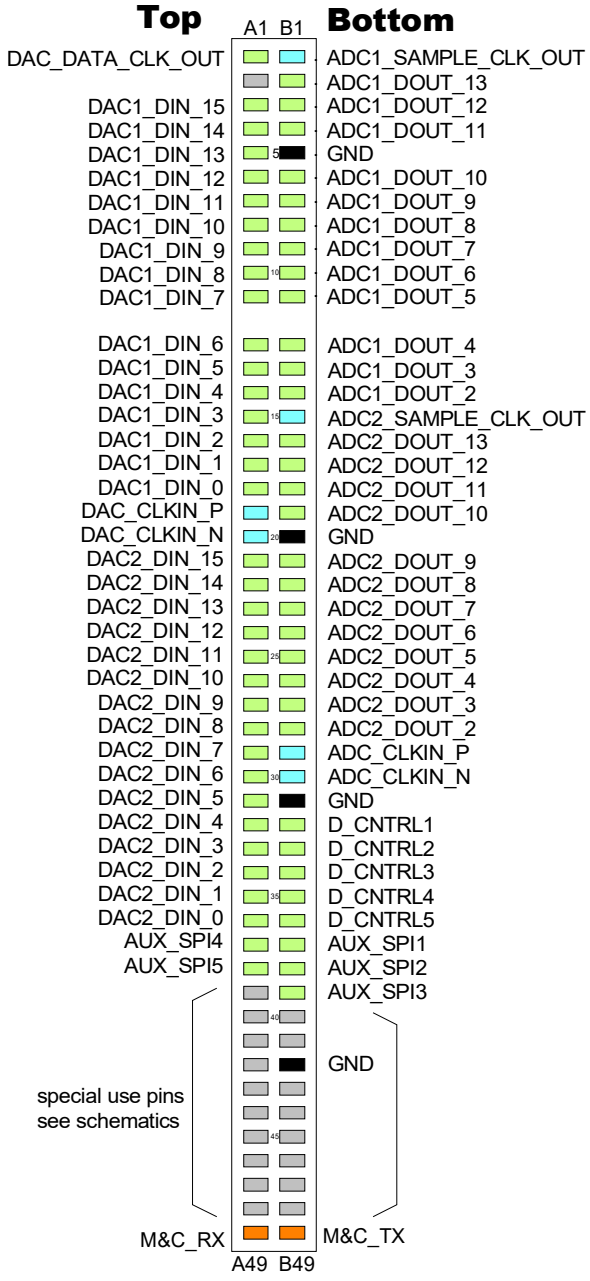
The COM-3504 is a USB device with a mini type AB connector. (G = GND)



Digital I/O Connector, J6

98-pin Female Connector

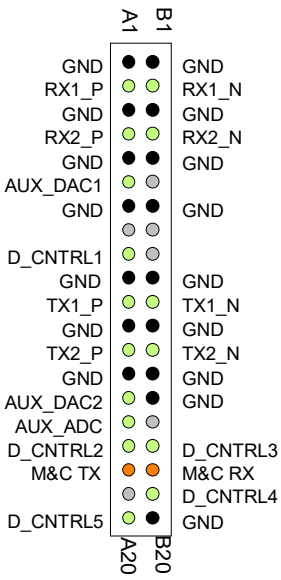
This connector is designed for a direct connection to FPGA-based ComBlocks (COM-18xx)



Analog Differential I/O Connector, J5

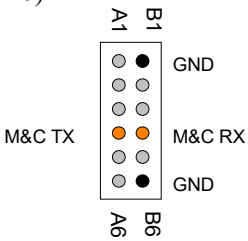
40-pin (2 rows x 20) 2mm male connector.

This connector is designed for a direct connection to the COM-350x transceivers.



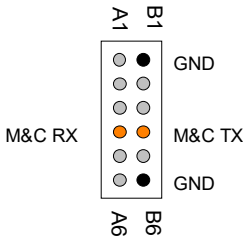
M&C Connector J9

12-pin (2 rows x 6) 2mm male connector.



M&C Connector J10

12-pin (2 rows x 6) 2mm female connector.



I/O Compatibility List

(not an exhaustive list)

98-pin high-speed connector
COM-1800 FPGA (Artix7 –100) + ARM + DDR3 socket + GbE LAN + USB + NAND development platform
40-pin Connector
COM-3501 UHF Transceiver
COM-3505 Dual-band 2.4/5GHz transceiver (single channel)
COM-3506 [400MHz-3GHz] customizable transceiver
2 SMA Rx Connectors
COM-2001 Dual DAC, for test purposes

ComBlock Ordering Information

COM-3504
DUAL ANALOG <-> DIGITAL CONVERSIONS

ECCN: 3A001.a.5

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