COM-4005 CELLULAR BAND [800 -1000 MHz] QUADRATURE RF MODULATOR

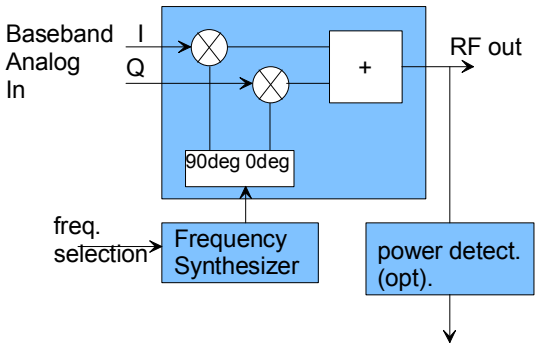
Key Features

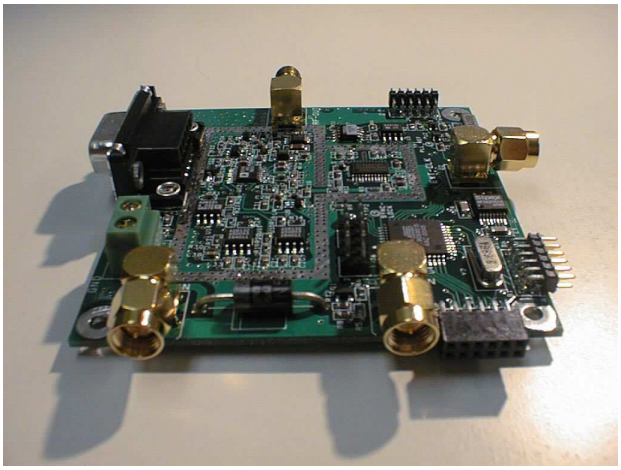
- Quadrature modulator 800 – 1000 MHz center frequency.
- Low-noise frequency synthesizer can be tuned over entire range by steps of 100, 31.25 or 25 KHz.
- Optional output power measurement has 0.1 dB resolution.
- 8 preset frequencies for fast (<2ms) local oscillator frequency tuning.
- Output power can be controlled over 20 dB range using 10-bit control words. Non-linear scale.
- Selectable internal / external 10 MHz frequency reference for the frequency synthesizer.
- Single 5V supply
- Connectorized 3"x 3" module for ease of prototyping. SMA connectors.

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com4005.pdf.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .

Block Diagram




(shown without shield)

Electrical Interface

Inputs / Outputs

Input Module Interface	Definition
ANALOG_I_IN	Modulated input signal, analog, baseband, real (I) axis. 1Vpp max. Positive DC bias is required so that signal is within the [0.3 – 3.0V] rails. The DC bias is removed internally by a low-pass filter with cutoff bandwidth < 2 Hz. SMA male connector.
ANALOG_Q_IN	Modulated input signal, analog, baseband, imaginary (Q) axis. 1Vpp max. Same electrical characteristics as above.
EXT_REF_CLK	External 10 MHz frequency reference for frequency synthesis. Sinewave, clipped sinewave or squarewave. Minimum level 0.5Vpp. Maximum level: 3.3Vpp. Use square wave for best phase noise performances.

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 Issued 11/25/2010

Analog Output Signals	Definition
RF_OUT	Modulated RF output. 800 – 1000MHz Maximum output level: -3 dBm. Impedance: 50 Ohms. SMA female connector
Control Lines	**Definition**
ENABLE	Low-voltage TTL input control. Used to turn the modulator on/off. Level signal: 3.3V = ON, 0V = OFF Response time is typically in the range 5 10 µsec On/Off rejection = 15 (TBC) dB typ. Connector J1 Pin B3. This control signal is enabled only when REG6 bit 1 = '1'.
PLL_STROBE	Low-voltage (3.3V / 0V) TTL input control. Used to increment the modulo- N_{freq} frequency pointer (where N_{freq} is defined in Register 35) RF frequency 0 ->RF frequency 1 ->RF frequency 2 ->RF frequency 0 > etc… Rising edge triggered. Minimum pulse width: 10 µsec. Connector J1 Pin A3.
Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is 250mA max.

Important: digital I/O signals are 0-3.3V LVTTL. Inputs are NOT 5V tolerant!

Configuration

Complete assemblies can be monitored and controlled centrally over a single asynchronous serial connection or, when available through adjacent ComBlocks, LAN/TCP-IP , USB, or CardBus connection.

The module configuration is stored in non-volatile memory.

The COM-4005 ignores any M&C message received within 1 ms of a transition on the PLL_STROBE and ENABLE signals.

Programmers developing custom applications (using the ComBlock API instead of the supplied ComBlock control center graphical user interface) should know that frequency changes are enacted upon (re-)writing to the last register (REG35).

Parameters	Configuration
RF frequency 0	Preselected frequency 0. Range 800 MHz to 1000 MHz, by steps of 100, 31.25 or 25 KHz, expressed in Hz. REG0: bits 7:0 (LSB) REG1: bits 15:8 REG2: bits 23:16 REG3: bits 31:24 (MSB)
Gain control	10-bit control. Non-linear scale. Zero is lowest power. AGC range : 22 dB @ 800 MHz (typ.) 26 dB @ 1000 MHz (typ.) REG4: bit 7-0 (LSB) REG5: bit 1-0 (MSB)
External/Internal frequency reference	0 = internal 1 = external. REG6: bit 0
External controls enabled/disabled	Enable or disable the PLL_STROBE and output ENABLE external controls on the J1 connector. 0 = external controls disabled 1 = external controls enabled REG6: bit 1
Modulator on/off	0 = modulator off 1 = modulator on Note: external control ENABLE may override this register. REG6: bit 2
Step size selection	Chose between 100, 31.25 or 25 KHz step size. 00 = 100 KHz step 01 = 31.25 KHz step 10 = 25 KHz step REG6 bits 4-3.
Frequency selection	Use to switch local oscillator frequency among preselected values. Note: the external PLL_STROBE control may override this selection. Range 0 through 7 REG6 bits 7-5.
RF frequency 1	Preselected frequency 1. Same format as RF frequency 0. REG7: bit 7:0 (LSB) REG8: bit 15:8

	REG9: bit 23:16 REG10: bit 31:24 (MSB)
RF frequency 2	Preselected frequency 2. Same format as RF frequency 0. REG11: bit 7:0 (LSB) REG12: bit 15:8 REG13: bit 23:16 REG14: bit 31:24 (MSB)
RF frequency 3	Preselected frequency 3. Same format as RF frequency 0. REG15: bit 7:0 (LSB) REG16: bit 15:8 REG17: bit 23:16 REG18: bit 31:24 (MSB)
RF frequency 4	Preselected frequency 4. Same format as RF frequency 0. REG19: bit 7:0 (LSB) REG20: bit 15:8 REG21: bit 23:16 REG22: bit 31:24 (MSB)
RF frequency 5	Preselected frequency 5. Same format as RF frequency 0. REG23: bit 7:0 (LSB) REG24: bit 15:8 REG25: bit 23:16 REG26: bit 31:24 (MSB)
RF frequency 6	Preselected frequency 6. Same format as RF frequency 0. REG27: bit 7:0 (LSB) REG28: bit 15:8 REG29: bit 23:16 REG30: bit 31:24 (MSB)
RF frequency 7	Preselected frequency 7. Same format as RF frequency 0. REG31: bit 7:0 (LSB) REG32: bit 15:8 REG33: bit 23:16 REG34: bit 31:24 (MSB)
Number of RF frequencies N_{freq} in the scanning list	Each time a PLL_STROBE pulse is received, the frequency pointer increments modulo N_{freq}. N_{freq} is in the range 1 – 8. REG35: bit 7:0.

Baseline configurations can be found at www.comblock.com/tsbasic_settings.htm and imported into the ComBlock assembly using the ComBlock Control Center File | Import menu.

Monitoring (via Serial Link / LAN)

Parameters	Monitoring
Power measurement (option -D)	10-bit number. The higher the number, the lower the power. The power measurement linearity is shown below. SREG36 bits 7-0: bit 7-0 (LSB)
	SREG37 bits 1-0: bits 9-8 (MSB)
PLL lock status	A persistent '1' indicates that the frequency synthesizer is locked to the frequency reference. SREG38 bit 0.

Operations

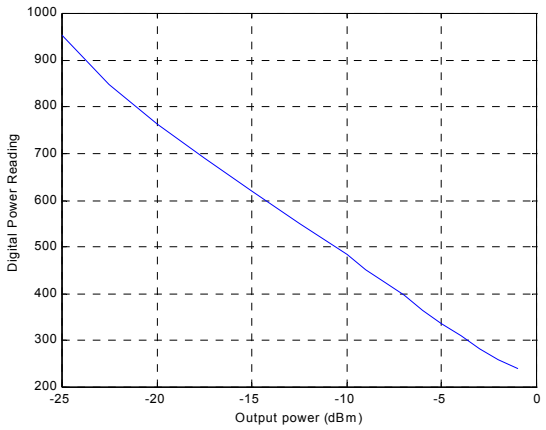
Internal vs External Frequency Reference

In order to use the external frequency reference, select external frequency reference by software command from the ComBlock control center. Then connect a 10 MHz sinewave, clipped sinewave or square wave to the SMA connector J2. Switching from internal to external frequency reference generally requires a power cycle (turn power off then on again).

In order to use the internal frequency reference, either physically disconnect the external 10 MHz signal at SMA connector J2, or place the external input signal in high impedance mode. Then select internal frequency reference by software command from the ComBlock control center.

Power Measurement (Option -B)

Output power measurement is provided as an option (-B). Output power measured with +/- 0.2 dB accuracy over a range from –25 dBm to the maximum output power. The 10-bit measurement linarity is shown below [800 MHz output signal]:



Test Points

Test points are provided for easy access by an oscilloscope probe.

Test Point	Definition
TP1	Internal / External reference clock
TP2	Frequency synthesizer PLL lock status. Active low: '0' when locked. Note: do not connect any long test cable to this test point as it may inject noise into the RF PLL.

Performance

Quadrature phase error: 1. deg rms. typ
I/Q amplitude balance error: 0.2 dB.typ
ON/OFF rejection: > 80 dB

LO leakage (at output, maximum AGC gain, +20 KHz input signal):

-36 dBm @ 800 MHz, typ.
-37 dBm @ 1.00 GHz, typ.

Sideband suppression (at output, maximum AGC gain, + 20KHz input signal):

-42 dBc @ 800 MHz, typ.
-51 dBc @ 1.0 GHz, typ.

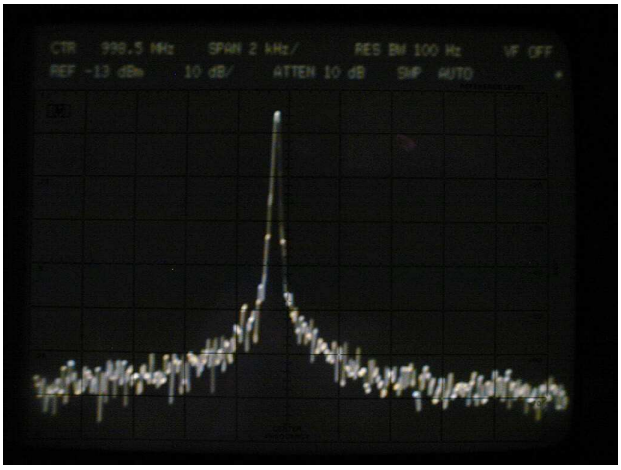
Out-of-band spurious spectral lines: < -60 dBc (Exception: a –47dBc spectral line may be present at 120 MHz from the center frequency).

Power detection (option -B) resolution: 0.1 dB.

Phase noise:

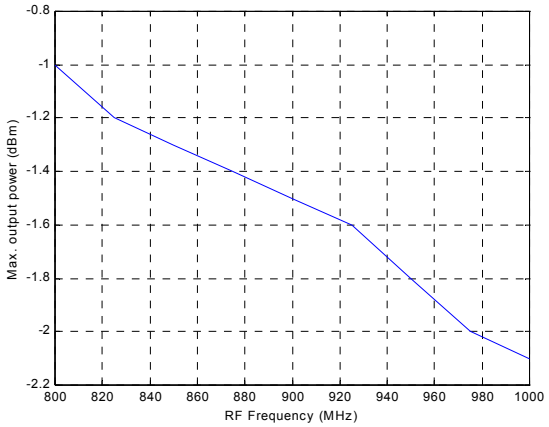
<-50 dBc @ 100 Hz
< -65 dBc @ 1 KHz
< -82 dBc @ 10 KHz
< -110 dBc @ 100 KHz

The phase noise measurements are similar when internal or external frequency references are used.



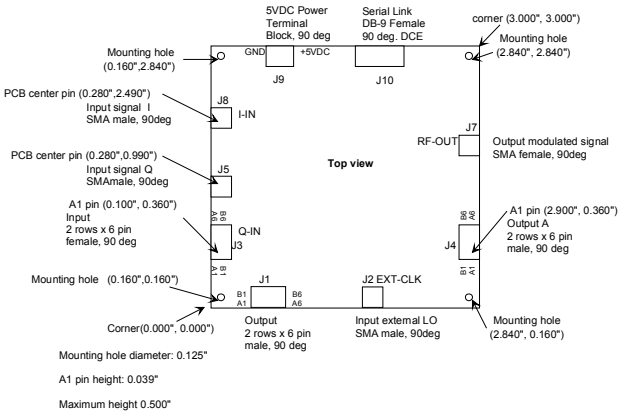
Phase noise measurement: internal reference clock 2 KHz/div, 10 dB/div. 998.5 MHz center freq., 100 Hz resolution bandwidth.

Maximum output power level (for a 1Vpp input):



Minimum output power: -25 dBm (800-1000 MHz).

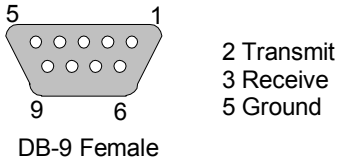
Mechanical Interface



Pinout

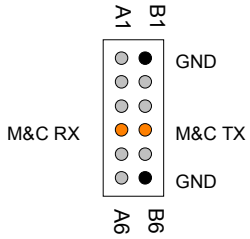
Serial Link J10

The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.



Input Connector J3

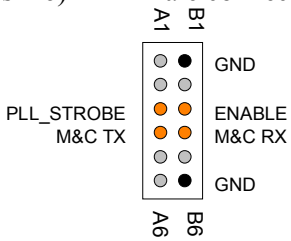
12-pin (2 rows x 6) 2mm female connector.



This module is is designed for direct connection to the COM-2001 baseband digital-to-analog conversion module.

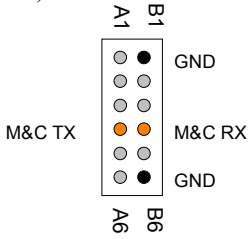
Connector J1

12-pin (2 rows x 6) 2mm male connector.



Output Connector J4

12-pin (2 rows x 6) 2mm male connector.



This connector is to forward monitoring and control signals to subsequent analog modules.

I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-2001 Dual D/A converter (baseband)	COM-3005 Cellular band [0.8 – 1GHz] receiver (back to back with RF attenuation in-between)
COM-3504 Dual Analog <-> Digital Conversions	

Configuration Management

This specification is to be used in conjunction with Atmel microcontroller software revision 4.

ComBlock Ordering Information

COM-4005-C	CELLULAR BAND [800 – 1000 MHz] QUADRATURE MODULATOR
COM-4005-D	CELLULAR BAND [800 -1000 MHz] QUADRATURE MODULATOR W/ OUTPUT POWER MEASUREMENT.

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