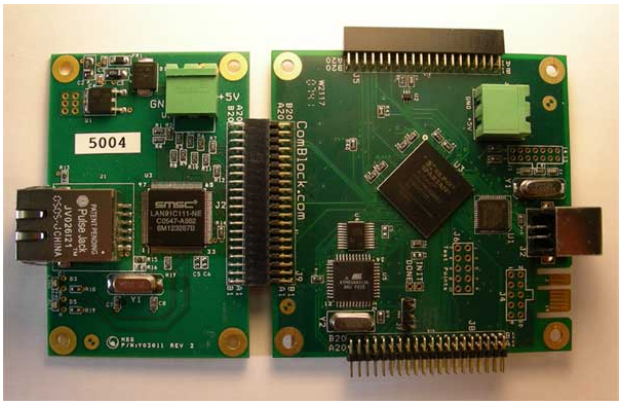
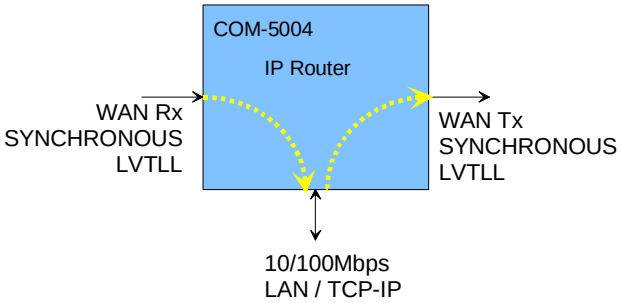
COM-5004 IP ROUTER

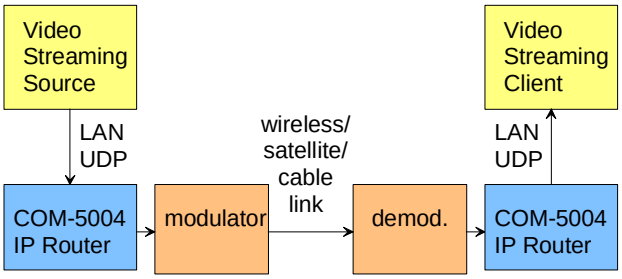


Key Features

- IP router acts as gateway between a 10/100Mbps LAN and a digital clock-synchronous link (WAN)
- Typical application is to bridge islands of IP-based networks through fixed data rate satellite / wireless / cable modems:
  - UDP video streaming
  - IP datacasting
  - Two-way IP communications
- IP packets can be transmitted as 8-bit parallel or 1-bit serial streams
- A CRC is attached to each transmitted IP packet for error detection at the receiving end
- 1-bit serial streams are HDLC encoded and scrambled
- IP offload engine (IP routing implemented in FPGA/VHDL) for maximum throughput performance
- Complies with IPv4 routers specifications RFC1812
- Single 5V supply. Standard 40 pin 2mm dual row connectors (right, left)



Typical Application



One-way video streaming over UDP

For the latest data sheet, please refer to the **ComBlock** web site: comblock.com/download/com5004.pdf.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .

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Interfaces

Input Signals	Definition
DATA_IN[7:0]	Input signal. The input width is can be 1-bit or 8-bit under user control. See control register REG20. Signals are pulled-down. LVTTL 0 – 3.3V
SAMPLE_CLK_IN	Input signal sampling clock. One CLK_IN-wide pulse. Read the input signal at the rising edge of CLK_IN when SAMPLE_CLK_IN = '1'. Samples can be consecutive. For example, SAMPLE_CLK_IN can be fixed at '1' to indicate that new input samples are provided once per CLK_IN clock period. Signal is pulled-up. LVTTL 0 – 3.3V
SAMPLE_CLK_IN _REQ	Input flow control signal (output). '1' indicates that the COM-5004 is ready to accept DATA_IN input samples into its input elastic buffer. LVTTL 0 – 3.3V. Signal is pulled-down.
CLK_IN	Input reference clock for synchronous I/O. DATA_IN and SAMPLE_CLK_IN are read at the rising edge of CLK_IN. Maximum frequency: 40 MHz. LVTTL 0 – 3.3V

Output Signals	Definition
DATA_OUT[7:0]	LVTTL 0 – 3.3V output signal. The output width is can be 1-bit or 8-bit under user control. See control register REG21
SAMPLE_CLK_OUT	LVTTL 0 – 3.3V output signal sampling clock. One CLK_OUT-wide pulse. Read the output signal at the rising edge of CLK_OUT when SAMPLE_CLK_OUT = '1'.
SAMPLE_CLK_OUT_REQ	Output flow control signal (input). '1' asks the COM-5004 to send DATA_OUT output data to the next module. LVTTL 0 – 3.3V. Signal is pulled-down.
CLK_OUT	LVTTL 0 – 3.3V 40 MHz output reference clock. (from internal oscillator).
EXT_TRIGGER_OUT	25 ns pulse triggered by software command. See command register REG22. Helpful in triggering events such as COM-8001 start of data acquisition. LVTTL 0 – 3.3V

Other Interfaces	Definition
LAN	4 wire. 10Base-T/100Base-TX. RJ45 connector. NIC wiring. Use standard category 5 cable for connection to a Hub. Use crossover cable for connection to a host computer.
USB	USB 2.0 Use USB 2.0 approved cable for connection to a host computer. Maximum recommended cable length is 3'. The USB connection is needed only for a one-time initial IP configuration.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is typically 450mA.

Initial Configuration

Before the first use, the router must be assigned a static IP address over USB or through adjacent ComBlocks by following the one-time procedure below:

a) Shorten the BOOT pin with the adjacent GND pin using a jumper, then turn the power on while holding the jumper. This allows the board to communicate over USB.

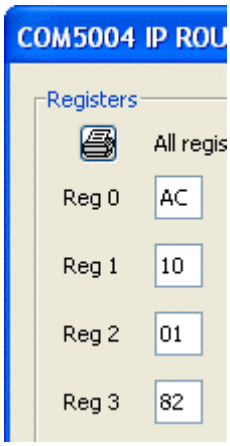
b) Connect a short USB cable between the COM-5004 and a PC. When using ComBlocks for the first time, the PC will ask for a USB driver. Just follow the instructions and point to the driver located in the ComBlock CD-ROM folder entitled "\Windows Drivers\USB 2.0\Windows Driver"

c) Start the ComBlock Control Center, click on the *Communication parameters setup* button and select USB as the primary communication channel.

d) In the ComBlock Control Center window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-1400 module, then click the *Settings* button.

e) Enter a router IP address in control registers REG0 through REG3. The IP address must be unique and must be consistent with your LAN (i.e. the first two or three numbers of the router IP address match the first two or three numbers of your computer's IP

address). Please note that the IP address is entered as hexadecimal numbers as defined in REG0-3 definition.



AC.10.01.82 hex = 172.16.1.130 decimal

f) Click on the Personalities button and set personality index 2 as the new default. Reboot.

This procedure is a one-time procedure required before the first use. Once the router IP address is saved in non-volatile memory, the ComBlock Control Center can communicate with the COM-5004 over the LAN.

Configuration

An entire ComBlock assembly comprising several ComBlock modules can be monitored and controlled centrally over a single connection with a host computer. Connection types include built-in types:

- TCP-IP/LAN,

or connections via adjacent ComBlocks:

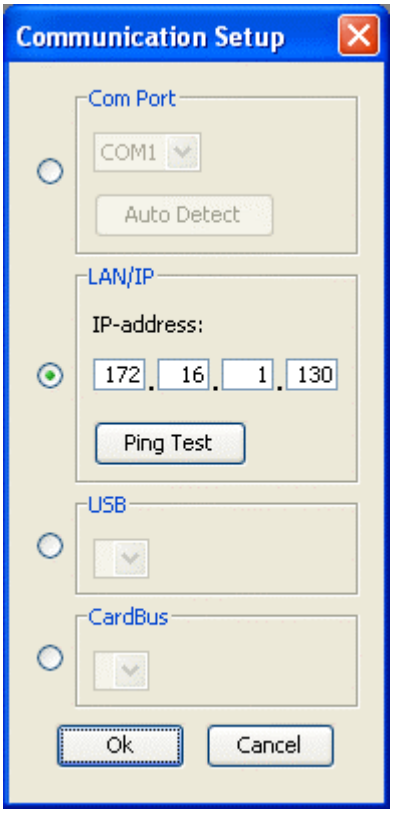
- USB
- TCP-IP/LAN,
- Asynchronous serial (DB9)
- PC Card (CardBus, PCMCIA).

The module configuration is stored in non-volatile memory.

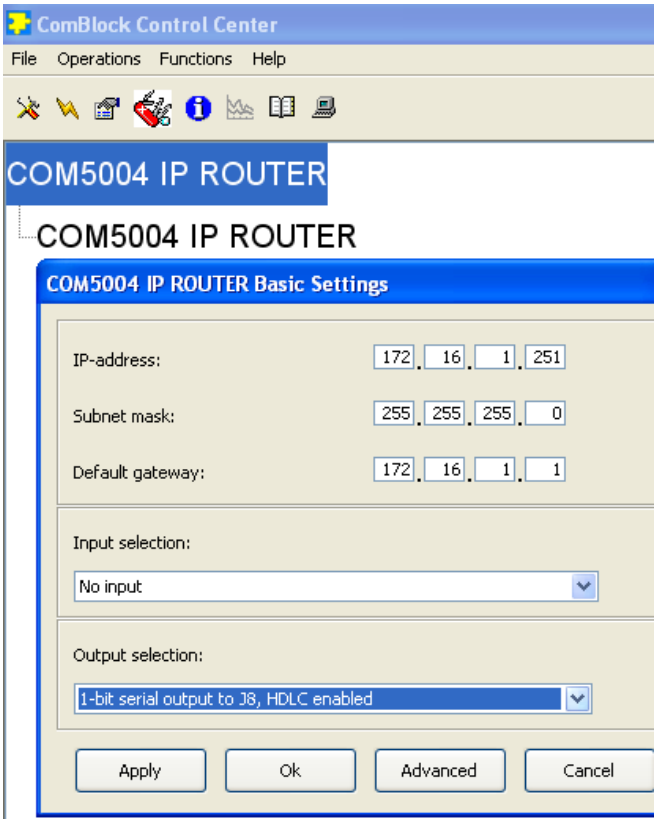
Configuration (Basic)

The easiest way to configure the COM-5004 is to use the **ComBlock Control Center** software supplied with the module on CD.

Start the ComBlock Control Center, click on the *Communication parameters setup* button and select LAN/IP as the primary communication channel. Enter the COM-5004 IP address as previously defined.



Then detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-5004 module to be configured, next click the *Settings* button to display the *Settings* window shown below:



Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write.

Undefined control registers or register bits are for backward software compatibility and/or future use. They are ignored in the current firmware version.

Parameters	Configuration
Router IP address	Router's own static IP address. Other local IP nodes must be told of this router IP address (usually referred to as "Default gateway" in the Internet Protocol properties control panel). Example : 0x AC 10 01 80 designates address 172.16.1.128 The new gateway IP address becomes effective immediately (no need to reset the ComBlock). REG0: MSB REG1 REG2 REG3: LSB
Subnet mask	4-byte subnet mask. Helps the COM-5004 IP router distinguish between local IP destinations within this subnet and remote destination addresses (to be forwarded to the default gateway address below) Example : 0x FF FF FF 00 designates IP subnet mask 255.255.255.0. The new mask becomes effective immediately (no need to reset the ComBlock). REG4: MSB REG5 REG6 REG7: LSB
Default gateway	Tells the IP router where to forward IP packets not destined for this subnet. 4-byte static IP address. The new address becomes effective immediately (no need to reset the ComBlock). REG8: MSB REG9 REG10 REG11: LSB
Reserved	REG12-19 Reserved for other network configurations. No need to write any data.
Input selection	00000 = J5 connector is disabled 00001 = 1-bit serial input from J5[1] 01000 = 8-bit parallel input from J5 10001 = 1-bit serial input from J8 connector (bi-directional I/O) 11101 = test mode: loopback for 1-bit serial HDLC-encoded stream. J5 input is disabled. REG20 bits 4-0
Bypass descrambling	V.34 descrambling of the bit-serial stream is implemented prior to HDLC decoding. This command is ineffective then serial HDLC decoding is disabled. 0 = descrambling enabled 1 = bypass the descrambling. REG20 bit 6
Bit-serial HDLC decoder enable	Perform HDLC decoding on 1-bit serial receive stream (applicable only when 1-bit input serial format is selected above). 0 = disabled 1 = enabled REG20 bit 7

[1] Enabling the bit-wise HDLC is strongly advised to preserve the bit to byte alignment information during bit-serial transmission.

Output selection	00000 = J8 connector is disabled. 00001 = 1-bit serial output to J8[2] 01000 = 8-bit parallel output to J8 10001 = 1-bit serial output to J5 (bi-directional I/O) 11111 = special case: 1-bit serial output to COM-7001 FEC encoder through J8. REG21 bits 4-0
Bypass scrambling	V.34 scrambling of the bit-serial stream is implemented after bit-serial HDLC encoding. This control is ineffective when bit-serial HDLC is disabled. 0 = scrambling enabled 1 = bypass the scrambling stage. REG21 bit 6
Bit-serial HDLC encoder enable	Perform HDLC encoding on 1-bit serial receive stream (applicable only when 1-bit output serial format is selected above). When no data is available from the selected source(s), the HDLC engine sends empty frames 7E 7E. 0 = disabled 1 = enabled. REG21 bit 7

COM-8001 external trigger	Special use: Writing to REG22 with a '1' in bit 1 will generate a 1 CLK wide pulse on pin J8/B6. The main application is to trigger the COM-8001 file playback/download. There is no need to reset this bit to '0' prior to writing a '1'. REG22 bit 1.
10Base-T / 100Base-TX LAN selection	00 = 10Base-T 01 = 100Base-TX 10 = Auto negotiation Changes will take effect at the next power up. REG22 bits 3-2
Half/Full duplex	Half-duplex is a safe configuration which can be used with older networking equipment. Full duplex results in higher throughput but may be incompatible with unswitched hubs. 0 = half-duplex 1 = full duplex. Changes will take effect at the next power up. REG22 bit 4
ARP cache immediate clear	Write a '1' to immediately clear the address resolution protocol (ARP) cache. This table keeps track of the destination MAC address on the LAN for each destination IP address. All entries in the ARP cache are refreshed automatically once every five minutes in the average. Clearing the ARP cache can be useful to avoid waiting when hardware changes occur on the network. REG22 bit 5
Directed broadcasts enable	Directed broadcast IP packets are those packets with IP destination address in the form (Network prefix, 255). For example 172.16.255.255 or 172.16.1.255. 0 = disable forwarding of directed broadcast IP packets 1 = enable forwarding of directed broadcast IP packets REG22 bit 6

[2] Enabling the bit-wise HDLC is strongly advised to preserve the bit to byte alignment information during bit-serial transmission.

Monitoring

Monitoring registers are read-only.

Parameters	Monitoring
TCP-IP connection	Monitors the TCP-IP connection for the M&C port 1028 1 = connected, 0 otherwise. SREG0 bit 0
Number of transmitted bytes (LAN to WAN)	Cumulative number of bytes sent in the LAN to WAN direction. Includes the byte-wise HDLC overhead of 6 bytes + 0.5% of the routed IP packet size. 32-bit byte count. Counter rolls over when reaching 0xFFFFFFFF. SREG1: bits 7-0 (LSB) SREG2: bits 15-8 SREG3: bits 23-16 SREG4: bits 31-24 (MSB)
Number of received bytes (WAN to LAN)	Cumulative number of bytes received in the WAN to LAN direction. Includes the byte-wise HDLC overhead of 6 bytes + 0.5% of the routed IP packet size. 32-bit byte count. Counter rolls over when reaching 0xFFFFFFFF. SREG5: bits 7-0 (LSB) SREG6: bits 15-8 SREG7: bits 23-16 SREG8: bits 31-24 (MSB)
Erroneous IP packets	Cumulative number of IP packets received on the WAN side with bad CRC and subsequently rejected. 32-bit byte count. Counter rolls over when reaching 0xFFFFFFFF. SREG9: bits 7-0 (LSB) SREG10: bits 15-8 SREG11: bits 23-16 SREG12: bits 31-24 (MSB)
MAC address	Unique 48-bit hardware address (802.3). In the form SREG13:SREG14:SREG15:…:SREG18

As the monitoring data is constantly changing, it is important to be able to prevent changes while reading a multi-byte parameter. The monitoring data is latched upon reading register 0. Therefore, register 0 should always be read first.

Digital Test Points

Test points are provided for easy access by an oscilloscope probe. The main focus of these test points is to help monitor proper flow control operation.

Test Point	Definition
LAN to WAN direction	
TP 1	Incoming LAN data packet. Timescale: 25 ns per byte.
TP 2	IP routing allowed flag. High at the end of the packet when all IP routing criteria are met.
TP 3	Forwarding IP packet to WAN. Packet is byte-wise HDLC encoded. Timescale: 25 ns per byte.
TP 4	Transmitter buffer overflow condition. The packet is discarded.
WAN to LAN direction	
TP 5	Receiving IP packet from WAN. Packet is byte-wise HDLC encoded. Timescale: 25 ns per byte.
TP 6	0x7E flag marking the start and end of the HDLC encoded packet.
TP 7	Bad CRC16 in packet received from the WAN. The packet is discarded.
TP 8	No routing information available in the routing table, no ARP reply from the target. The packet is discarded.
TP9	Receiver buffer overflow condition. The packet is discarded.
TP10	Outgoing LAN data packet. Timescale: 25ns per byte.
INIT#	CLK_P internal processing clock divided by 8. 5 MHz square wave.
DONE	1 when the FPGA is loaded with a valid .mcs configuration file. The COM-5004 is operational typically 0.4 seconds after power up.

Operation

Concept

The COM-5004 forwards IP packets from a RJ-45 10/100Mbps LAN interface to a clock-synchronous Low Voltage TTL (LVTTL) interface and vice versa.

The IP packets received over the LAN are stripped of their link layer information: Ethernet source address, destination address and type are removed, keeping only the IP fields.

TCP, UDP, ICMP and IGMP packets are processed since they are transmitted as IP datagrams.

Non IP packets are rejected.

IP packets whose Time-To-Live field has reached zero are discarded. For the other packets, the TTL is decremented.

Limited broadcasts (those with destination IP address 255.255.255.255) are not forwarded.

Packets received while the IP router is busy are also discarded without notification.

The IP packet maximum size (maximum transmission unit (MTU)) is 1500 bytes. No datagram fragmentation is necessary nor used.

The IP packets are then encapsulated within a byte-wise HDLC frame, one packet per frame. A 16-bit CRC is inserted at the end of each frame to detect errors upon reception.

The resulting packet is then sent over the LVTTL synchronous link using one of several formats: byte-wise or bit serial with serial HDLC.
[Note: the bit-serial HDLC is in addition to the byte-wise HDLC framing].

The reverse process is performed at the receiving end. Erroneous packets which do not pass the CRC test are rejected.

The forwarding rules are specified in the RFC1812 document “Requirements for IP Version 4 Routers”.

When an IP packet is received over the synchronous interface, the IP router will check whether the packet destination is for this local subnet or not. If not, the packet will be forwarded to the default gateway IP. To determine whether a packet is destined to this subnet, the router compares the masked destination address (Destination IP address & subnet mask) with the masked router address
(IP router own IP address & subnet mask).

Example:

- Router IP address: 172.16.1.1
- Router subnet mask: 255.255.255.0
- Packet destination IP address is 74.54.97.66

Masked packet destination: 74.54.97.0
Masked router address: 172.16.1.0
Since the masked packet destination does not match the masked router address, the packet is not for a local destination. Consequently the router will forward the packet to the default gateway.

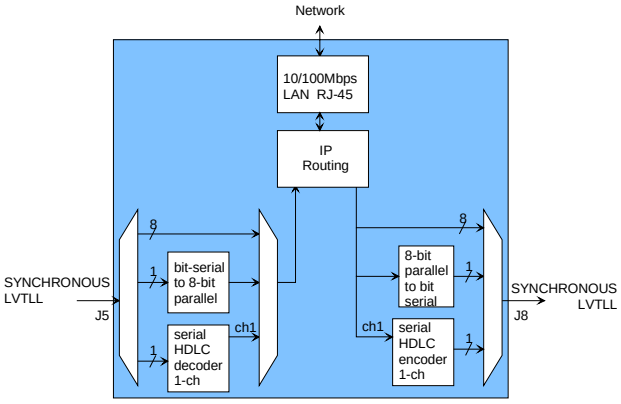
Valid IP packets are re-encapsulated inside an Ethernet packet, one IP packet per Ethernet packet.

The IP to Ethernet MAC address association is determined by means of an Address Resolution Protocol (ARP) query-reply transaction. The COM-5004 will send an ARP request asking “whois the destination IP address?” and will wait for the ARP reply with the MAC information.

The IP address – MAC address relationships are stored within two ARP cache memories to expedite the Ethernet packet construction. The ARP cache memories are refreshed every 5 minutes on average. The total cache capacity is 170 entries. The user can clear the ARP cache without wait: see control register REG22 bit 5.

LVTTL I/O Format

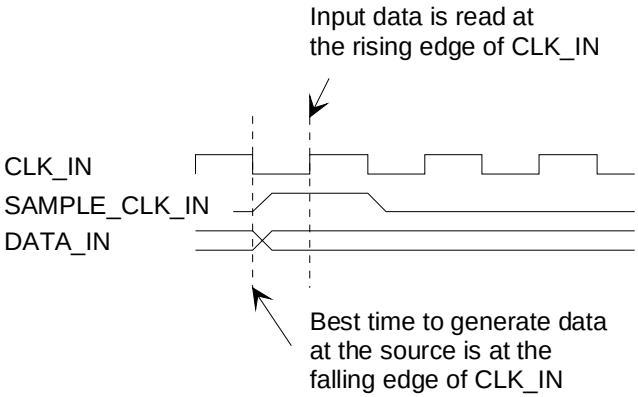
The user can select among several formats (8-bit parallel mode or 1-bit serial with HDLC) for the input and output connectors through control registers.



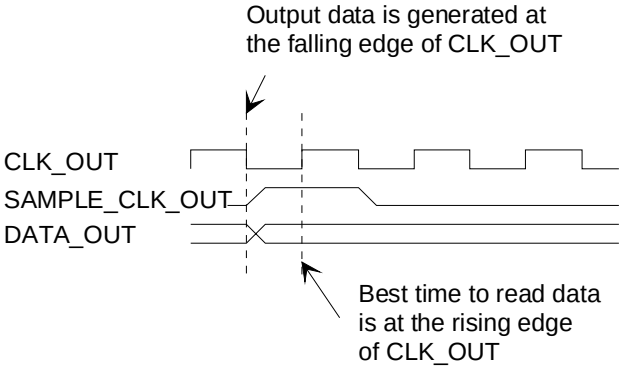
I/O Format

Timing for the LVTTL interface is shown below:

Input



Output



Format Conversion

Parallel to serial conversion occurs at the output when an 8-bit byte received over the IP link is converted to one-bit serial when so configured by the user. The key rule for parallel to serial conversion is that the most significant bit (MSb) is transmitted first.

Likewise, in the serial-to-parallel conversion which may be implemented at the input, the first received bit is placed at the MSb position in the byte.

Serial HDLC

A bit-serial HDLC format can be used to convey data over a synchronous bit-serial link such as a wireless or satellite link. The HDLC objective is three-fold:

(a) Tell the receiver side when no information is available for transmission (sending empty frames).

(b) Implement multiple virtual channels over a common physical link (unused feature here)

(c) Recover the original bit-to-byte alignment of the original USB or TCP-IP connection at the receiving end.

This bit-serial HDLC can be enabled or disabled under user control. See control registers REG20 and REG21.

Please refer to the COM-5003 specifications for more details about the serial HDLC frame format.

Trigger Pulse

Users can remotely generate a short (25ns) pulse to trigger external devices such as the COM-8001 arbitrary waveform generator. The EXT_TRIGGER_OUT pulse is generated on pin J8/B6 upon sending control register REG22 with bit 1 set to '1'.

Recovery

The COM-5004 is protected against corruption by an invalid FPGA configuration file or an invalid user configuration. To recover from such an occurrence, connect the BOOT pin to the nearby ground pin using a jumper and power-up the COM-5004. Remove the jumper after 1 second. This will restore USB communications with the ComBlock Control Center. This boot file is un-erasable. Once this is done, the user can safely restore the user configuration and/or re-load a valid FPGA configuration file into flash memory using the ComBlock Control Center.

TCP-IP

As a server, the module opens a TCP-IP socket in listening mode at port 1028, waiting for a connection request from a ComBlock Control Center (the client) for monitoring and control purposes.

Ping

The module responds to ping requests with size up to 470 bytes. Ping can be used to check the module response over the LAN network. Ping can be used at any time, concurrently with other transmit and receive transactions. For example, on a Windows operating system, open the Command prompt window and type “ping –t –l 470 172.16.1.128” to send pings forever of length 470 bytes to address 172.16.1.128.

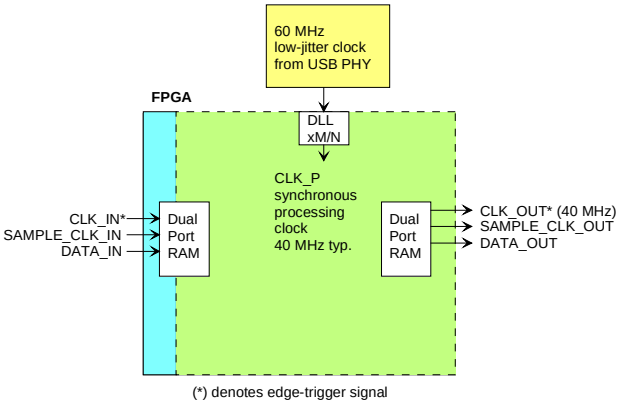
Power Up

The LAN link is available 2.05 seconds after power up.

Timing

Clocks

The clock distribution scheme embodied in the COM-5004 is illustrated below.



Baseline clock architecture
Green = 40 MHz processing zone and output clock
Light blue = user defined input clock

Input:
The input signals at the J5 connector are synchronous with the CLK_IN clock at J5/A1. This clock can be up to 40 MHz.

A 32Kbit dual-port RAM elastic buffer is used at the boundary between inputs and internal processing area. Thus, the input clock frequency can be independent from the internal processing clock frequency.

Internal processing:
The core signal processing performed within the FPGA is synchronous with the 40 MHz processing clock CLK_P. The processing clock is derived from the USB PHY 60 MHz oscillator. CLK_P is not related to the external CLK_IN clock.

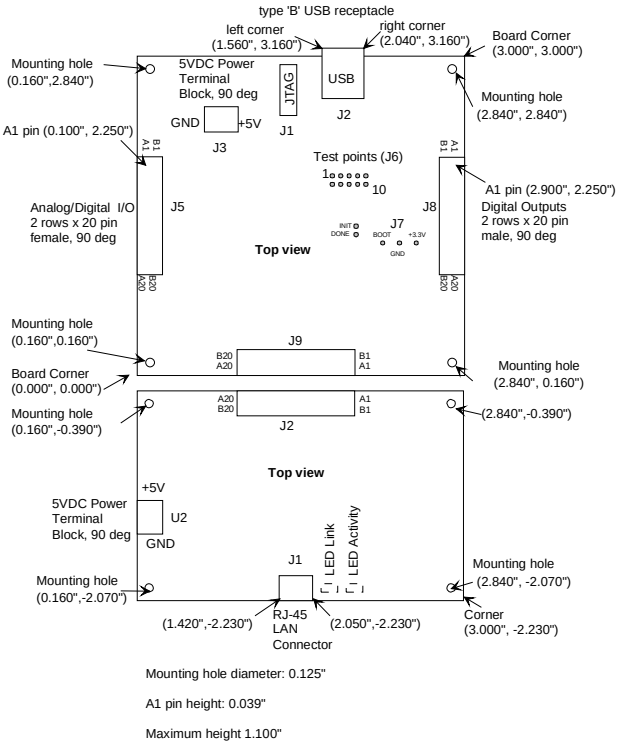
Output:
The 40 MHz output clock CLK_OUT is the same as the processing clock CLK_P.

The output signals are synchronous with the rising edge of the 40 MHz reference clock CLK_OUT (i.e. all signals are stable at the rising edge of the reference clock CLK_OUT).

LEDs

2 LEDs located close to the LAN RJ-45 jack provide summary information as to the LAN: Link and activity.

Mechanical Interface



Schematics

The board schematics are available on-line at ComBlock.com/download/com_1400schematics.zip for the main board and ComBlock.com/download/com_5002schematics.zip for the LAN adapter.

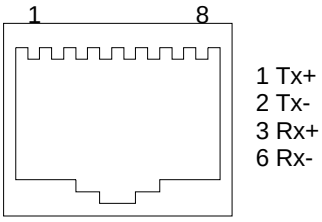
Pinout

USB Connector J2

USB type B receptacle.

LAN Connector J1

The RJ-45 Jack is wired as a standard PC network interface card. Connection to a LAN switch is over a straight-through cable. Use a crossover cable to connect directly to a PC.

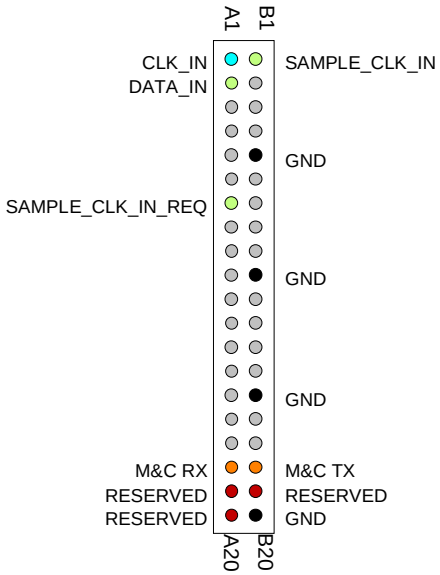


RJ-45 Jack

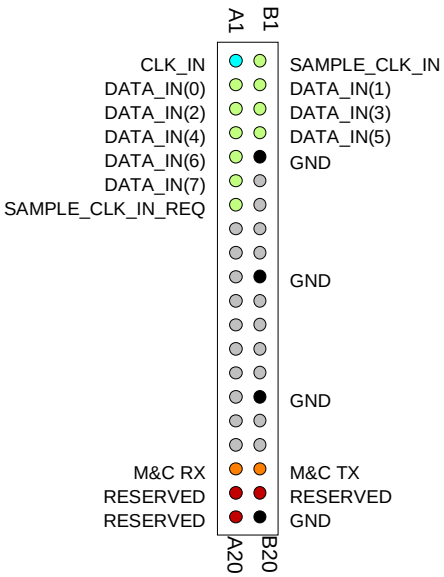
Input Connector J5

There are several possible connector configurations, depending on the application:

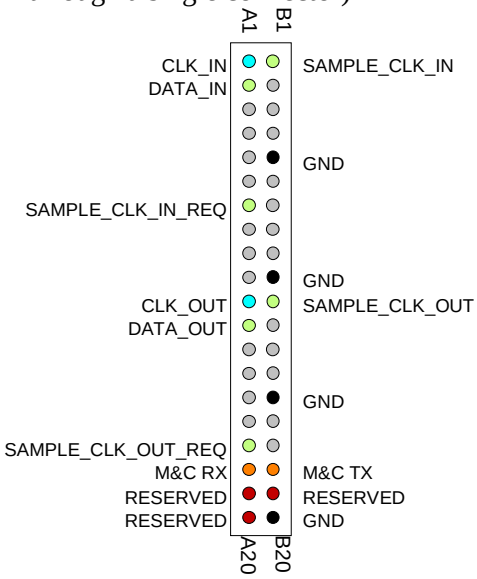
(a) 1-bit wide connection to another ComBlock [COM-1009, COM-7001, COM-1202, COM-1418, COM-1027, etc]



(b) 8-bit wide connection to another ComBlock [COM-5004, COM-8002,etc]



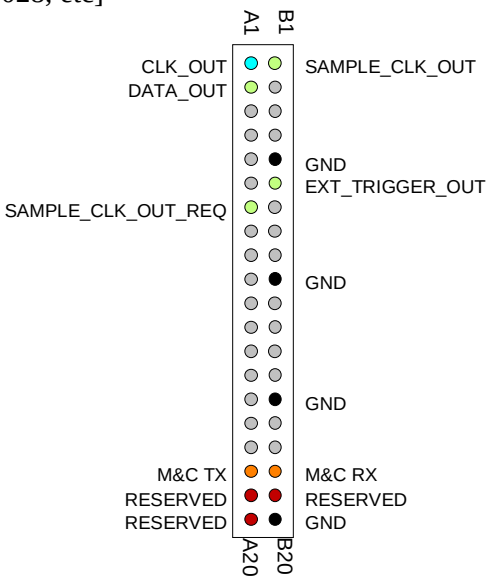
(c) Bi-directional connection (input and output through a single connector)



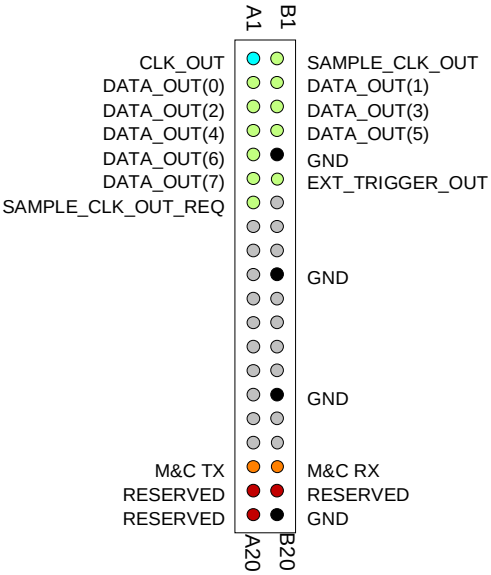
Output Connector J8

There are several possible connector configurations, depending on the application:

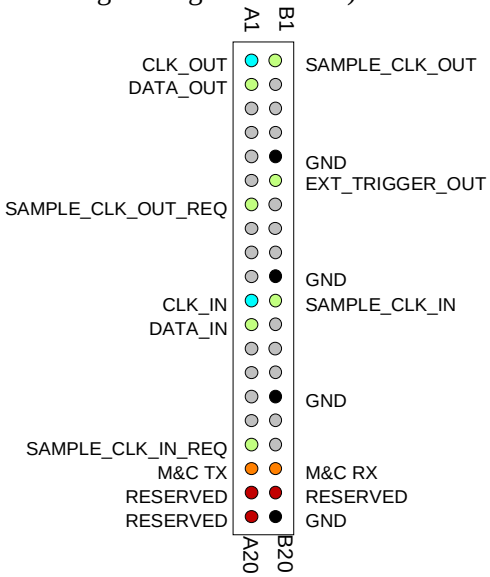
(a) 1-bit wide connection to another ComBlock [COM-1010, COM-1402, COM-1019, COM-1028, etc]



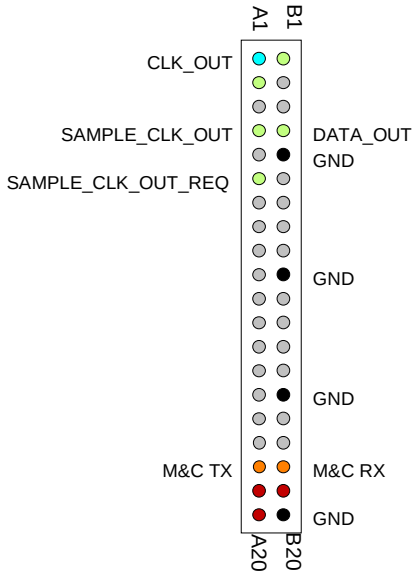
(b) 8-bit wide connection to another ComBlock [COM-8001, COM-5004, etc]



(c) Bi-directional connection (input and output through a single connector)



(d) Special case: 1-bit serial connection to a COM-7001 turbo code encoder.



I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-7001 Turbo Code Encoder / Decoder	COM-7001 Turbo Code Encoder / Decoder
COM-1009 Viterbi Decoder K=7	COM-1010 Convolutional encoder K=9,7,5
COM-1400 FPGA development platform	COM-1400 FPGA development platform

Configuration Management

This specification is to be used in conjunction with VHDL software revision 5.

ComBlock Ordering Information

COM-5004 IP Router

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