

# COM-5101 SIGNAL/POWER CONDITIONING & RS422 INTERFACE

# **Key Features**

- Support functions for Comblock assembly:
  - DC/DC converter for extended supply range.
  - RS422 interface for longer cable connections.
  - 40 MHz clock as reference processing clock for FPGAs.
  - Signal conditioning for easer interfacing with binary streams (data/clock).
- DC/DC converter: Input supply: 6 – 26V. Vcc1 ouput: 5V 2.5A max. Vcc2 ouput: 5V 2.5A max. Reverse voltage protection. Resettable fuse.
- RS-422:
  4 differential input signals
  4 differential output signals
- RS-232:
  1 full duplex link for monitoring & control.
- Connectorized: DB25 on user side Two standard 40-pin 2mm dual row connectors on the ComBlock sides.

For the latest data sheet, please refer to the **ComBlock** web site: <u>www.comblock.com/download/com5101.pdf</u>. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to <u>www.comblock.com/product\_list.htm</u>.

# Block Diagram





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# **Electrical Interface**

DB25 Module	Definition	
Interface (J1)		
Pins 1,2,14	Ground	
Pins 3,4,15,16	Input supply V IN	
	Range $6 - 26VDC$	
Pin 5	RS 232 TX	
	RS-232C Transmit (O).	
	Typically used for ComBlock	
	monitoring and control: asynchronous	
	serial, 115 Kbaud/s. 8-bit, no parity,	
	one stop bit. No flow control. However,	
	the actual signal definition may be	
	different depending on the	
	configuration option.	
Pin 17	RS232_RX	
	RS-232C Receive (I).	
	Typically used for ComBlock	
	monitoring and control: asynchronous	
	serial, 115 Kbaud/s. 8-bit, no parity,	
	one stop bit. No flow control. However,	
	the actual signal definition may be	
	different depending on the	
D: 12.25	configuration option.	
Pins 13,25	RS-422 differential receive pair 1 (I).	
	Includes 100 Ohm termination and	
D: 12.24	IKOhm pullup/pulldown.	
Pins 12,24	K5-422 differential receive pair 2 (1).	
	Includes 100 Onm termination and	
Ding 11 22	INORM pullup/pulldown.	
PIIIS 11,25	Includes 100 Ohm termination and	
	11 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Pins 10 22	RS-422 differential receive pair 4 (I)	
1 1115 10,22	Includes 100 Obm termination and	
	1KOhm pullup/pulldown	
Pins 9.21	RS-422 differential transmit pair 1 (O)	
Pins 8.20	RS-422 differential transmit pair 2 (0)	
Pins 7.19	RS-422 differential transmit pair 2 (0).	
Pins 6.18	RS-422 differential transmit pair $J(0)$ .	
40-pin Male	Definition	
Connector		
(J6)		
CLK	40 MHz reference clock (O)	
	LVTTL, 0-3.3V. Pin A1.	
Programmable	LVTTL, 0-3.3V.	
signal definition	Interface compatible with most	
	ComBlocks. Refer to connection matrix	
	for details. Mostly used for output	
	signals.	
M&C_TX	Monitoring & Control chain (O)	
	LVTTL, 0-3.3V. Pin A18	
M&C_RX	Monitoring & Control chain (I)	
	LVTTL, 0-3.3V. Pin B18	

40-pin Female	Definition	
Connector (J2)		
CLK_IN	40 MHz reference clock (I)	
	LVTTL, 0-3.3V. Pin A1.	
Programmable	LVTTL, 0-3.3V.	
signal definition	Interface compatible with most	
	ComBlocks. Refer to connection	
	matrix for details. Mostly used for	
	input signals.	
M&C_RX	Monitoring & Control chain (I)	
	LVTTL, 0-3.3V. Pin A18	
M&C_TX	Monitoring & Control chain (O)	
	LVTTL, 0-3.3V. Pin B18	

#### The maximum peak throughput on each RS422 line is 10 MHz. (Maximum interface speed is 2 samples every 200 ns).

# Operation

The COM-5101 can be configured in many ways by selecting a firmware configuration option and by setting the JP1 jumpers, as described below. The main features which can be configured by firmware are

- (a) Internal versus external 40 MHz clock selection.
- (b) Signal to pin assignment for 40-pin connectors J2/J6.
- (c) RS422/RS232 transceivers signal assignment.
- (d) Signal reclocking/reformatting types.

The firmware configuration option is to be selected at the time of order. However, with minimum Xilinx software and JTAG programming tools (not supplied), other options can be programmed incircuit by users. All configuration files are available for download at <u>www.comblock.com/download.htm</u>

Each firmware option encompasses up to 16 different configurations, to be selected by the user by means of the four JP1 jumpers.

### -A Firmware Option

JP1 Jumper Configuration	
[1 2 3 4]	
0000	Connection Matrix A0
0001	Connection Matrix A1
0010	Connection Matrix A2
0011	Connection Matrix A3
0100	Connection Matrix A4
0101	Connection Matrix A5

<b>Connection Matrix A0 Summary</b>		
Signal Group	Signals	
ComBlock (via J2)	1 clock	
to RS422	3 signals	
	No flow control	
RS422 to	1 clock	
ComBlock (via J6)	3 signals	
	No flow control	
40 MHz clock	Internal oscillator. Supplied to	
	ComBlock assembly via J6	
RS232 M&C	Connected to ComBlock via J6	

The primary use of this configuration is to simplify the interface to most ComBlocks by alleviating the need for a 40 MHz synchronous clock over the RS422 cable.



In the direction ComBlock to RS422, the signals are reformatted as shown below.



#### Reformatting from J2/LVTTL to RS-422 interface

In the direction RS422 to ComBlocks, the signals are reformatted as shown below:



Connection Matrix A0		
To Signal	From	Reformatting
-	Signal(s)	_
RS422_TX1	J2/A1 & J2/B1	Converts the CLK_IN synchronous 'SAMPLE_CLK' signal found in most ComBlocks to a simple edge-trigger signal to indicate when to sample the three other RS422 data streams in
		RS422_TX2/3/4.
RS422_TX2 RS422_TX3 RS422_TX4	J2/A2 J2/B2 J2/A3	Converts the CLK_IN synchronous data streams to RS422 signals to be read at the rising edge of RS422_TX1
J6/A1	Internal 40 MHz clock	
J6/B1	RS422_RX1 & Internal 40 MHz clock	Converts rising-edge of RS422 signal into a 25ns pulse synchronous with the internal 40 MHz clock. Creates the 'SAMPLE_CLK_IN' signal needed by most digital ComBlock inputs.
J6/A2	RS422_RX2 & Internal 40 MHz clock	Reclock to make signals synchronous with the internal 40 MHz clock.
J6/B2	RS422_RX3 & Internal 40 MHz clock	Creates the 'DATA_IN' signal needed by most digital ComBlock inputs.
J6/A3	RS422_RX4 & Internal 40 MHz clock	
J6/A18 M&C_TX	RS232_RX	
J2/B18 M&C_TX	RS232_RX	
KS232_TX	J6/B18 or J2/A18 M&C RX	

# I/O Compatibility List and Limits

(not an exhaustive list)

Input (J2)	Output (J6)
COM-1001 BPSK/QPSK/OQPSK	
digital demodulator	
COM-1011 Direct Sequence Spread-	
Spectrum demodulator 10 Mchip/s	
COM-1019 Direct Sequence Spread-	
Spectrum demodulator 20 Mchip/s	
COM-1027 FSK/MSK/GFSK/GMSK	
demodulator	

COM-1010 Convolutional encoder	COM-1009
	Viterbi
	decoder

<b>Connection Matrix A1 Summary</b>		
Signal Group	Signals	
ComBlock (via J2)	1 clock	
to RS422	2 signals	
	No flow control	
RS422 to	1 clock	
ComBlock (via J6)	3 signals	
	1 flow control signal	
40 MHz clock	Internal oscillator. Supplied to	
	ComBlock assembly via J6	
RS232 M&C	Connected to ComBlock via J6	

The A1 connection matrix is similar to the A0 connection matrix, except for the provision of a flow control signal to regulate data throughput in the RS422 to ComBlock direction. This configuration is to be used in conjunction with ComBlock modulators. Indeed modulators typically require a flow control mechanism, as the modulation data rate is determined by the modulator at the end of the transmission chain. The flow control signal propagates upstream to control the source throughput.



40-pin connectors J2 / J6

<b>Connection Matrix A1</b>		
To Signal	From Signal(s)	Reformatting
RS422_TX1	J2/A1 & J2/B1	Converts the CLK_IN synchronous 'SAMPLE_CLK' signal found in most ComBlocks to a simple edge-trigger signal to indicate when to sample the three other

		RS422 data streams in RS422 TX2/3/4.
RS422 TX2	J2/A2	Converts the CLK
RS422 TX3	J2/B2	synchronous data streams
_		to RS422 signals to be
		read at the rising edge of
		RS422_TX1.
J6/A1	Internal 40	
	MHz clock	
J6/B1	RS422_RX1	Converts rising-edge of
	& Internal 40	RS422 signal into a 25ns
	MHz clock	pulse synchronous with the
		internal 40 MHz clock.
		Creates the
		'SAMPLE_CLK_IN'
		signal needed by most
		digital ComBlock inputs.
J6/A2	RS422_RX2	Reclock to make signals
	& Internal 40	synchronous with the
	MHz clock	internal 40 MHz clock.
J6/B2	RS422_RX3	Creates the 'DATA_IN'
	& Internal 40	signal needed by most
	MHz clock	digital ComBlock inputs.
J6/A3	RS422_RX4	
	& Internal 40	
	MHz clock	
RS422_TX4	J6/A7	Converts the CLK
		synchronous data streams
		to RS422 signals to be
		read at the rising edge of
		RS422_RX1.
J6/A18	RS232_RX	
M&C_TX		
RS232_TX	J6/B18	
	M&C_RX	

### I/O Compatibility List and Limits

(not an exhaustive list)	
Input (J2)	Output (J6)
COM-1001	COM-1002
BPSK/QPSK/OQPSK	BPSK/QPSK/OQPSK
digital demodulator	digital modulator.
COM-1011 Direct	COM-1012 Direct Sequence
Sequence Spread-	Spread-Spectrum digital
Spectrum demodulator 10	modulator.
Mchip/s	
COM-1019 Direct	COM-1018 Direct Sequence
Sequence Spread-	Spread-Spectrum digital
Spectrum demodulator 20	modulator.
Mchip/s	
COM-1027 FSK	COM-1028
demodulator	FSK/MSK/GFSK/GMSK
	digital modulator

<b>Connection Matrix A2 Summary</b>		
Signal Group	Signals	
ComBlock (via J2)	unused	
to RS422		
RS422 to	1 bit clock	
ComBlock (via J6)	1 byte clock	
	1 serial data stream to be converted	
	to 8-bit parallel.	
	1 trigger signal	
40 MHz clock	Internal oscillator. Supplied to	
	ComBlock assembly via J6	
RS232 M&C	Connected to ComBlock via J6	

The A2 connection matrix is primarily intended for use in conjunction with the COM-8001 arbitrary waveform generator. It allows one to load a file from a host computer into the COM-8001 SDRAM memory at speed up to 10 Mbit/s over a RS422 connection. The data stream is transmitted serially over the RS422 connection and converted into an 8bit byte for interface compatibility with the COM-8001 input. As this configuration does not support flow-control, the sender is responsible for maintaining the serial throughput below the 10 Mbit/s limit.



Connection Matrix A2			
To Signal	From	Reformatting	
	Signal(s)		
J6/A1	Internal 40		
CLK_OUT	MHz clock		
J6/B1	RS422_RX1	Creates a	
SAMPLE_CLK_OUT	(serial bit	SAMPLE_CLK_OUT	
	clock) and	pulse indicating that	
	RS422_RX2	the DATA_OUT byte	
	(byte clock)	is ready to be read.	
	& Internal	The pulse is generated	
	40 MHz	upon receiving the last	
	clock	serial bit (LSB).	
J6/A2	RS422_RX3	The serial data stream	
DATA_OUT(0)	(serial bit),	conveyed by	
J6/B2	RS422_RX1	RS422_RX3 is	
I6/A3	(serial bit	converted into a 8-bit	
DATA OUT(2)	clock),	byte. Bit 7 (most	
J6/B3	RS422_RX2	significant bit) is	
DATA OUT(3)	(byte clock)	transmitted first.	
J6/A4	& Internal	Bit / is identified in	
DATA_OUT(4)	40 MHz	the serial data stream	
J6/B4	clock	by RS422_RX2 (byte	
DATA OUT(5)		$clock) = 1^{\circ}$ . For all	
$J_{0}$ $J_{0$		other serial bits, the	
I6/A6		KS422_KX2 byte	
DATA OUT(7)		CIOCK IS U.	
J6/B6	RS422 RX4	Reclock to make	
TRIGGER_OUT	(trigger out),	signals synchronous	
	RS422 RX1	with 40 MHz clock.	
	(serial bit	Creates the	
	clock)	'TRIGGER_OUT'	
	& Internal	signal needed by the	
	40 MHz	COM-8001.	
	clock		
J6/A18 M&C_TX	RS232_RX		
RS232_TX	J6/B18		
	M&C RX		

# I/O Compatibility List and Limits

(not an exhaustive list)

Input (J2)	Output (J6)
	COM-8001 Arbitrary waveform generator.
	256MB/1GB, 40 Msamples/s.

<b>Connection Matrix A3 Summary</b>		
Signal Group	Signals	
RS422 to ComBlock (via J2)	4 signals	
ComBlock (via J2) to RS422	4 signals	
ComBlock (via J6) to/from RS422	Unused.	
40 MHz clock	Unused.	
RS232 M&C	Connected to ComBlock assembly via J2	

The primary use of this configuration is to convey four signals in each direction between a ComBlock assembly and a user over the RS422 cable. No reclocking or reformatting takes place.  $\geq \square$ 



Connection Matrix A0		
To Signal	From Signal(s)	Reformatting
RS422_TX1	J2/B1	None
RS422_TX2	J2/A2	
RS422 TX3	J2/B2	
RS422_TX4	J2/A3	
J2/A11	RS422_RX1	None
J2/B11	RS422 RX2	
J2/A12	RS422_RX3	
J2/B12	RS422_RX4	
J6/A18	RS232_RX	
M&C_TX		
J2/B18	RS232_RX	
M&C_TX		
RS232_TX	J6/B18 or J2/A18	
	M&C_RX	

### I/O Compatibility List and Limits

(not an exhaustive list)

Input (J2)	Output (J6)
COM-7001-B Turbo Code Encoder / Decoder	

<b>Connection Matrix A4 Summary</b>		
Signal Group	Signals	
RS422 to	1 serial data	
ComBlock (via J6)		
ComBlock to	1 data clock, rising edge	
RS422 (via J6)		
40 MHz clock	Internal oscillator. Supplied to	
	ComBlock assembly via J6	
RS232 M&C	Connected to ComBlock via J6	

The A4 connection matrix can be used to connect an external data source to a ComBlock transmit assembly. Two signals are conveyed over the RS422 cable:

- a serial data stream from from the data source to the ComBlock assembly.
- a data clock from the ComBlock assembly to the data source.

The data source is expected to generate one data bit at each <u>rising edge</u> of the data clock. Conversely, the ComBlock assembly reads the serial data shortly after the falling edge of the data clock. For falling edge trigger, see connection Matrix A5.

There is no need for flow-control signals as the ComBlock only generate a data clock when it can accept serial input data.



cycle. It consists of 50ns positive pulses, irrespective of the actual data throughput.

<b>Connection Matrix A4</b>		
To Signal	From Reformatting	
	Signal(s)	
RS422_TX1	J6/A7	Data clock.
		The flow control signal from the transmit ComBlock module is converted into a 50ns data clock pulse requesting (pulling) a serial data bit from the external data source.
		The maximum response time for the external data source is 50ns after the rising edge of the data clock RS422_TX1.
J6/A1	Internal 40 MHz clock	
J6/B1	J6/A7 & Internal 40 MHz clock	Generate the SAMPLE_CLK_IN signal needed by most transmit ComBlock modules.
J6/A2	RS422_RX1	Serial data from the external data source.
J6/A18 M&C_TX	RS232_RX	
RS232_TX	J6/B18 M&C RX	

### I/O Compatibility List and Limits

(not an ex	chaustive list)
Input	Output (J6)
(J2)	
	COM-1002 BPSK/QPSK/OQPSK digital
	modulator.
	COM-1012 Direct Sequence Spread-
	Spectrum digital modulator.
	COM-1018 Direct Sequence Spread-
	Spectrum digital modulator.
	COM-1028 FSK/MSK/GFSK/GMSK digital
	modulator
	COM-1010 Convolutional encoder

(\*) denotes reclocking and reformatting.

#### 40-pin connector J6

Note: The data clock signal requesting data from the external data source does not have a 50% duty

<b>Connection Matrix A5 Summary</b>		
Signal Group	Signals	
RS422 to	1 serial data	
ComBlock (via J6)	mBlock (via J6)	
ComBlock to	1 data clock, falling edge	
RS422 (via J6)		
40 MHz clock	Internal oscillator. Supplied to	
	ComBlock assembly via J6	
RS232 M&C	Connected to ComBlock via J6	

The A5 connection matrix can be used to connect an external data source to a ComBlock transmit assembly. Two signals are conveyed over the RS422 cable:

- a serial data stream from from the data source to the ComBlock assembly.
- a data clock from the ComBlock assembly to the data source.

The data source is expected to generate one data bit at each <u>falling edge</u> of the data clock. Conversely, the ComBlock assembly reads the serial data shortly after the falling edge of the data clock. For rising edge trigger, see connection Matrix A4.

There is no need for flow-control signals as the ComBlock only generate a data clock when it can accept serial input data.



(\*) denotes reclocking and reformatting.

#### 40-pin connector J6

Note: The data clock signal requesting data from the external data source does not have a 50% duty

cycle. It consists of 50ns inverted pulses, irrespective of the actual data throughput.

### **RS-422 Line Termination**

All RS422 receivers include a 100 Ohm line termination resistor. Pull up/down resistors ensure that the RS422 receiver will be in a determined state when the line is not connected.

### **RS-422 Twisted Pairs**

When assembling the harness to be connected to the DB-25 connector, please make sure that the differential RS-422 signals are conveyed over twisted pairs.

For example the RS422\_RX1P/RS422\_RX1N signals are conveyed over a twisted pair. It would be unwise to twist two wires which are not part of the same pair.

# Supply LED

A green LED indicates that output supply voltage is present. It does not mean, however, that the voltage is correct as the LED may turn on even in undervoltage conditions.

# Fuse

The V\_IN supply voltage through the DB-25 is protected by a resettable fuse. The fuse acts like an ordinary fuse to open a circuit in the event of overcurrent caused by a short circuit condition, for example, but resets after the fault is cleared and the power is removed. The fuse ratings vary with temperature as follows:

	Temperature	
Hold current	0C	2.88A
Hold current	20C	2.5A
Hold current	60C	1.5A
Trip current	0C	5.76A
Trip current	20C	5.0A
Trip current	60C	3.0A
Time to trip	20C, 12.5A	10.3s max

# **Output Short-Circuit Protection**

The COM-5101 is protected against ground shortcircuit fault on the regulated output as long as the input voltage is less than 21VDC.

# **Chassis / Circuit Ground**

The chassis ground (outer shell of the DB-25 connector) can be connected or disconnected to the circuit ground by means of a 0 Ohm 0603 surface mount resistor (R30). This allows the user to avoid ground loops by selecting a single connection between chassis ground and circuit ground when integrating the ComBlock modules within a metal chassis. R30 in installed by default. Please refer to the COM-5101 schematics for details: www.comblock.com/download/com\_5101schemati

<u>cs.pdf</u>

# Bypassing the DC/DC Converters

The COM-5101 is equipped with up to two DC/DC converters accepting input voltages in the range 6-26VDC. In applications where the user can only supply +5V, a provision is made to bypass the DC/DC converters. 0 Ohm 0603 surface-mount resistor pads are located around the DC/DC converters to enable/disable bypass. Please refer to the COM-5101 schematics for details: www.comblock.com/download/com\_5101schematics.pdf

# Mechanical Interface



### Pinout

### **DB25 Connector J1**



04000102.dsf

# Input Connector J2 (Capabilities)



### **Output Connector J6**



# **ComBlock Ordering Information**

COM-5101-A

Signal/Power conditioning & RS422 interface, -A configuration

ECCN: 5A991.b.12

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