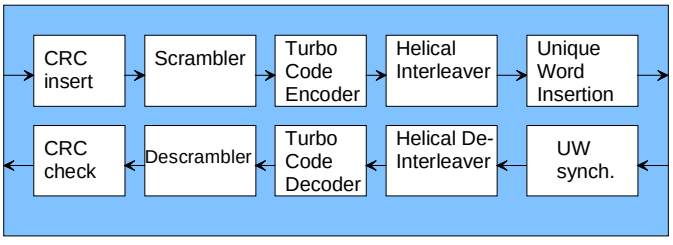
COM-7001 TURBO CODE ERROR CORRECTION ENCODER / DECODER

Key Features

- Full duplex turbo code encoder / decoder.
- Rate: 0.25 to 0.97.
- Block length: 64 bits to 4 Kbits.
- Speed up to 11.7 Mbps.
- Automatic frame synchronization.
- 4-bit soft-quantization input.
- Includes unique word for frame synchronization, helical interleaving, scrambling and CRC.
- Single 5V supply. Connectorized 3"x 3" module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right, bottom). Interfaces with 5V and 3.3V logic.

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com7001.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .



Turbo Codes

Two-dimensional and three-dimensional turbo codes are supported. The constituent code for each dimension is chosen among the following :

Hamming	**Parity**
	(4,3)
(8,4)	(8,7)
(16,11)	(16,15)
(32,26) [2D only]	(32,31) [2D only]
(64,57) [2D only]	(64,63) [2D only]

There are two key restrictions in selecting the 2D or 3D codes :
(a) the third dimension code is limited to a maximum length of 16 bits.
(b) the maximum block size (including the CRC) is 4096 bits.

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Below are a few examples of code selection and the resulting block size and code rate.

Code	Block size (bits)	Rate
2D (64,57)x(64,57)	4096	0.793
3D (32,26)x(32,26)x(4,3)	4096	0.495
3D (16,11)x(16,11)x(16,11)	4096	0.325
2D (8,4)x(8,4)	64	0.25

The overall ability to correct errors is affected by the code rate, the block size and the number of iterations at the decoding end. A high number of iterations will reduce the throughput but increase the error correction capability. It the data rate is set above the capabilities of the decoder, the number of decoding iterations will be automatically reduced.

Below are a few examples of code selection, the resulting coding gain at 10^{-6} BER and data throughput , assuming 6 decoding iterations :

Code	Coding gain @ 10^{-6} BER	Throughput (encoded / decoded) in Mbit/s
2D (64,57)x(64,57)	7.3 dB	11.7/9.2
3D (32,26)x(32,26)x(4,3)	8.1 dB	10.4/5.1
3D (16,11)x(16,11)x(16,11)	8.5 dB	11.0/3.5

Utilities to help with the selection of turbo codes and the computation of block length, rate and coding gain can be found at www.aha.com.

Electrical Interface

The input signals on connector J2 are synchronous with the input clock CLK_IN (pin A1/J2). The maximum frequency for CLK_IN is 40 MHz. Input signals are read at the rising edge of CLK_IN.

All I/O signals on the other connectors (J3/J4) are synchronous with the internal 40 MHz clock CLK_OUT. Output signals are generated on the falling edge, while input signals are read on the rising edge of CLK_OUT.

Coded data input	Definition
DATA_C_IN[3:0]	Coded data input (typically from a demodulator). 4-bit soft quantized. Unsigned representation.
DATA_C_CLK_IN	Input sample clock. One CLK-wide pulse. Read input data at rising edge of CLK when DATA_C_CLK_IN = '1'
Decoded Output	**Definition**
DATA_D_OUT	Decoded data bit.
DATA_D_CLK_OUT	Decoded bit clock. One CLK-wide pulse. Read output data at rising edge of CLK when DATA_D_CLK_OUT = '1'
SOF_D_OUT	Code block synchronization pulse. One CLK-wide pulse, aligned with DATA_D_CLK_OUT for the first bit of the frame (code block).
DATA_D_VALID_OUT	Indicates whether residual errors were found in the PREVIOUS frame after error correction based on the CRC check (when enabled). Read at the following start of frame when FRAME_SYNC = '1'.
Uncoded data input	**Definition**
DATA_U_IN	Uncoded data to be transmitted over noisy channel.
DATA_U_CLK_IN	Input bit clock. One CLK-wide pulse. Read input data at rising edge of CLK when DATA_U_CLK_IN = '1'
DATA_U_CLK_IN_REQ	Output. One CLK-wide pulse. Requests a sample from the module upstream. For flow-control purposes.
Encoded data output	**Definition**
DATA_E_OUT	Encoded data to be transmitted over noisy channel.
DATA_E_CLK_OUT	Output bit clock. One CLK-wide pulse. Read input data at rising edge of CLK when DATA_E_CLK_OUT = '1'
DATA_E_CLK_OUT_REQ	Input. One CLK-wide pulse. Sample request from the module downstream (modulator). For flow-

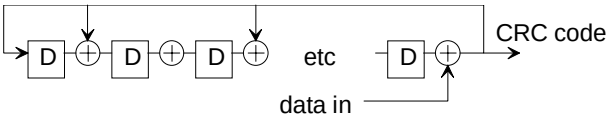
	control purposes.
Ancillary Signals	**Definition**
CLK_IN	Input clock for the I/O signals on connector J2. Maximum frequency is 40 MHz.
CLK_OUT	Output clock for the I/O signals on connector J3/J4. Fixed frequency $\mathbf{f_{clk}}$ of 40 MHz.
Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the CLK frequency. The maximum power consumption at 40 MHz is 300mA.

Operations

CRC check

The Cyclic Redundancy Code is used to detect blocks which contain uncorrected errors. A 16-bit or 32-bit CRC is appended to the data in each block. In applications where spectral efficiency is important, the CRC check can be disabled by software command.

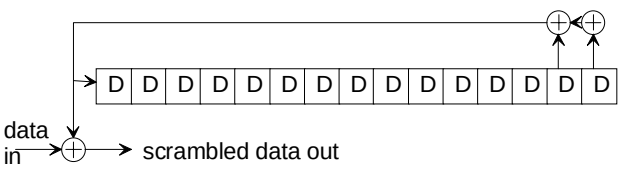
The generic form of the CRC code generator is shown below:



Two standard CRC encoders are available: CCITT 16-bit CRC and 32-bit CRC. The feedback taps are 0x1 10 21 and 0x1 04 C1 1D B7 respectively. The MSB is the leftmost tap on the generic CRC code generator shown above.

Scrambling

A scrambler can be used to randomize the transmitted bit pattern. The scrambler is a 16-bit linear feedback shift register with generator polynomial $1 + x^{14} + x^{15}$.



The scrambler/descrambler is reset at each frame. The seed value (contents of the register upon reset) is 0x5210, where the MSB is in the rightmost register 15. The scrambling and descrambling feature can be enabled or disabled by software command.

Unique Word

A unique word is used for synchronizing the received data stream with the periodic code blocks. The unique word is 32-bit long:
01011010 00001111 10111110 01100110 (binary)
0x 5A 0F BE 66 (hex)
The most significant bit (left-most) is transmitted first.

In order to limit the bandwidth expansion to less than 5%, the unique word transmission frequency depends on the code block size:

Code block size	UW transmission rate
≥ 1024 bits	Once every block
≥ 512 bits and < 1024 bits	Once every two blocks
≥ 256 bits and < 512 bits	Once every four blocks
< 256 bits	Once every eight blocks

The unique word is not error corrected.

The unique word transmission or reception can be disabled by software command. This can be useful in configurations where frame synchronization references are available externally.

If unique word synchronization is enabled, the 32-bit unique word is removed from the received data stream prior to error correction.

Configuration (via Serial Link / LAN)

Complete assemblies can monitored and controlled centrally over a single serial or LAN connection.

The module configuration parameters are stored in non-volatile memory. All control registers are read/write.

Programmers developing custom applications (using the ComBlock API instead of the supplied ComBlock control center graphical user interface) should know that configuration changes are enacted upon (re-)writing to the last register (REG12).

This module operates at a fixed internal clock rate $\mathbf{f_{clk}}$ of 40 MHz.

Undefined control registers or register bits are for backward software compatibility and/or future use. They are ignored in the current firmware version.

Parameters	Attributes
I/O pinout selection	00 = full duplex 01 = encoder only 10 = decoder only REG0 bits 2-1
CRC insertions (transmitter side)	00 = off 01 = 16-bit on 10 = 32-bit on REG0 bits 4-3
CRC check (receiver side)	00 = off 01 = 16-bit on 10 = 32-bit on REG0 bits 6-5
Scrambling (transmitter side)	0 = off 1 = on REG0 bit 7
Scrambling (receiver side)	0 = off 1 = on REG1 bit 0
Tx unique word	0 = off 1 = on REG1 bit 1
Rx unique word synchronization and removal.	0 = off 1 = on REG1 bit 2
Turbo code bypass mode	When set, bypasses the turbo product code at both the encoder and decoder. Connects Uncoded side (_U) to Encoded side (_E). Connects Coded side (_C) to Decoded side (_D). Note: soft-quantized bits are lost in the process. Only the most signicant bit is kept. 0 = off 1 = on REG1 bit 3
Internal pattern generation (test mode)	00 = test mode disabled 01 = counting sequence: When set, the baseband input is disabled and a periodic pattern is internally generated at the encoder input. The pattern consists of an 8-bit counter, MSB transmitted first. 10 = internal generation of 2047-bit periodic pseudo-random bit sequence as modulator input. (overrides external input bit stream). The test pattern bit rate is automatically set by the external sink module (typically a modulator) as part of the flow control mechanism. REG1 bits 5-4
Tx code X-axis (1st dimension)	0000 = no code 0011 = (8,4) Hamming 0100 = (16,11) Hamming 0101 = (32,26) Hamming 0110 = (64,57) Hamming 1010 = (4,3) parity code 1011 = (8,7) parity code 1100 = (16,15) parity code 1101 = (32,31) parity code 1110 = (64,63) parity code REG2 bits 3-0
Tx code Y-axis (2nd dimension)	Same definition as above. REG2 bits 7-4
Tx code Z-axis (3rd dimension)	Same as above but limited to codes of length 16 or less. REG3 bits 3-0
Tx code block size (encoded block size)	Function of the code selection and the CRC selection above. For example if a 3D code (4,3)x(8,7)x(16,15) is used in conjunction with 32-bit CRC, the block length is 3x7x15 – 32 = 283. This field must always be defined (even when configured in decoder-only mode). REG3 bits 7-4 (LSB) REG4 bits 7-0
Rx code X-axis (1st dimension)	Same definition as for tx code. Receiver codes can be selected independently of transmitter codes. REG5 bits 3-0
Rx code Y-axis (2nd dimension)	Same definition as above REG5 bits 7-4
Rx code Z-axis (3rd dimension)	Same as above but limited to codes of length 16 or less. REG6 bits 3-0
Rx code block size (decoded block size)	Function of the code selection. For example if a 3D code (4,3)x(8,7)x(16,15) is used, the block length is 4x8x16 = 512. Maximum size is 4096. Special case: 0 means 4096 This field must always be defined (even when configured in encoder-only mode). REG6 bits 7-4 (LSB) REG7 bits 7-0
Turbo code decoder maximum number of iterations	1 – 254. Typical settings is 6. Special case: 0 = the decoder outputs the hard decision value for each bit without correction. REG8 bits 7-0
Encoder data rate internal / external selection	In most cases, the COM-7001 encoder output data rate is determined by modules downstream (for example a

	modulator). There are, however, cases when the encoder output data rate is set using an internal NCO (for example when testing turbo code encoder and decoder back to back). 0 = exter nal. Encoder output bit rate is based on DATA_E_CLK_OUT_REQ bit requests from following module. 1 = internal. Output bit rate is selected internally by the NCO frequency set in REG10/11/12. Bit requests DATA_E_CLK_OUT_REQ are ignored. REG9 bit 6
Enable test points	1 = Enable additional test points on connector J4. 0 = Disable. REG9 bit 7.
Encoder output data rate	Internal generation of the encoder output data rate. Ignore this field when the output data rate is determined by modules downstream. 24-bit signed integer (2's complement representation) expressed as fsymbol rate * 2^{24} / $\mathbf{f_{clk}}$. The internal processing clock $\mathbf{f_{clk}}$ is typically 40 MHz. REG10 = bit 7-0 (LSB) REG11 = bit 15 – 8 REG12 = bit 23 – 16 (MSB)

Baseline configurations can be found at www.comblock.com/tsbasic_settings.htm and imported into the ComBlock assembly using the ComBlock Control Center File | Import menu.

Configuration example:
REG0 = 0x80
REG1 = 0x07
REG2 = 0x66
REG3 = 0x10
REG4 = 0xCB
REG5 = 0x66
REG6 = 0x00
REG7 = 0x00
REG8 = 0x06
REG9/10/11/12 = 0x00

Scrambling enabled. No CRC inserted. Unique word insertion and detection. Turbo code enabled. Same code for encoder and decoder: 2D (64,57)x(64,57), rate = 0.793. Block size is 4096 bit.

Monitoring (via Serial Link / LAN)

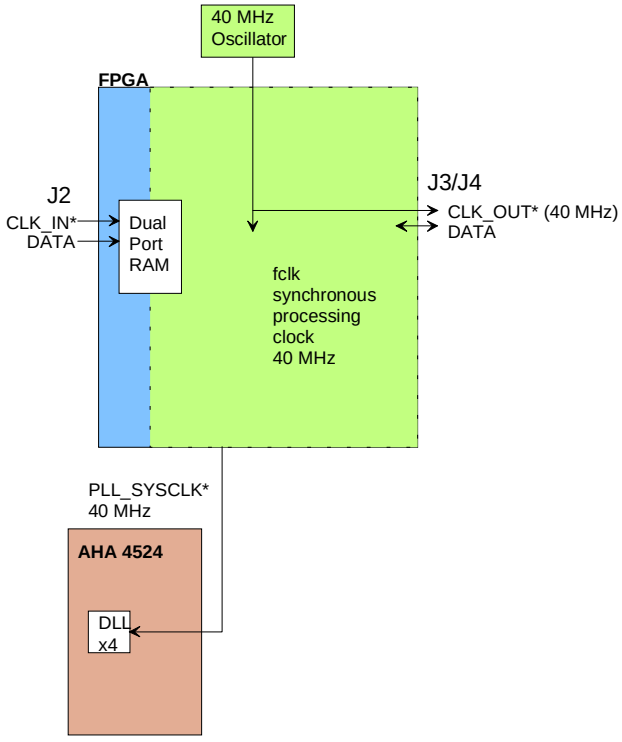
Monitoring registers are read-only.

Parameters	Monitoring
Channel bit error rate	Bit errors counted over 1024 uncorrected bits (unique word). This measurement is refreshed every 16 frames. REG13: bits 7-0 REG14: bits 15-8
Number of errors corrected in each frame	REG15: bits 7-0 REG16: bits 11-8
CRC check	0 = pass 1 = fail REG16 bit 12
Option o / Version v	Returns '7001ov' when prompted for option o and version v numbers.

Timing

Clocks

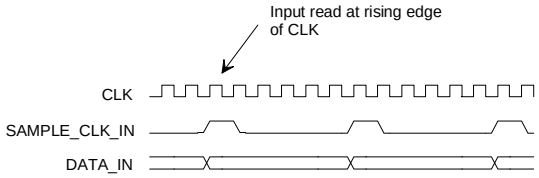
The clock distribution scheme embodied in the COM-7001 is illustrated below.



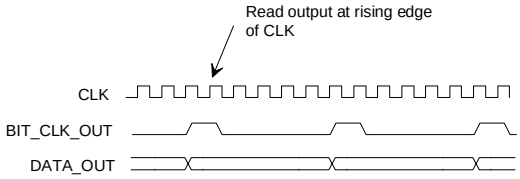
(*) denotes edge-trigger signal

Baseline clock architecture
Green = $\mathbf{f_{clk}}$ processing zone 40 MHz
Blue = CLK_IN I/O zone
Brown = AHA4524, 160 MHz

Input



Output



Test Points

Test points are provided for easy access by an oscilloscope probe.

Test Point	Definition
TP1 (E_GOUT)	'1' when the turbo code encoder data path is empty and not processing a block. '0' otherwise. Use this test point to assess the encoder utilization ratio.
TP2 (D_GOUT)	'1' when the turbo code decoder data path is empty. Use this test point to assess the decoder utilization ratio.
TP3	Receive unique word synchronization. '1' when a unique word is detected with less than 10% bit errors (at least 28 matching bits out of 32).
TP4	Receive start of frame, at the turbo decoder output.
INIT	Unique word transmit enable. Provides some indication as to the encoded frame period.
J4/B7	Receive frame synchronization. Solid '1' when receiving periodic frame preambles at the right time. '0' or toggling otherwise.
J4/B8	'1' when encoder input buffer contains at least a full frame of data ready to encode, '0' otherwise.
J4/B9	'1' when encoder output buffer contains data, '0' when empty
J4/B11	'1' when decoder input buffer contains a full frame of data ready to decode, '0' otherwise.
J4/B12	'1' when decoder output buffer contains data, '0' when empty.

Special test points on connector J4 are enabled only when REG9(7) = '1'. High impedance otherwise.

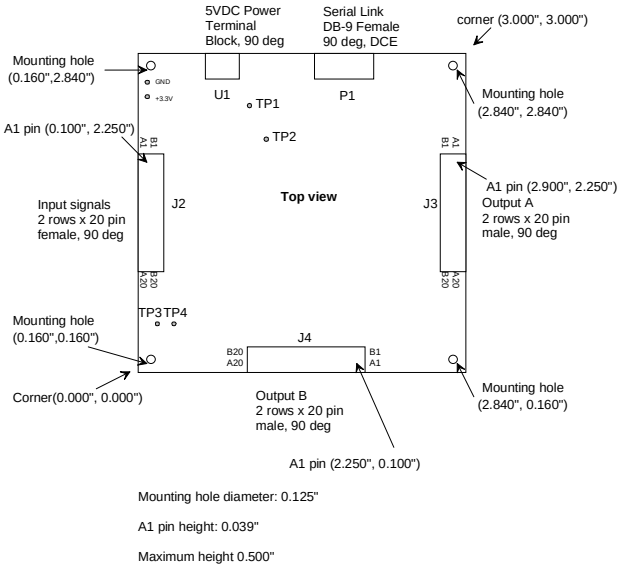
Schematics

The hardware schematics are available on the ComBlock CD shipped with every module.

Configuration Management

This specification document is consistent with the following software versions:
COM-7001 FPGA firmware: Version 22 and above.
ComBlock Control Center graphical user interface: Revision 2.24 and above.
These software versions can be downloaded from www.comblock.com/download.htm

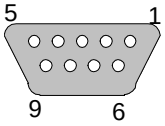
Mechanical Interface



Pinout

Serial Link P1

The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.



DB-9 Female

2 Transmit
3 Receive
5 Ground

Input / Output Connectors

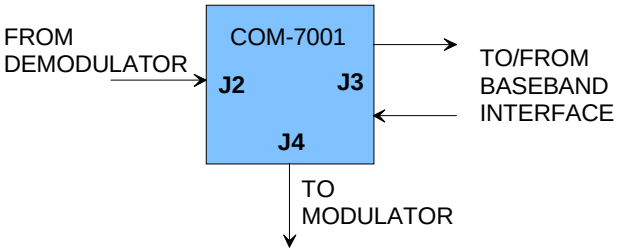
The pinout for the 40-pin input / output connectors can be selected by software command among three possible configurations:

(a) full duplex

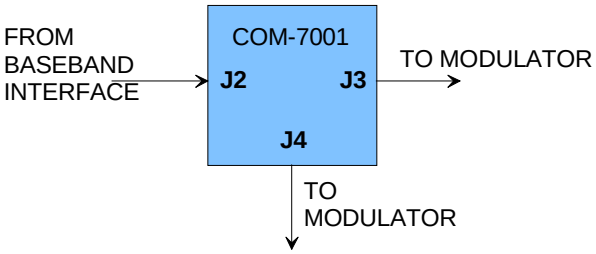
(b) encoder only

(c) decoder only

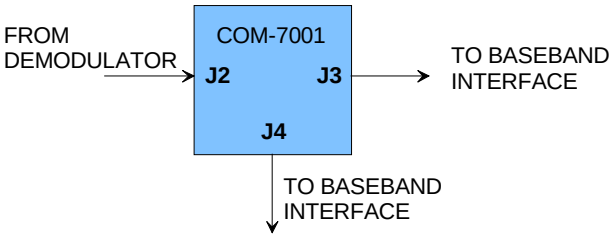
Full duplex mode

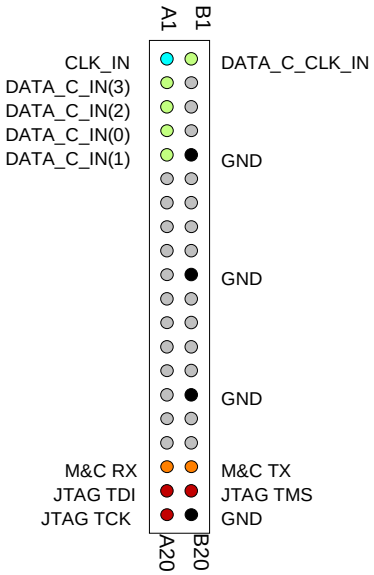


Encoder-only mode



Decoder-only mode



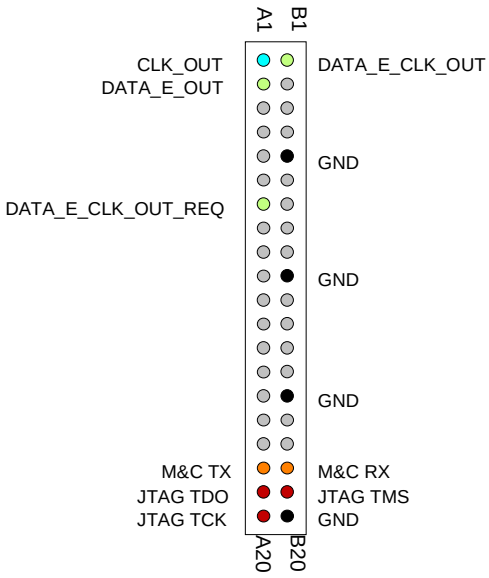


Interface with demodulator

The decoder input is designed for direct connection with the following modules:

COM-1001 BPSK/QPSK/OQPSK demodulator

COM-1011/1018 DSSS Demodulator



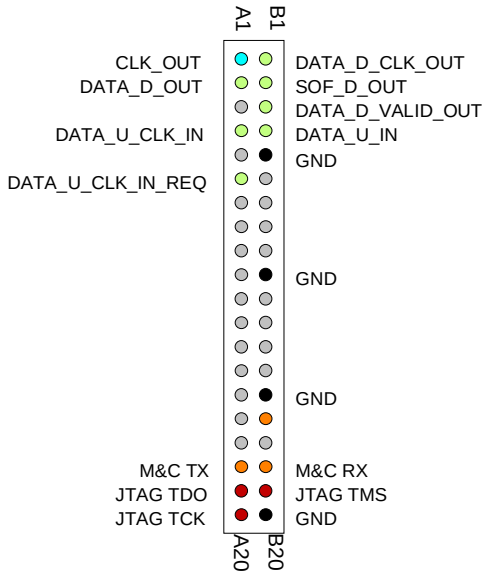
Interface with modulator

The modulator output is designed for direct connection with the following modules:

COM-1002 BPSK/QPSK/OQPSK modulator

COM-1012/1019 DSSS modulator

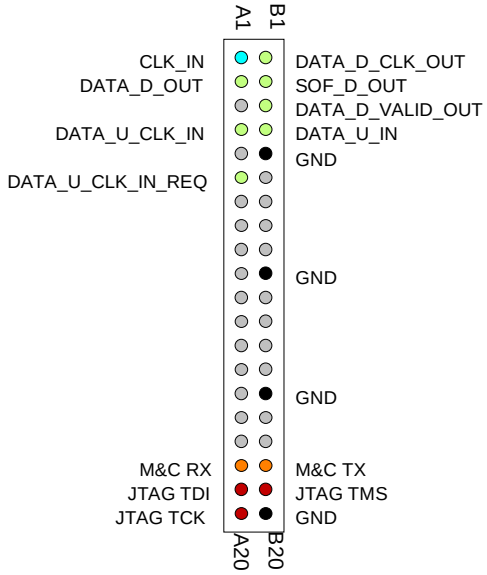
COM-1028 FSK/MSK/GFSK/GMSK modulator



Baseband Interface (J3/J4 Male Connectors)

The baseband interface is designed for direct connection with the following module:

COM-5001 LAN/IP Network Interface



Baseband Interface (J2 Female Connector)

The baseband interface is designed for direct connection with the following module:
COM-5001 LAN/IP Network Interface

I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-5001 LAN/IP Network Interface	COM-5001 LAN/IP Network Interface
COM-1001 BPSK/QPSK/OQPSK demodulator	COM-1002 BPSK/QPSK/OQPSK modulator
COM-1011/1018 DSSS demodulator	COM-1012/1019 DSSS modulator
COM-1027 FSK/MSK/GFSK/GMSK demodulator	COM-1028 FSK/MSK/GFSK/GMSK modulator

ComBlock Ordering Information

COM-7001 TURBO CODE ENCODER / DECODER

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