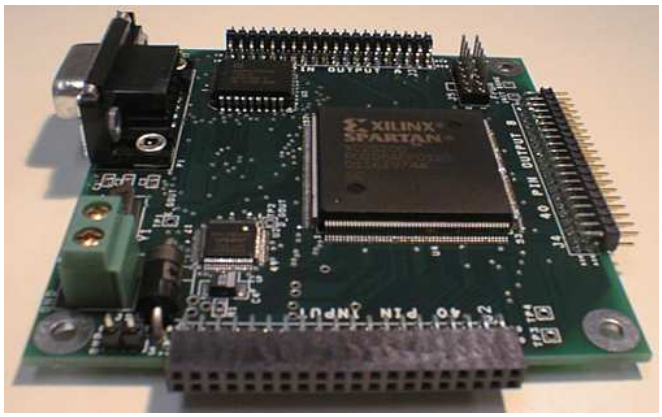
COM-7002 TURBO CODE
ERROR CORRECTION ENCODER / DECODER



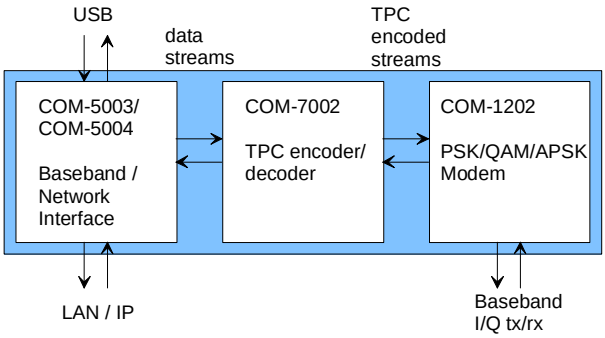
Key Features

- Full duplex turbo code encoder / decoder.
- Rate: 0.25 to 0.97.
- Block length: 64 bits to 4 Kbits.
- Speed up to 11.7 Mbps.
- Automatic frame synchronization.
- 4-bit soft-quantization input.
- Includes unique word for frame synchronization, helical interleaving, scrambling and CRC.
- Built-in BER tester
- Simple software upgrade from the COM-7001.
- Single 5V supply. Connectorized 3”x 3” module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right, bottom). Interfaces with 5V and 3.3V logic.

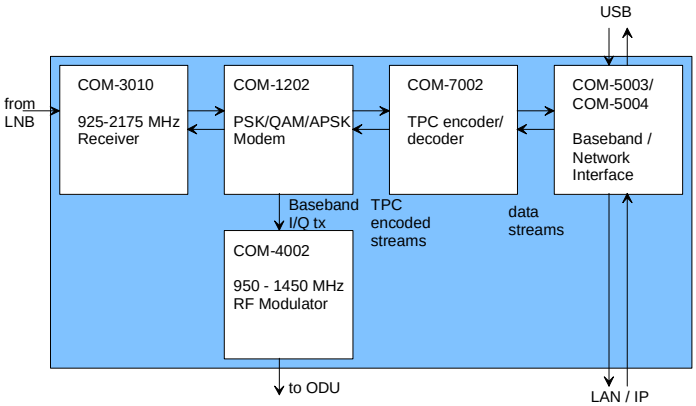
For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com7002.pdf.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.html .

Typical Applications

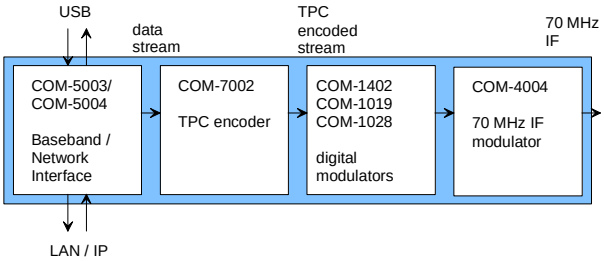


Baseband modem (tx/rx)

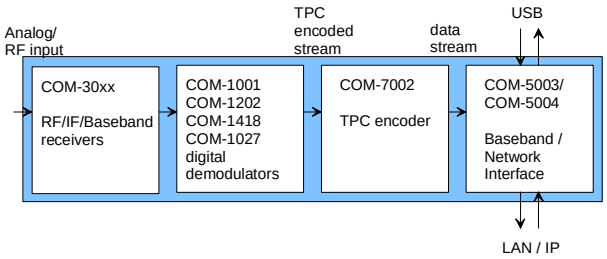


RF modem (tx/rx)

MSS • 18221-A Flower Hill Way • Gaithersburg, Maryland 20879 • U.S.A.
Telephone: (240) 631-1111 Facsimile: (240) 631-1676 www.ComBlock.com
 Issued 5/4/2013

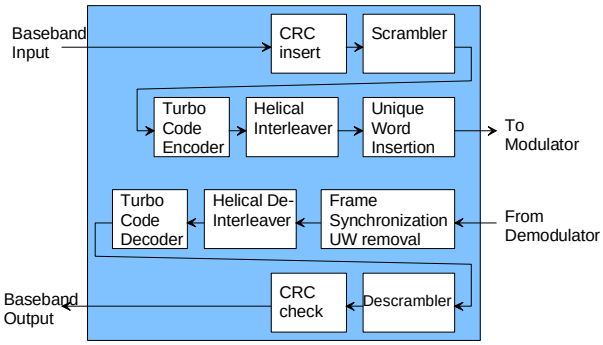


70 MHz IF modulator (tx-only)



Analog/RF receiver (rx-only)

Block Diagram



Turbo Codes

Two-dimensional and three-dimensional turbo codes are supported. The constituent code for each dimension is chosen among the following :

Hamming	Parity
	(4,3)
(8,4)	(8,7)
(16,11)	(16,15)
(32,26) [2D only]	(32,31) [2D only]
(64,57) [2D only]	(64,63) [2D only]

There are two key restrictions in selecting the 2D or 3D codes :
(a) the third dimension code is limited to a maximum length of 16 bits.
(b) the maximum block size (including the CRC) is 4096 bits.

Below are a few examples of code selection and the resulting block size and code rate.

Code	Block size (bits)	Rate
2D (64,57)x(64,57)	4096	0.793
3D (32,26)x(32,26)x(4,3)	4096	0.495
3D (16,11)x(16,11)x(16,11)	4096	0.325
2D (8,4)x(8,4)	64	0.25

The overall ability to correct errors is affected by the code rate, the block size and the number of iterations at the decoding end. A high number of iterations will reduce the throughput but increase the error correction capability. It the data rate is set above the capabilities of the decoder, the number of decoding iterations will be automatically reduced.

Below are a few examples of code selection, the resulting coding gain at 10^{-6} BER and data throughput , assuming 6 decoding iterations :

Code	Coding gain @ 10^{-6} BER	Throughput (encoded / decoded) in Mbit/s
2D (64,57)x(64,57)	7.3 dB	11.7/9.2
3D (32,26)x(32,26)x(4,3)	8.1 dB	10.4/5.1
3D (16,11)x(16,11)x(16,11)	8.5 dB	11.0/3.5

Utilities to help with the selection of turbo codes and the computation of block length, rate and coding gain can be found at www.aha.com.

Electrical Interfaces

Coded data input (from demodulator)	Definition
DATA_C_IN[3:0]	Coded data input (typically from a demodulator). 4-bit soft quantized. Unsigned representation.
SAMPLE_C_CLK_IN	Input sample clock. One CLK_C_IN-wide pulse. Read input data at rising edge of CLK_C_IN when SAMPLE_C_CLK_IN = '1'
CLK_C_IN	Input clock. Maximum frequency is 90 MHz.

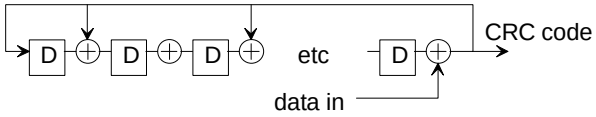
Decoded Output (to baseband interface)	**Definition**
DATA_D_OUT	Decoded data bit.
SAMPLE_D_CLK_OUT	Decoded bit clock. One CLK_OUT-wide pulse. Read output data at rising edge of CLK_OUT when SAMPLE_D_CLK_OUT = '1'
SOF_D_OUT	Code block synchronization pulse. One CLK_OUT-wide pulse, aligned with SAMPLE_D_CLK_OUT for the first bit of the frame (code block).
DATA_D_VALID_OUT	Indicates whether residual errors were found in the PREVIOUS frame after error correction based on the CRC check (when enabled). Read at the following start of frame when FRAME_SYNC = '1'.
Uncoded data input (from baseband interface)	**Definition**
DATA_U_IN	Uncoded data to be transmitted over noisy channel.
SAMPLE_U_CLK_IN	Input bit clock. One CLK_U_IN-wide pulse. Read input data at rising edge of CLK_U_IN when SAMPLE_U_CLK_IN = '1'
SAMPLE_U_CLK_IN_REQ	Output. One CLK_U_IN - wide pulse. Requests a sample from the module upstream. For flow-control purposes.
CLK_U_IN	Input clock. Maximum frequency is 90 MHz.
Encoded data output (to modulator)	**Definition**
DATA_E_OUT	Encoded data to be transmitted over noisy channel.
SAMPLE_E_CLK_OUT	Output bit clock. One CLK_OUT-wide pulse. Read input data at rising edge of CLK_OUT when SAMPLE_E_CLK_OUT = '1'
SOF_E_OUT	Code block synchronization pulse. One CLK_OUT-wide pulse, aligned with SAMPLE_E_CLK_OUT for the first bit of the frame (code block).
SAMPLE_E_CLK_OUT_REQ	Input. One CLK_OUT-wide pulse. Sample request from the module downstream (modulator). For flow-control purposes.
Ancillary Signals	**Definition**
CLK_OUT	Output clock for the output signals on connectors J2/J3. Fixed frequency $\mathbf{f_{clk}}$ of 40 MHz.
Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the data throughput. The maximum power consumption is 300mA.

Operations

CRC check

The Cyclic Redundancy Code is used to detect blocks which contain uncorrected errors. A 16-bit or 32-bit CRC is appended to the data in each block. In applications where spectral efficiency is important, the CRC check can be disabled by software command.

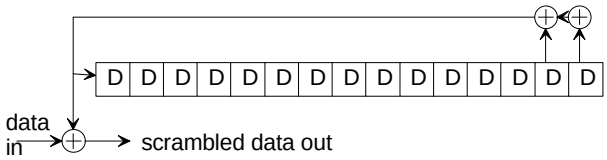
The generic form of the CRC code generator is shown below:



Two standard CRC encoders are available: CCITT 16-bit CRC and 32-bit CRC. The feedback taps are 0x1 10 21 and 0x1 04 C1 1D B7 respectively. The MSB is the leftmost tap on the generic CRC code generator shown above.

Scrambling

A scrambler can be used to randomize the transmitted bit pattern. The scrambler is a 16-bit linear feedback shift register with generator polynomial $1 + x^{14} + x^{15}$.



The scrambler/descrambler is reset at each frame. The seed value (contents of the register upon reset) is 0x5210, where the MSB is in the rightmost register 15. The scrambling and descrambling feature can be enabled or disabled by software command.

Unique Word

By nature, the turbo-code FEC is a block code: coded data is packetized into blocks/frames. The decoder cannot operate without first recovering the frame boundaries. In order to help recovering the frame synchronization at the receiver, the transmitter inserts periodic preambles between frames. The preamble is referred to as “unique word”.

The unique word is 32-bit long:
01011010 00001111 10111110 01100110 (binary)
0x 5A 0F BE 66 (hex)
The most significant bit (left-most) is transmitted first.

In order to limit the bandwidth expansion to less than 5%, the unique word transmission frequency depends on the code block size:

Code block size	UW transmission rate
≥ 1024 bits	Once every block
≥ 512 bits and < 1024 bits	Once every two blocks
≥ 256 bits and < 512 bits	Once every four blocks
< 256 bits	Once every eight blocks

The unique word is not error corrected.

The unique word transmission or reception can be disabled by software command. This can be useful in configurations where frame synchronization references are available externally.

If unique word synchronization is enabled, the 32-bit unique word is removed from the received data stream prior to error correction.

Configuration

An entire ComBlock assembly comprising several ComBlock modules can be monitored and controlled centrally over a single connection with a host computer. Connection types include built-in types:

- Asynchronous serial (DB9)

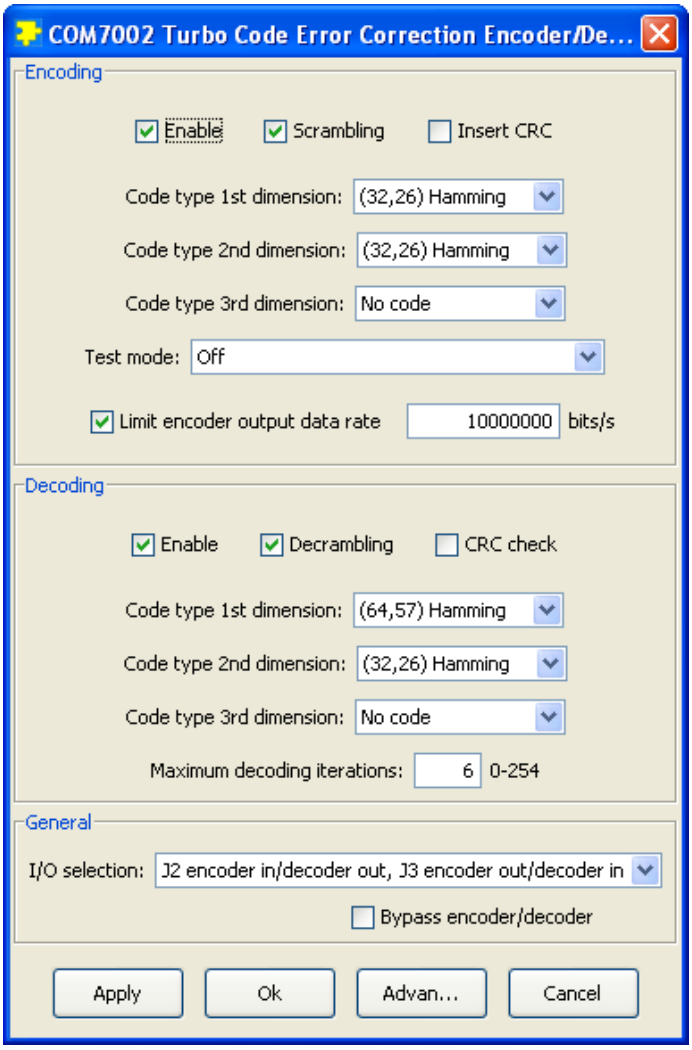
or connections via adjacent ComBlocks:

- USB
- TCP-IP/LAN,
- Asynchronous serial (DB9)
- PC Card (CardBus, PCMCIA).

The module configuration is stored in non-volatile memory.

Configuration (Basic)

The easiest way to configure the COM-7002 is to use the **ComBlock Control Center** software supplied with the module on CD. In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-7002 module to be configured, next click the *Settings* button to display the *Settings* window shown below.



Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write.

Definitions for the Control registers and Status registers are provided below.

Control Registers

The module configuration parameters are stored in volatile (SRT command) or non-volatile memory (SRG command). All control registers are read/write.

This module operates at a fixed internal clock rate $\mathbf{f_{clk}}$ of 40 MHz.

Undefined control registers or register bits are for backward software compatibility and/or future use. They are ignored in the current firmware version.

Parameters	Attributes
Mode	00 = full duplex 01 = encoder only 10 = decoder only REG0 bits 2-1
CRC insertions (transmitter side)	00 = off 01 = 16-bit on 10 = 32-bit on REG0 bits 4-3
CRC check (receiver side)	00 = off 01 = 16-bit on 10 = 32-bit on REG0 bits 6-5
Scrambling (transmitter side)	0 = off 1 = on REG0 bit 7
Scrambling (receiver side)	0 = off 1 = on REG1 bit 0
Tx unique word	0 = off 1 = on REG1 bit 1
Rx unique word synchronization and removal.	0 = off 1 = on REG1 bit 2
Turbo code bypass mode	When set, bypasses the turbo product code at both the encoder and decoder. Connects Uncoded side (_U) to Encoded side (_E). Connects Coded side (_C) to Decoded side (_D). Note: soft-quantized bits are lost in the process. Only the most signicant bit is kept. 0 = off 1 = on REG1 bit 3

Internal pattern generation (test mode)	00 = test mode disabled 01 = counting sequence: When set, the baseband input is disabled and a periodic pattern is internally generated at the encoder input. The pattern consists of an 8-bit counter, MSB transmitted first. 10 = internal generation of a PRBS-11 2047-bit periodic pseudo-random bit sequence as Turbo code encoder input. (overrides external input bit stream). This test mode is typically used to measure end-to-end BER over a transmission channel. The test pattern bit rate is automatically set by the module downstream (typically a modulator) as part of the flow control mechanism, unless limited herein in REG9(6). REG1 bits 5-4
Encoder code X-axis (1st dimension)	0000 = no code 0011 = (8,4) Hamming 0100 = (16,11) Hamming 0101 = (32,26) Hamming 0110 = (64,57) Hamming 1010 = (4,3) parity code 1011 = (8,7) parity code 1100 = (16,15) parity code 1101 = (32,31) parity code 1110 = (64,63) parity code REG2 bits 3-0
Encoder code Y-axis (2nd dimension)	Same definition as above. REG2 bits 7-4
Encoder code Z-axis (3rd dimension)	Same as above but limited to codes of length 16 or less. REG3 bits 3-0
Encoder code block size (**U**nencoded block size)	Function of the code selection and the CRC selection above. For example if a 3D code (4,3)x(8,7)x(16,15) is used in conjunction with 32-bit CRC, the block length is 3x7x15 – 32 = 283. This field must always be defined (even when configured in decoder-only mode). REG3 bits 7-4 (LSB) REG4 bits 7-0
Decoder code X-axis (1st dimension)	Same definition as for tx code. Receiver codes can be selected independently of transmitter codes. REG5 bits 3-0
Decoder code Y-axis (2nd dimension)	Same definition as above REG5 bits 7-4
Decoder code Z-axis (3rd dimension)	Same as above but limited to codes of length 16 or less. REG6 bits 3-0
Decoder code block size (**C**oded block size)	Function of the code selection. For example if a 3D code (4,3)x(8,7)x(16,15) is used, the block length is 4x8x16 = 512. Maximum size is 4096. Special case: 0 means 4096 This field must always be defined (even when configured in encoder-only mode). REG6 bits 7-4 (LSB) REG7 bits 7-0
Turbo code decoder maximum number of iterations	1 – 254. Typical settings is 6. Special case: 0 = the decoder outputs the hard decision value for each bit without correction. REG8 bits 7-0
Encoder data rate internal / external selection	In most cases, the COM-7002 encoder output data rate is determined by modules downstream (for example a modulator). There are, however, cases when the encoder output data rate is set using an internal NCO (for example when testing turbo code encoder and decoder back to back). 0 = external. Encoder output bit rate is based on SAMPLE_E_CLK_OUT_REQ bit requests from following module. 1 = internal. Output bit rate is selected internally by the NCO frequency set in REG10/11/12. Bit requests SAMPLE_E_CLK_OUT_REQ are ignored. REG9 bit 6
Maximum Encoder output data rate	Internal generation of the encoder output data rate. Ignore this field when the output data rate is determined by modules downstream. 24-bit signed integer (2's complement representation) expressed as fsymbol rate * 2^{24} / $\mathbf{f_{clk}}$. The internal processing clock $\mathbf{f_{clk}}$ is typically 40 MHz. REG10 = bits 7-0 (LSB) REG11 = bits 15 – 8 REG12 = bits 23 – 16 (MSB)

I/O selection	0 = J2 as baseband interface: (**U**ncoded in, **D**ecoded out) J3 as modem interface: (**C**oded in, **E**ncoded out) 1 = J2 as modem interface: (**C**oded in, **E**ncoded out) J3 as baseband interface: (**U**ncoded in, **D**ecoded out) 2 = J2 as demodulator interface (**C**oded in) J4 as modulator interface (**E**ncoded out) J3 as baseband interface: (**U**ncoded in, **D**ecoded out) REG13 bits 7-0

(Re-)Writing to control register REG13 is recommended after a configuration change to enact the change (Note: this is done automatically when using the graphical user interface).

Status Registers

Digital status registers are read-only.

Parameters	**Monitoring**
Channel bit error rate	Bit errors counted over 1024 uncorrected bits (unique word). This measurement is refreshed every 16 frames. SREG13: bits 7-0 SREG14: bits 15-8
Number of errors corrected in each frame	SREG15: bits 7-0 SREG16: bits 11-8
CRC check	0 = pass 1 = fail SREG16 bit 4
BER Tester	
Parameters	**Monitoring**
Bit Errors	Bit errors can be counted at the decoder output when a PRBS-11 test sequence is transmitted. Number of bit errors in a 1,000,000 bit window. SREG17: error_count[7:0] (LSB) SREG18: error_count[15:8] SREG19: error_count[23:16] (MSB) The bit errors counter is updated once every periodic measurement window. Reading the value will not reset the counter.
Cumulative number of decoded bit errors	Cumulative number of bits at the decoder output. SREG20 (LSB) SREG21, SREG22 SREG23(MSB)
Cumulative number of decoded bits	Cumulative number of bits at the decoder output. SREG24 (LSB) SREG25, SREG26 SREG27(MSB)

Note: multi-byte values are latched upon reading status register SREG13

Test Points

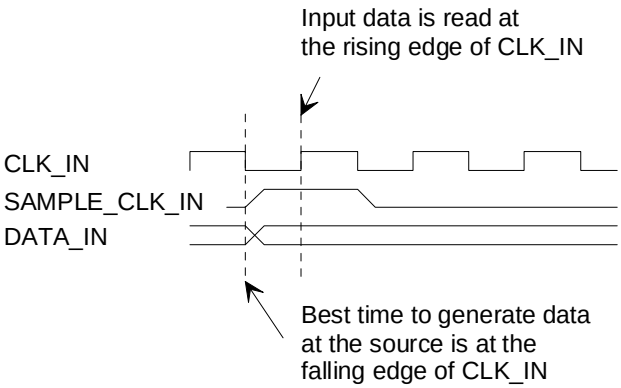
Test points are provided for easy access by an oscilloscope probe.

Test Point	**Definition**
TP1 (E_GOUT)	'1' when the turbo code encoder data path is empty and not processing a block. '0' otherwise. Use this test point to assess the encoder utilization ratio.
TP2 (D_GOUT)	'1' when the turbo code decoder data path is empty. Use this test point to assess the decoder utilization ratio.
TP3	Receive unique word synchronization. '1' when a unique word is detected with less than 10% bit errors (at least 28 matching bits out of 32).
TP4	Bit error detected by BER tester after decoding. Valid only when a PRBS-11 test sequence is sent by the encoder.
INIT	Unique word transmit enable. Provides some indication as to the encoded frame period.
J4/B7*	Receive frame synchronization. Solid '1' when receiving periodic frame preambles at the right time. '0' or toggling otherwise.
J4/B8*	'1' when encoder input buffer contains at least a full frame of data ready to encode, '0' otherwise.
J4/B9*	'1' when encoder output buffer contains data, '0' when empty
J4/B11*	'1' when decoder input buffer contains a full frame of data ready to decode, '0' otherwise.
J4/B12*	'1' when decoder output buffer contains data, '0' when empty.

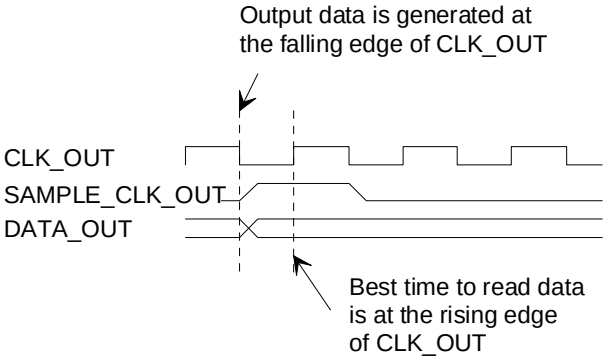
(*)-These special test points on connector J4 are enabled only when REG9(7) = '1'. High impedance otherwise.

Timing

Input



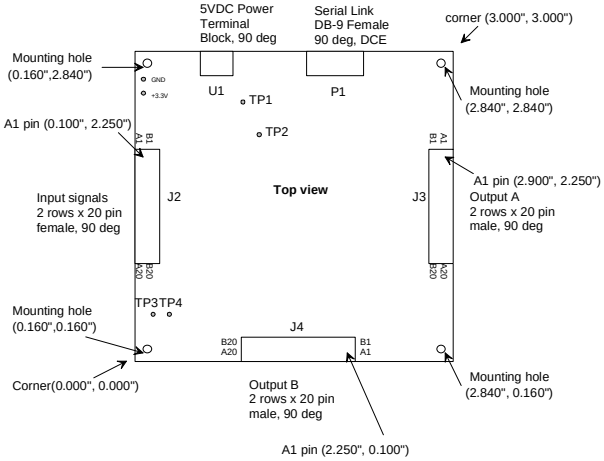
Output



Schematics

The hardware schematics are available on the ComBlock CD shipped with every module as \Hardware Schematics\com_7001schematics.pdf

Mechanical Interface



Mounting hole diameter: 0.125"

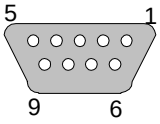
A1 pin height: 0.039"

Maximum height 0.500"

Pinout

Serial Link P1

The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.

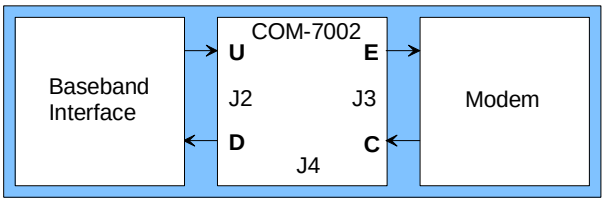


DB-9 Female

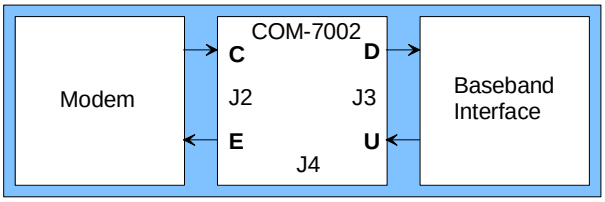
2 Transmit
3 Receive
5 Ground

Input / Output Connectors

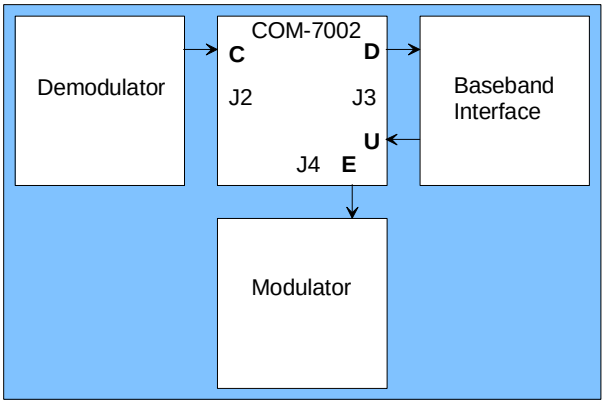
The pinout for the 40-pin input / output connectors can be selected by software command (REG13) among several possible configurations:



REG13 = 0

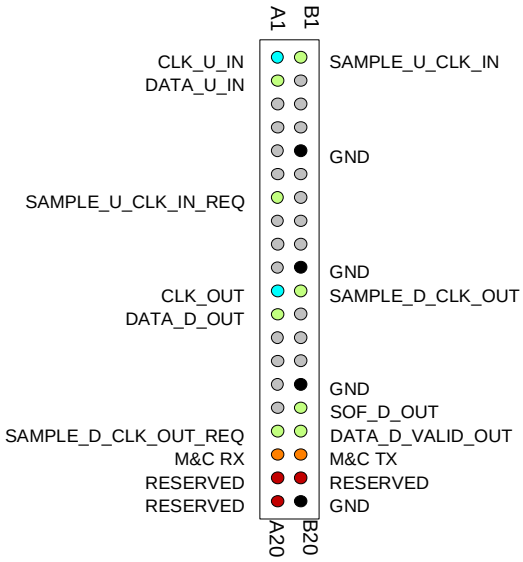


REG13 = 1

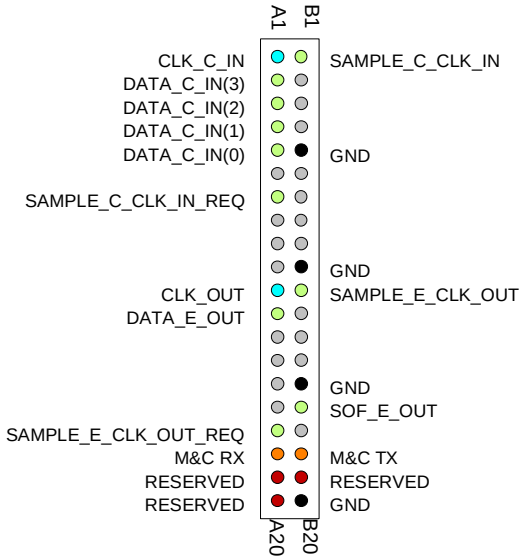


REG13 = 2

Connector J2

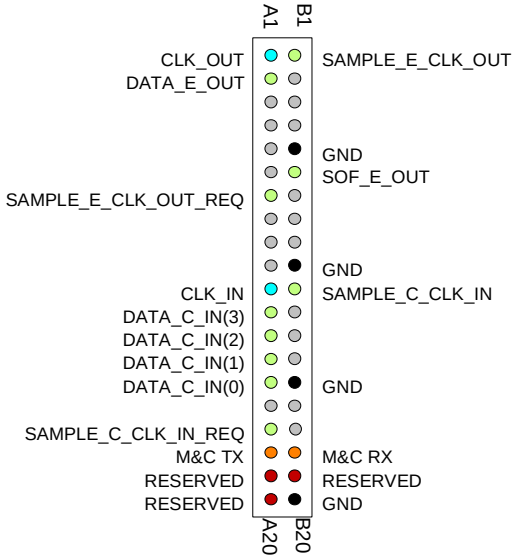


REG13 = 0 J2 as baseband interface

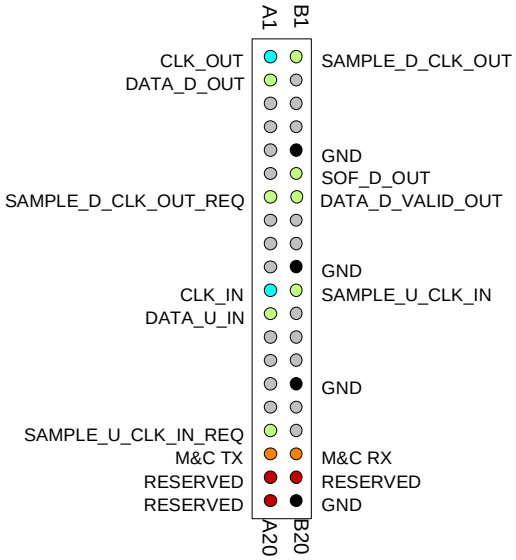


REG13 = 1,2 J2 as modem interface

Connectors J3 / J4



REG13 = 0 J3 as modem interface



REG13 = 1 J3 as baseband interface

I/O Compatibility List

(not an exhaustive list)

COM-5003 TCP-IP / USB gateway
COM-5004 IP router
COM-1202/1203 PSK/QAM/APSK modem
COM-1518 DSSS demodulator
COM-1027 FSK/MSK/GFSK/GMSK demodulator
COM-1402 PSK/QAM/APSK modulator
COM-1519 DSSS modulator
COM-1028 FSK/MSK/GFSK/GMSK modulator
COM-1x00 FPGA/ARM development platforms FPGA development platforms

Configuration Management

This specification document is consistent with the following software versions:
COM-7002 FPGA firmware: Version 4 and above.
ComBlock Control Center graphical user interface: Revision 3.0.6h and above.
These software versions can be downloaded from www.comblock.com/download.html

Comparison with Previous ComBlocks

Key Improvements with respect to COM-7001 TPC encoder/decoder
The COM-7002 emphasises bi-directional encoding/decoding thus significantly reducing the number of ComBlocks needed for building full-duplex communication equipment. Other bi-directional ComBlock modules include the COM-5003, COM-5004, COM-1202 and more to come. Existing COM-7001 users can upgrade (free) to the COM-7002 by reprogramming the flash memory with the latest COM-7002 firmware.

ComBlock Ordering Information

COM-7002 TURBO CODE ENCODER / DECODER

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Gaithersburg, Maryland 20879 • U.S.A.
Telephone: (240) 631-1111
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