COM-7003 TURBO CODE ERROR CORRECTION ENCODER / DECODER

Key Features

- Full duplex turbo code encoder / decoder.
- Flexible dynamic (i.e. at runtime) user-selected configuration:
  - Block length up to 2032 bits
  - Puncturing patterns for rates 1/3,1/2,2/3,3/4,4/5,5/6,6/7
- Speed up to 16.5 Mbps (payload bits)
- Frame error rate examples:
  - 2032-bit frame, Rate 1/3, soft-quantization, 15-iterations:
    FER = 10^{-2} @ E_b/N_o = 1.4 dB
    FER = 10^{-3} @ E_b/N_o = 1.6 dB
  - 768-bit frame, Rate 3/4, soft quantization, 15-iterations:
    FER = 10^{-2} @ E_b/N_o = 3.1 dB
    FER = 10^{-3} @ E_b/N_o = 3.5 dB
- Automatic frame synchronization.
- optional 16-bit CRC insertion and frame error detection/suppression.
- 4-bit soft-quantization decoder input.
- I/Os:
  - High-speed connector for clock synchronous interface
  - Gigabit Ethernet LAN RJ-45 with TCP server
- Built-in frame error rate counter, BER tester, and PRBS11 test sequence generator.
- Connectorized 3”x 3.5” module for ease of prototyping. Single 5V supply with reverse voltage and overvoltage protection. Interfaces with 3.3V LVTTL logic.

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com7003.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.html .

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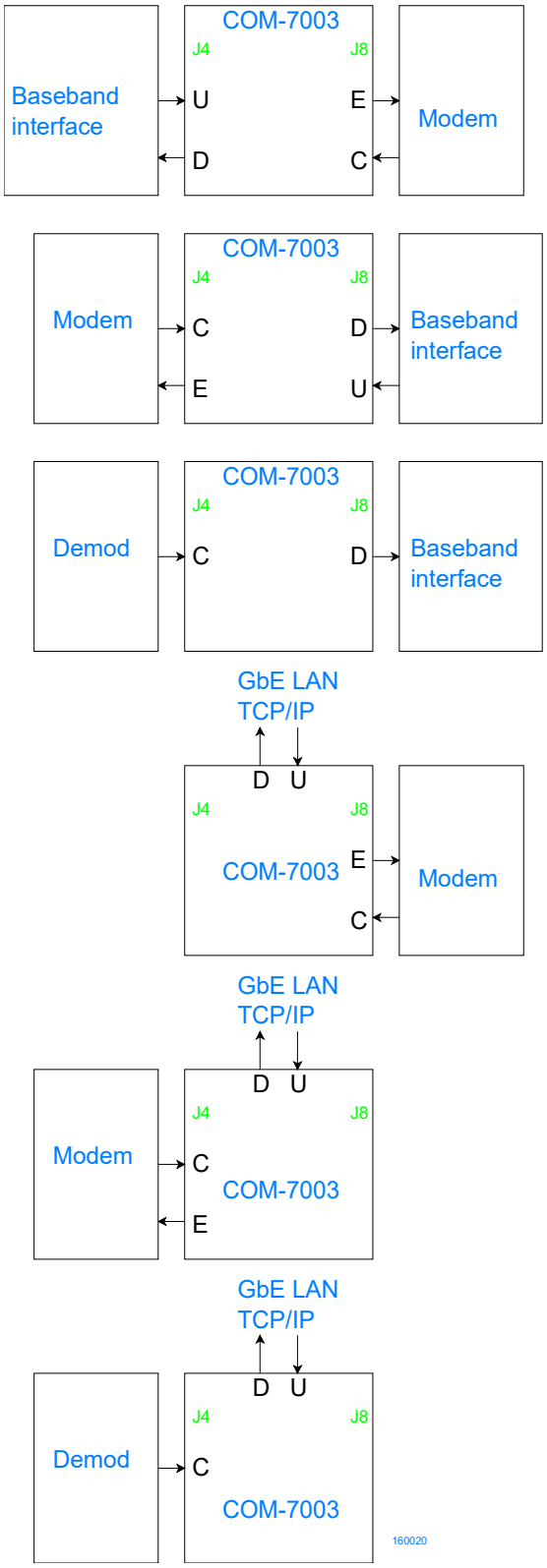
Applications

Encoder: Uncoded (_U) input, Encoded (_E) output
Decoder: Coded (_C) input, Decoded (_D) output.



Electrical Interfaces

Operating input voltage range

Supply voltage	+4.5V min, +12V max

Absolute Maximum Ratings

Supply voltage	-0.5V min, +20V max
98-pin connector inputs	-0.5V min, +3.6V max

Important:
The I/O signals connected directly to the FPGA are NOT 5V tolerant!

Coded data input (from demodulator)	**Definition**
DATA_C_IN[3:0]	Coded data input (typically from a demodulator). 4-bit soft quantized. Unsigned representation. 0000 represents a strong 0 1111 represents a strong 1 0111 represents a weak 0 1000 represents a weak 1
DATA_C_VALID_IN	Coded data input valid. One CLK_C_IN-wide pulse. Read input data at rising edge of CLK_C_IN when DATA_C_VALID_IN = '1'
DATA_C_CTS_OUT	Flow control output signal (Clear To Send). One CLK_C_IN -wide pulse. Requests a sample from the modem upstream.
CLK_C_IN	Input clock. Maximum frequency is 160 MHz.

Decoded Output (to baseband interface)	**Definition**
DATA_D_OUT	Decoded data bit
DATA_D_VALID_OUT	Decoded data valid. One CLK_OUT-wide pulse. Read output data at rising edge of CLK_OUT when DATA_D_VALID_OUT = '1'
SOF_D_OUT	Code block synchronization pulse. One CLK_OUT-wide pulse, aligned with DATA_D_VALID_OUT for the first bit of the decoded frame (code block).
DATA_D_CTS_IN	Flow control input signal (Clear To Send). One CLK_OUT -wide pulse. Requests more data from the decoder.
Uncoded data input (from baseband interface)	**Definition**
DATA_U_IN	Uncoded data to be transmitted over noisy channel.
DATA_U_VALID_IN	Uncoded data valid. One CLK_U_IN-wide pulse. Read input data at rising edge of CLK_U_IN when DATA_U_VALID_IN = '1'
DATA_U_CTS_OUT	Flow control output signal (Clear To Send). One CLK_U_IN -wide pulse. Requests a sample from the module upstream.
CLK_U_IN	Input clock. Maximum frequency is 160 MHz.
Encoded data output (to modulator)	**Definition**
DATA_E_OUT	Encoded data to be transmitted over noisy channel.
DATA_E_VALID_OUT	Encoded data valid output. One CLK_OUT-wide pulse. Read input data at rising edge of CLK_OUT when DATA_E_VALID_OUT = '1'
SOF_E_OUT	Encoded block start of frame pulse. One CLK_OUT-wide pulse, aligned with DATA_E_VALID_OUT for the first bit of the encoded frame (code block).
DATA_E_CTS_IN	Flow control input signal (Clear To Send). One CLK_OUT -wide pulse. Requests more data from the encoder.
Ancillary Signals	**Definition**
CLK_OUT	Output clock for the output signals on connectors J4/J8. Fixed frequency $\mathbf{f_{clk}}$ of 125 MHz.
Power Interface	4.5 – 12VDC. Terminal block. Power consumption is approximately proportional to the data throughput. The maximum power consumption is 300mA.

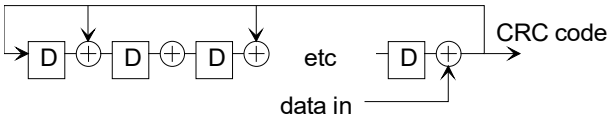
Operations

CRC check

An optional Cyclic Redundancy Code can be used to detect blocks which contain uncorrected errors. A 16-bit CRC is appended to the data in each block. In applications where spectral efficiency is important, the CRC check can be disabled by software command.

When CRC is enabled at both encoder and decoder, the frame error rate can be measured. The decoder tabulates the cumulative number of received frames as well as the cumulative number of frames with bad CRC. This feature is available for any transmitted sequence.

The CRC16 used is described by its generator polynomial: $x^{16} + x^{15} + x^2 + x^0$ (same as USB)
The generic form of the CRC code generator is shown below.



The MSB is the leftmost tap on the generic CRC code generator shown above.

Decoded frames with bad CRC are discarded.

Unique Word

By nature, the turbo-code FEC is a block code: coded data is packetized into blocks/frames. The decoder cannot operate without first recovering the frame boundaries. In order to help recovering the frame synchronization at the receiver, the transmitter inserts periodic preambles between frames. The preamble is referred to as “unique word”.

The unique word is 32-bit long:
01011010 00001111 10111110 01100110 (binary)
0x 5A 0F BE 66 (hex)
The most significant bit (left-most) is transmitted first.

In order to limit the bandwidth expansion to less than 5%, the unique word transmission frequency depends on the encoded code block size:

Code block size	UW transmission rate
≥ 1024 bits	Once every block
≥ 512 bits and < 1024 bits	Once every two blocks
≥ 256 bits and < 512 bits	Once every four blocks
< 256 bits	Once every eight blocks

The unique word is not error corrected.

The 32-bit unique word is removed from the received data stream prior to error correction.

Configuration

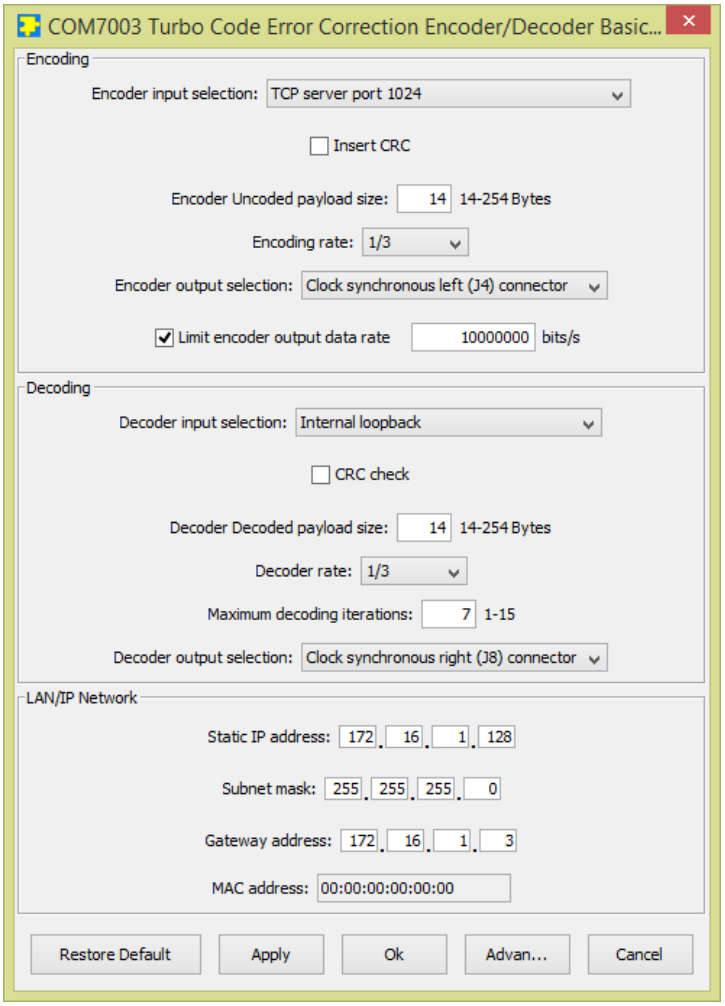
An entire ComBlock assembly comprising several ComBlock modules can be monitored and controlled centrally over a single connection with a host computer. Connection types include built-in types:

- USB
- TCP-IP/LAN

The module configuration is stored in non-volatile memory and automatically reloaded at power-up.

Configuration (Basic)

The easiest way to configure the COM-7003 is to use the **ComBlock Control Center** software supplied with the module on CD. In the **ComBlock Control Center** window detect the ComBlock module(s) by clicking the *Detect* button, next click to highlight the COM-7003 module to be configured, next click the *Settings* button to display the *Settings* window shown below.



Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write.

Definitions for the Control registers and Status registers are provided below.

Control Registers

The module configuration parameters are stored in volatile (SRT command) or non-volatile memory (SRG command). All control registers are read/write.

This module operates at a fixed internal clock rate $\mathbf{f}_{clk}$ of 125 MHz.

Undefined control registers or register bits are for backward software compatibility and/or future use. They are ignored in the current firmware version.

Encoder	
Parameters	**Attributes**
Encoder input selection	0 = encoder bypassed 1 = clock synchronous J4 left connector 2 = clock synchronous J8 right connector 3 = TCP server, port 1024 4 = internal PRBS11 test sequence 5 = 0-255 counting test sequence REG0(2:0)
Encoder output selection	0 = clock synchronous J4 left connector 1 = clock synchronous J8 right connector REG0(5:4)
Turbo code encoder **U**ncoded payload size	Payload size in Bytes. Must NOT be an integer multiple of 15 Maximum 254 Bytes. REG1
Turbo code encoder rate	0 = rate 1/3 1 = rate 1/2 2 = rate 2/3 3 = rate 3/4 4 = rate 4/5 5 = rate 5/6 6 = rate 6/7 REG2(3:0)
CRC insertion	0 = disabled 1 = 16-bit CRC enabled REG2(7)
Turbo code encoder **E**ncoded frame size	Encoded frame size in bits. For example: when payload size is 14, rate 1/3, the encoded frame size is 14*8*3 = 336 bits. Includes optional 16-bit CRC. Does not include any periodic synchronization field. REG3 LSB REG4(4:0) (MSB)

Decoder	
Parameters	**Attributes**
Decoder input selection	0 = decoder bypassed 1 = clock synchronous J4 left connector 2 = clock synchronous J8 right connector 3 = internal loopback REG5(2:0)
Decoder output selection	0 = clock synchronous J4 left connector 1 = clock synchronous J8 right connector 2 = TCP server, port 1024 REG5(5:4)
Turbo code decoder **D**ecoded payload size	Payload size in Bytes. Must NOT be an integer multiple of 15 Maximum 254 Bytes. REG6
Turbo code decoder rate	0 = rate 1/3 1 = rate 1/2 2 = rate 2/3 3 = rate 3/4 4 = rate 4/5 5 = rate 5/6 6 = rate 6/7 REG7(3:0)
CRC detection	0 = disabled 1 = 16-bit CRC detection enabled REG7(7)
Turbo code decoder **C**oded frame size	Coded frame size in bits. For example: when payload size is 14, rate 1/3, the coded frame size is 14*8*3 = 336 bits. Includes optional 16-bit CRC. Does not include any periodic synchronization field. REG8 LSB REG9(4:0) (MSB)
Turbo code decoder maximum number of iterations	1 – 15. Typical settings is 7. Must be an odd number REG10(3:0)
Encoder data rate internal / external selection	In most cases, the COM-7003 encoder output data rate is determined by modules downstream (for example a modulator). There are, however, cases when the encoder output data rate is set using an internal NCO (for example when testing turbo code encoder and decoder back to back). 0 = external. Encoder output bit rate is based on SAMPLE_E_CLK_OUT_REQ bit requests from following module. 1 = internal. Output bit rate is selected internally by the NCO frequency set in REG11/12/13. Bit requests

	SAMPLE_E_CLK_OUT_REQ are ignored. REG0(7)
Maximum Encoder output data rate	Internal generation of the encoder output data rate. Ignore this field when the output data rate is determined by modules downstream. 24-bit signed integer expressed as fsymbol rate * 2^{24} / f_{clk}. REG11 (LSB) - REG13 (MSB)
Ethernet LAN	
Parameters	**Attributes**
IPv4 address	LAN is shared between payload data traffic and monitoring and control. 4-byte IPv4 address. Example : 0x AC 10 01 80 designates address 172.16.1.128 The new address becomes effective immediately (no need to reset the ComBlock). REG14 (MSB) - REG17(LSB)
Subnet mask	Typically 0x FF FF FF 00 (255.255.255.0) REG18 (MSB) – REG21(LSB)
Gateway IP address	Where to forward IP frames not destined to this Local Area Network. REG22 (MSB) - REG25 (LSB)

(Re-)Writing to control register REG26 is recommended after a configuration change to enact the change (Note: this is done automatically when using the graphical user interface).

Status Registers

Digital status registers are read-only.

Parameters	**Monitoring**
Hardware self-check	At power-up, the hardware platform performs a quick self check. The result is stored in status registers SREG0-9 Properly operating hardware will result in the following sequence being displayed: SREG0-SREG7 = 01 F1 1D xx 1F 93 10 22
TCXO reference clock presence	1 = detected 0 = missing SREG8(0)
125 MHz internal clock PLL lock	1 = locked 0 = unlocked SREG8(1)
LAN1 MAC bad CRC counter	SREG9 (LSB) – SREG10(MSB)
MAC address	Unique 48-bit hardware address (802.3). In the form SREG11:SREG12:SREG13:…:SREG16
Channel bit error rate	Bit errors counted over 1024 uncorrected bits (unique word). This measurement is refreshed every 16 frames. Valid for any transmitted sequence, whether test sequence or user payload data. SREG17 (LSB) - SREG18 (MSB)
BER Tester	
Parameters	**Monitoring**
BER tester synchronized	'1' when the BERT is synchronized with the periodic PRBS11 test sequence being transmitted. SREG20(7)
Bit Errors	Bit errors can be counted at the decoder output when a PRBS-11 test sequence is transmitted. Number of bit errors in a 8,000,000 bit window. SREG21: error_count[7:0] (LSB) SREG22: error_count[15:8] SREG23: error_count[23:16] (MSB) Valid only when the BERT is synchronized. (see above) The bit errors counter is updated once every periodic measurement window. Reading the value will not reset the counter.

Frame Errors	
Parameters	**Monitoring**
Cumulative number of decoded frames	Reading the value will not reset the counter. SREG24(LSB)-SREG27(MSB)
Cumulative number of erroneous decoded frames	Bad decoded frames are counted only when the optional CRC is enabled at both encoder and decoder. Works with any transmitted sequence. SREG28(LSB)-SREG31(MSB)

Multi-byte status variables are latched upon (re-)reading SREG7.

Test Points

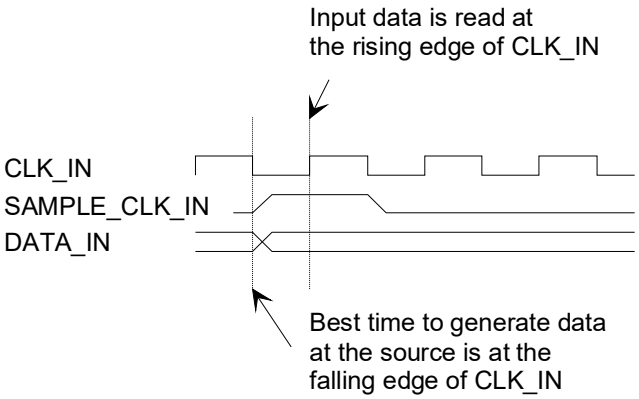
Test points are provided for easy access by an oscilloscope probe.

Test Point	Definition
J8/A29	Receive unique word synchronization. '1' when a unique word is detected with less than 10% bit errors (at least 28 matching bits out of 32).
J8/A30	Outline of receive coded data frame following the unique word
J8/A31	receive coded data bits
J8/A32	Receive frame synchronization. Solid '1' when receiving periodic frame preambles at the right time. '0' or toggling otherwise.
J8/A33	BER tester detection of the start of the 2047-bit periodic PRBS11 pseudo-random test sequence. Only valid when encoding a PRBS11 test sequence.
J8/A34	BER tester synchronized with the incoming PRBS11 test sequence. Only valid when encoding a PRBS11 test sequence.
J8/A35	BER tester byte error. Only valid when encoding a PRBS11 test sequence.
J8/A36	Turbo code decoder input flow control signal. '1' when the decoder is not busy.
J8/A37	Turbo code encoder input flow control signal. '1' when the encoder is not busy.

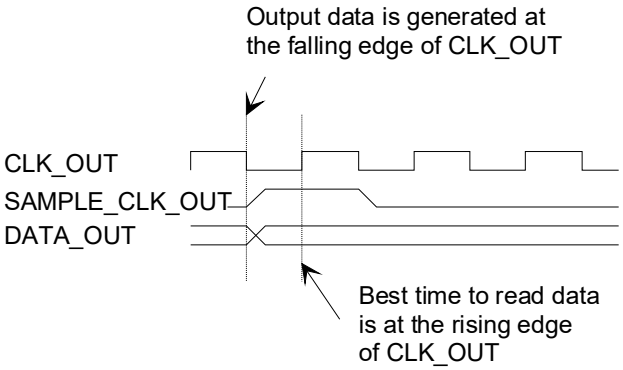
J4/A29	Turbo code decoder frame counter (LSb)
J4/A30	Turbo code decoder valid frame (CRC matches)
J4/A31	Turbo code decoder bad frame (CRC does not match)

Timing

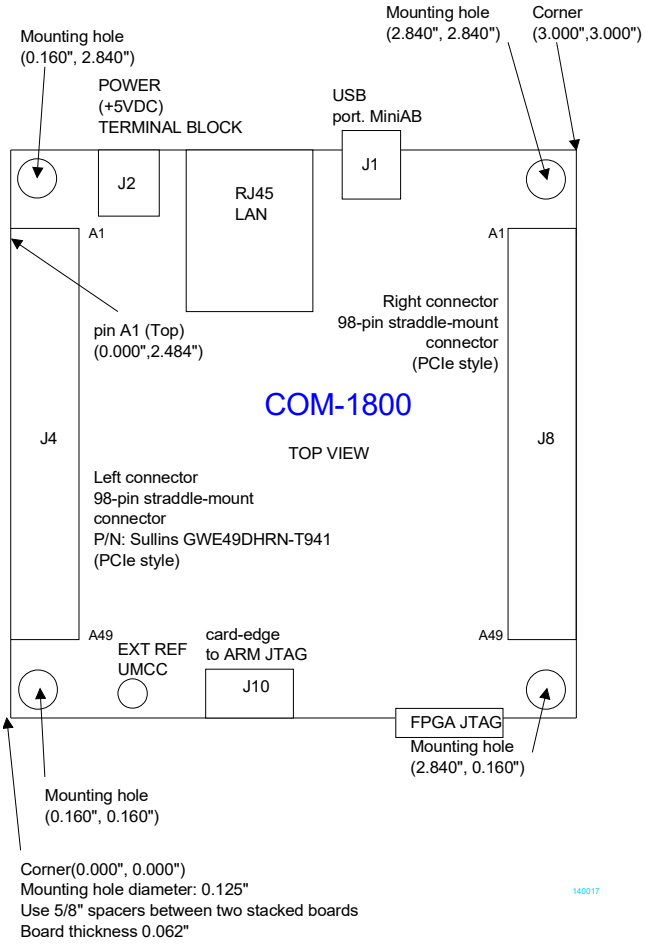
Input



Output



Mechanical Interface



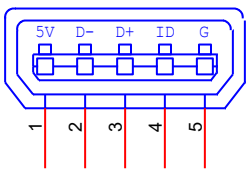
Schematic

The board schematic is available on-line at
ComBlock.com/download/com_1800schematics.pdf

Pinout

USB

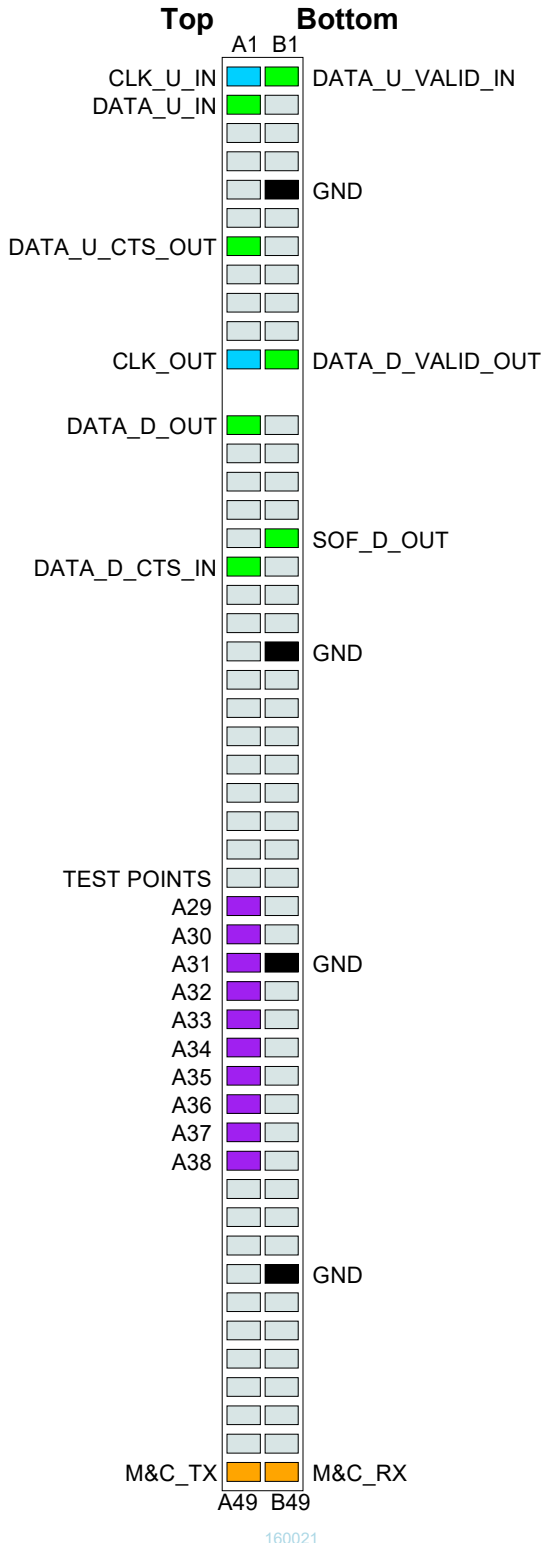
The USB port is equipped with mini type AB connectors. (G = GND). The COM-7003 acts as a USB device.



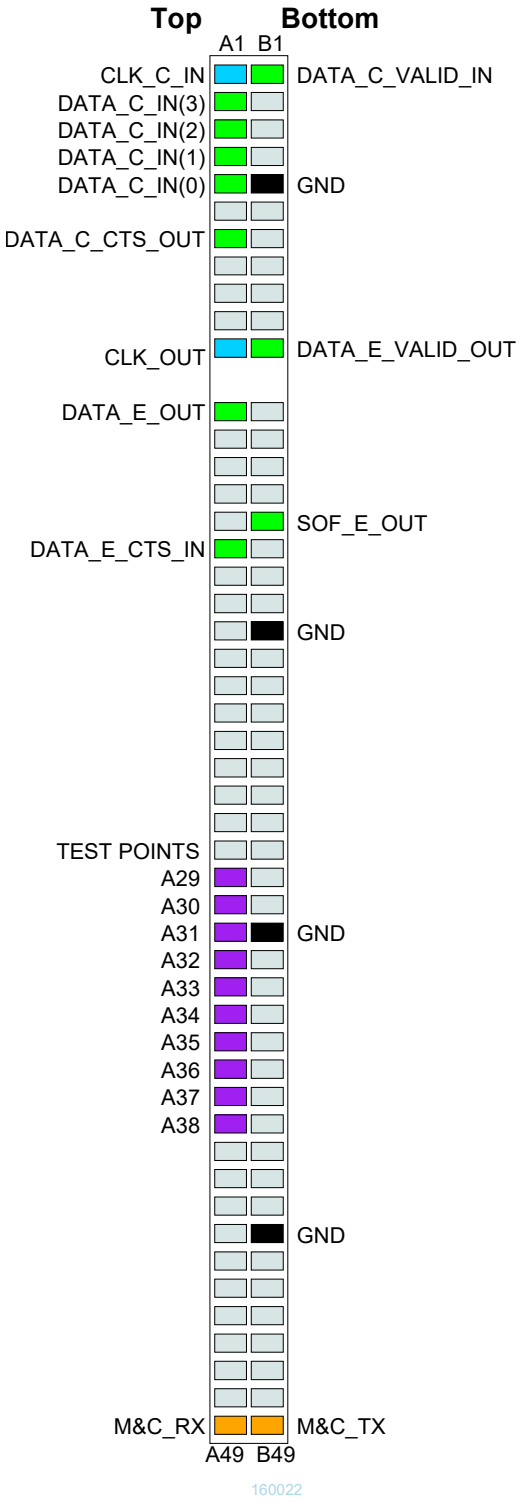
Input / Output Connectors

The pinout for the 98-pin input / output connectors can be selected by software command among several possible configurations:

Left Connector J4

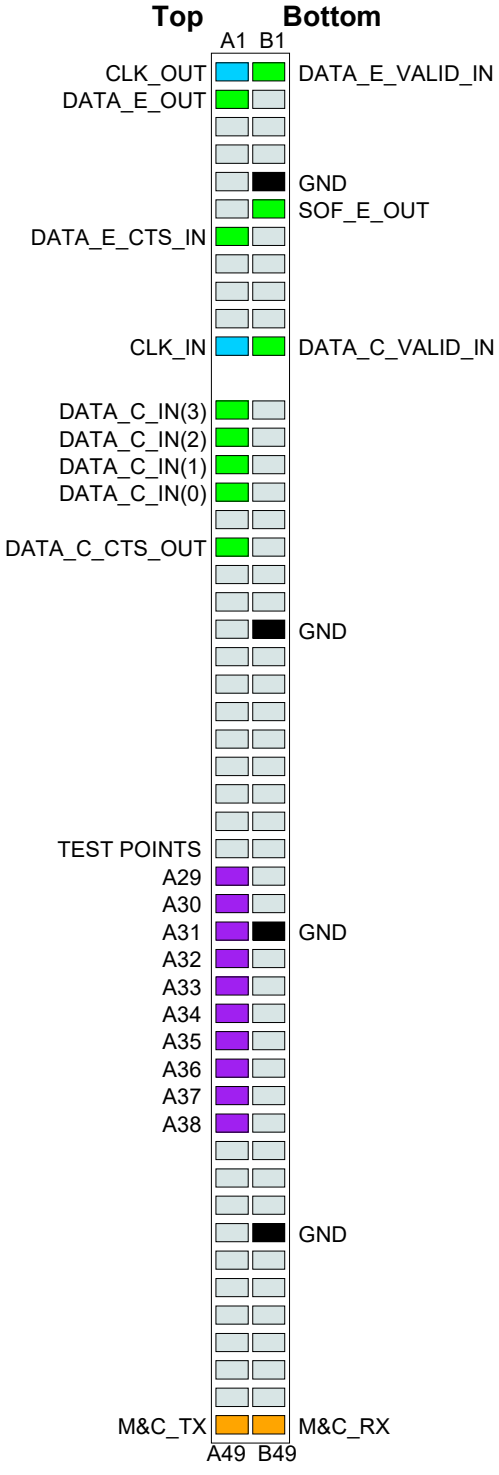


J4 as baseband interface

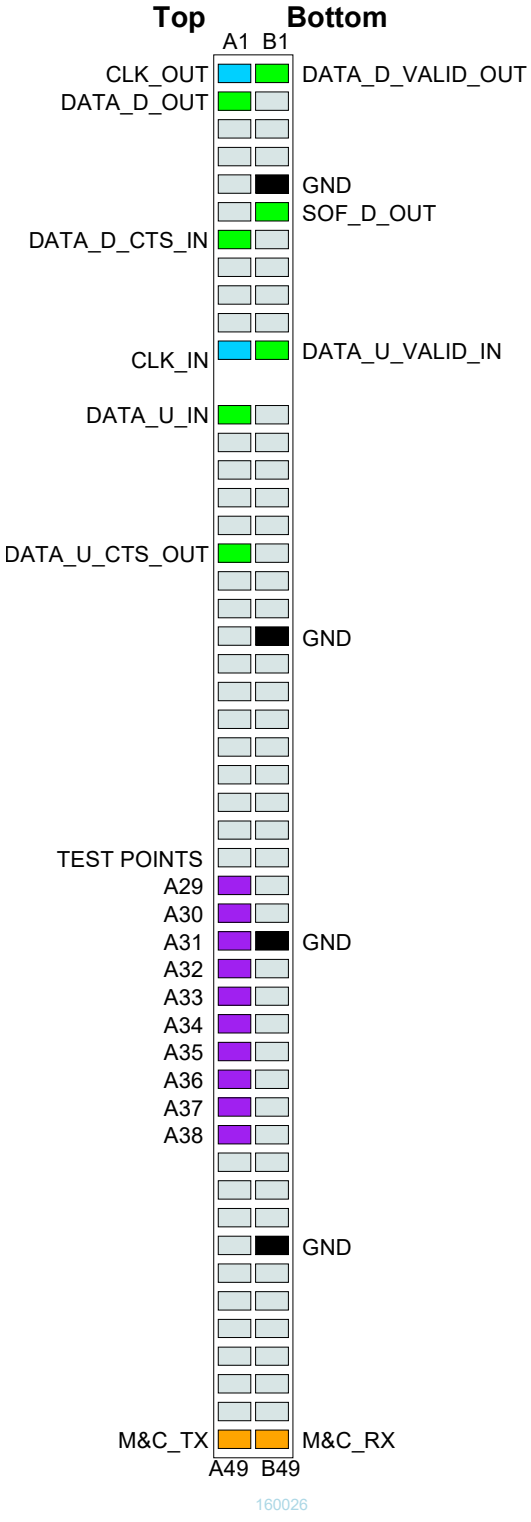


J4 as modem interface

Right Connector J8



J8 as modem interface



J8 as baseband interface

I/O Compatibility List

(not an exhaustive list)

COM-1800 FPGA + GbE LAN development platform
COM-5003 TCP-IP / USB gateway
COM-5004 IP router
COM-1202/1203 PSK/QAM/APSK modem
COM-1518 DSSS demodulator
COM-1519 DSSS modulator

Configuration Management

This specification document is consistent with the following software versions:

COM-7003 FPGA firmware: Version 3 and above.

ComBlock Control Center graphical user interface: Revision 3.12k and above.

These software versions can be downloaded from www.comblock.com/download.html

It is possible to read back the option and version of the FPGA configuration currently active. Using the ComBlock Control Center, highlight the COM-7003 module, then go to the advanced settings. The option and version are listed at the bottom of the configuration panel.

ComBlock Ordering Information

COM-7003 TURBO CODE ENCODER / DECODER

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