COM-7003SOFT
Turbo code encoder/decoder
VHDL source code overview / IP core

Overview

The COM-7003SOFT is an error correction turbo-code encoder/decoder written in generic VHDL.

The entire **VHDL source code** is deliverable.

Key features and performance:

- Flexible dynamic (i.e. at runtime) user-selected configuration:
  - Block length up to 8000 bits
  - Puncturing patterns for rates 1/3,1/2,2/3,3/4,4/5,5/6,6/7,7/8
- Frame error rate examples:
  - 2032-bit frame, Rate 1/3, 5-bit soft quantization, 15-iterations:
    FER = 10^{-2} @ E_b/N_o = 1.4 dB
    FER = 10^{-3} @ E_b/N_o = 1.6 dB
  - 768-bit frame, Rate 3/4, 5-bit soft quantization, 15-iterations:
    FER = 10^{-2} @ E_b/N_o = 3.1 dB
    FER = 10^{-3} @ E_b/N_o = 3.5 dB
- Provided with IP core:
  - VHDL source code
  - Matlab .m file for simulating the encoding and decoding algorithms, for generating stimulus files for VHDL simulation and for end-to-end BER performance analysis at various signal to noise ratios
  - VHDL testbench
- Complies with ETSI EN 301 545-2, DVB-RCS2.

Target Hardware

The code is written in generic standard VHDL so that it can be ported to a variety of FPGAs. The code was developed and tested on a Xilinx 7-series FPGA but is expected to work similarly on other targets.

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Configuration

Synthesis-time configuration parameters

The following constants are user-defined in the decoder component generic section prior to synthesis. These parameters generally define the size of the decoder embodiment.

Synthesis-time configuration parameters	
Parameters	**Configuration**
Number of soft-quantized bits at the decoder input **NQBITS**	Typical values: 4. A minor performance improvement can be achieved with 5-bits.
log2 of the maximum payload size in Bytes, rounded up **NADDRBITS**.	While the actual payload size is user-programmable at run-time, the maximum payload size is an important factor that affects the number of RAM blocks used in the FPGA. For the maximum payload size of 1000 Bytes, set **NADDRBITS** = 10.

Run-time configuration parameters

The user can set and modify the following controls at run-time through the top level component interface:

Parameters	Configuration
Frame size **BURST_PAYLOAD_SIZE**	Uncoded/Decoded frame size, expressed in bytes. Valid range 1 – 1000 Bytes. Constraints: - when using puncturing **BURST_PAYLOAD_SIZE** *4 must be an integer multiple of the puncturing period. - must NOT be an integer multiple of 15.
Encoding rate **R1/R2**	Valid values are 1/3,1/2,2/3,3/4,4/5,5/6,6/7,7/8

I/Os

General

CLK: input
The synchronous clock. The user must provide a global clock (use BUFG). The CLK timing period must be constrained in the .xdc file associated with the project.

SYNC_RESET: input
Synchronous reset. The reset MUST be exercised at least once to initialize the internal variables. It must be exercised whenever a control parameter is changed.

Encoder/Decoder controls

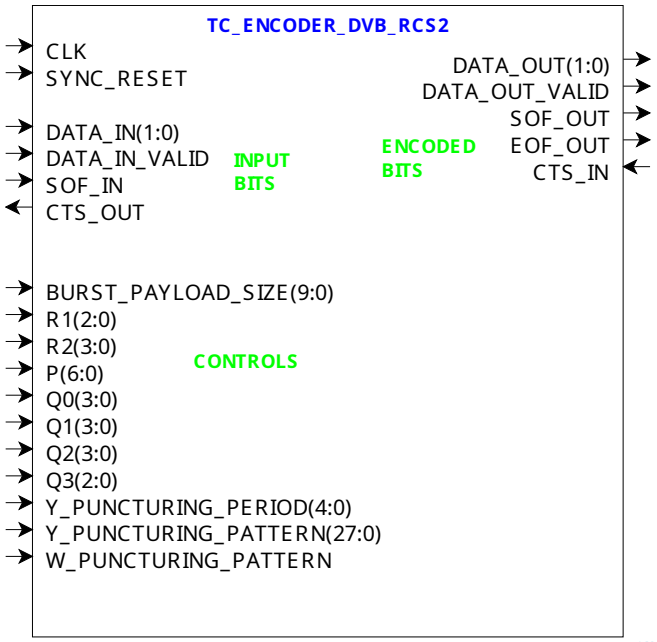
Users can define the encoder and decoder controls with one of two possible levels of abstraction: simple and detailed.

The simplest form is described by the payload size **BURST_PAYLOAD_SIZE** and the code rate **R1/R2**, as described in the run-time configuration section above.

A more detailed configuration consists of several arcane parameters **BURST_PAYLOAD_SIZE**, **P**, **Q0**, **Q1**, **Q2**, **Q3**, **Y_PUNCTURING_PERIOD**, **Y_PUNCTURING_PATTERN**, **W_PUNCTURING_PATTERN**, defined in Table A-1 of [1].

To simplify operation, a VHDL component (DVB_RCS2_CONFIG.VHD) and a Matlab `table1.m` program are provided to look-up stored configurations by waveform ID:
see Annex A Table A-1 Reference Waveforms for Linear Modulation Bursts [1]

Encoder



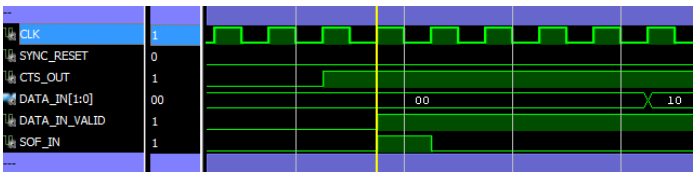
DATA_IN(1:0): Input data is read two bits at a time A(bit 0) and B (bit1).

DATA_IN_VALID: input.
1 CLK-wide pulse indicating that DATAIN is valid.

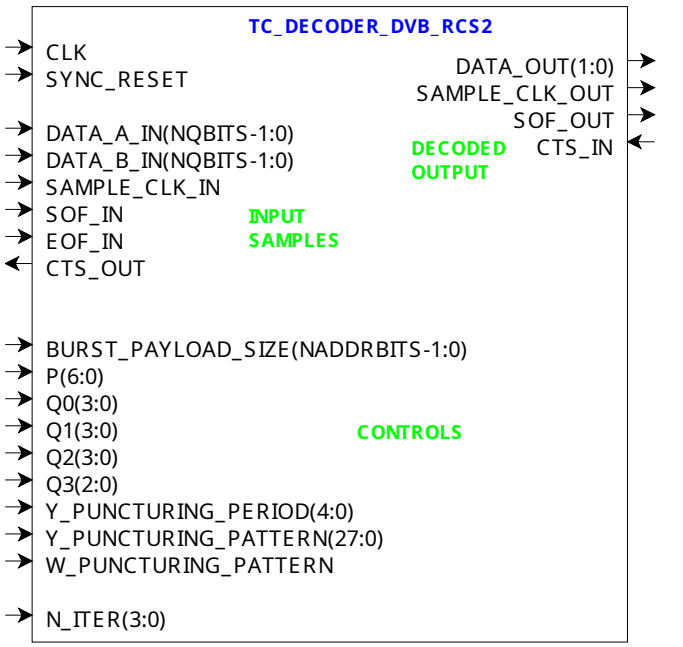
SOF_IN: input Start Of Frame. 1 CLK-wide pulse. The SOF is aligned with **DATA_IN_VALID**. Note that there is no need for an end of frame as the input frame size is defined as a control parameter.

CTS_OUT: output.
Clear-To-Send flow control. '1' indicates that the encoder is ready to accept another input dibit. IMPORTANT: relying on CTS_OUT for flow control may not be sufficient because of latency in stopping the flow. NEVER send the next SOF_IN when CTS_OUT = '0'. This implies the sender must count the data symbol in a frame, stop at N and wait 2 CLKs at least before checking CTS_OUT again.

The encoder outputs mirror its inputs:
DATA_OUT(1:0), **DATA_OUT_VALID**, **SOF_OUT**, **EOF_OUT**, **CTS_IN**.



Decoder



DATA_A_IN / DATA_B_IN: Two soft-quantized input samples. The precision (**NQBITS**) is selectable at the time of synthesis. A 4-bit soft-quantization is considered a good trade-off between decoding performance and FPGA occupancy. A 5-bit soft-quantization may yield minor performance improvement.

Usage: it is expected that the demodulator preceding this decoder will normalize the demodulated samples prior to soft-quantization by using an AGC loop. The AGC target level is important in maximizing the decoder BER performance.

DATA_IN_VALID: input.
1 CLK-wide pulse indicating that DATAIN is valid.

SOF_IN / EOF_IN: inputs Start Of Frame and End Of Frame. 1 CLK-wide pulses.
A aligned with **DATA_IN_VALID**.

CTS_OUT: output.
Clear-To-Send flow control. '1' indicates that the encoder is ready to accept another input dual input samples.

The decoder outputs mirror its inputs:
DATA_OUT(1:0), **DATA_OUT_VALID**, **SOF_OUT**, **CTS_IN**.

N_ITER(3:0): input. Number of decoder iterations. MUST be an odd number between 1 and 15. The more iterations, the lower the BER. However, the decoder latency is nearly proportional to the number of iterations. 7 is a good tradeoff between performance and latency.

Performance

Encoder throughput

The maximum encoder throughput is as follows:

- Encoded output: $2*f_{clk}$ bits/s
- Uncoded input: $2*f_{clk}*R$ bits/s,
  where R is the encoding rate and f_{clk} the FPGA clock.

Decoder latency

The decoder can only handle one frame at a time. The latency between input SOF and decoded output EOF is a function of **BURST_PAYLOAD_SIZE**, the coding rate **R1/R2** and the selected number of decoding iterations **N_ITER**:

Latency (in processing clocks CLK) = (**BURST_PAYLOAD_SIZE** * 4 + 25) * (2 * **N_ITER** + 1/(**R1/R2)**)

For example, in the case of a 1000 Bytes payload, rate 3/4 and 7 iterations, the latency is 61717 clocks (including 5333 clocks for encoded input samples, 4000 clocks for output decoded bits).

Frame Error Rate

The decoded errors are somewhat bursty in nature, with many error-free decoded frames followed by an occasional erroneous frame with many bit errors. Therefore, we prefer to measure the decoder performance in terms of frame error rate (FER).

Frame error rate examples:

- 2032-bit frame, **Rate 1/3**, 5-bit soft quantization, 15-iterations:
  FER = 10^{-2} @ E_b/N_o = 1.4 dB
  FER = 10^{-3} @ E_b/N_o = 1.6 dB
- 768-bit frame, **Rate 3/4**, 5-bit soft quantization, 15-iterations:
  FER = 10^{-2} @ E_b/N_o = 3.1 dB
  FER = 10^{-3} @ E_b/N_o = 3.5 dB
- 472-bit frame, **Rate 1/2**, 5-bit soft quantization, 15-iterations:
  FER = 10^{-2} @ E_b/N_o = 1.9 dB
  FER = 10^{-3} @ E_b/N_o = 2.2 dB

Software Licensing

The COM-7003SOFT is supplied under the following key licensing terms:

1. A nonexclusive, nontransferable license to use the VHDL source code internally, and
2. An unlimited, royalty-free, nonexclusive transferable license to make and use products incorporating the licensed materials, solely in bit stream format, on a worldwide basis.

The complete VHDL/IP Software License Agreement can be downloaded from http://www.comblock.com/download/softwarelicense.pdf

Configuration Management

The current software revision is 3.

Directory	Contents
/doc	Specifications, user manual, implementation documents
/src	.vhd source code,.pkg packages, .xdc constraint files (Xilinx) One component per file.
/sim	VHDL test benches
/matlab	Matlab .m file for simulating the encoding and decoding algorithms, for generating stimulus files for VHDL simulation and for end-to-end BER performance analysis at various signal to noise ratios
/bin	.bit configuration files (for use with ComBlock COM-1800 FPGA development platform)

Project files:

Xilinx ISE 14 project file: com-7003.xise
Xilinx Vivado v2015.2 project file: project_1.xpr

VHDL development environment

The VHDL software was developed using the following development environment:

(a) Xilinx ISE 14.7 for synthesis, place and route

(b) Xilinx Vivado 2015.2 for synthesis, place and route and VHDL simulation

The entire project fits easily within a Xilinx Artix7-100T. Therefore, the ISE project can be processed using the free Xilinx WebPack tools.

Device Utilization Summary

The encoder size is fixed (not parameterized).

Device: Xilinx Artix7-100T

Encoder		% of Xilinx Artix7-100T
Registers	721	0.6%
LUTs	996	1.6%
Block RAM/FIFO	3.5	2.6%
DSP48	1	0.4%
GCLKs	1	3.1%

The decoder size depends essentially on two key parameters defined in the generic section of *tc_decoder_dvb_rcs2.vhd*, namely:

- The maximum payload size defined by the constant **NADDRBITS**
- The number of soft-quantized bits at the decoder input **NQBITS**

Decoder **4-bit soft-quantization** **Frame size < 2048 bits**		% of Xilinx Artix7-100T
Registers	3558	2.8%
LUTs	10652	16.8%
Block RAM/FIFO	15	11.1%
DSP48	1	0.4%
GCLKs	1	3.1%

Decoder **4-bit soft-quantization** **Frame size ≤ 8000 bits**		% of Artix7-100T
Registers	3591	2.8%
LUTs	10726	16.9%
Block RAM/FIFO	39.5	29.3%
DSP48	1	0.4%
GCLKs	1	3.1%

Clock and decoding speed

The entire design uses a single global clock CLK. Typical maximum clock frequencies for various FPGA families are listed below:

Device family	**Encoder**	**Decoder**
Xilinx Artix 7 -2 speed grade	212 MHz	155 MHz
Xilinx Kintex-7 -2 speed grade	294 MHz	230 MHz

Ready-to-use Hardware

The COM-7003SOFT was developed on, and therefore ready to use on the following commercial off-the-shelf hardware platform:

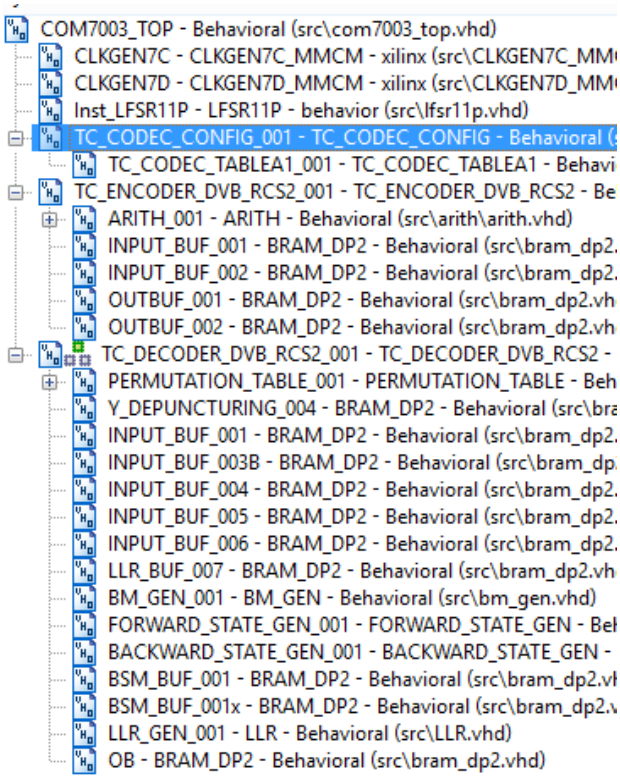
FPGA development platform
COM-1800 FPGA (XC7A100T) + ARM + DDR3 SODIMM socket + GbE LAN development platform

Xilinx-specific code

The VHDL source code is written in generic VHDL and thus can be ported FPGAs from various vendors. No Xilinx CORE nor Xilinx primitive is used.

VHDL components overview

Top level



TC_CODEC_CONFIG.vhd generates detailed configuration parameters for the encoder and decoder. The user enters the burst payload size (in BYTES) and the coding rate R1/R2. This component looks up the optimum detailed configuration in Table-A1 of [1]

TC_ENCODER_DVB_RCS2.vhd is the encoder top component.

The *ARITH.vhd* component performs minor arithmetic operations to compute the initial permutation indices 3, (4Q1+3) modulo N, (4Q2+3 + 4Q0P) modulo N, (4Q3+3 + 4Q0P) modulo N.

BRAM_DP2.vhd is a generic dual-port memory, used as input and output elastic buffers. Memory is inferred (no Xilinx primitive is used).

TC_DECODER_DVB_RCS2.vhd is the decoder top component. It processes one frame at a time, i.e. the input flow must be stopped until the entire frame is decoded.

PERMUTATION_TABLE.vhd generate permutation and inverse permutation lookup tables

BM.vhd generates the 16 branch metrics value, based on the received samples ABYW and the associated erasure information (when puncturing is enabled).

FORWARD_STATE_GEN.vhd generates forward state metrics a(k+1,s) from the previous state metrics a(k,s')

BACKWARD_STATE_GEN.vhd generates backward state metrics b(k,s) from the next state metrics b(k+1,s)

LLR.vhd generates the log likelihood ratio (LLR) from a(k), bm(s,s'), b(k+1). see Matlab turbo.m

COM7003_TOP.vhd: is mostly a use example when the turbo-codec is implemented on a ComBlock COM-1800 FPGA development platform. This component includes encoder, decoder, detailed codec configuration, clock generation, interface to a supervisory microcontroller (8-bit address/data bus to exchange control registers REG and status registers SREG). CLK_P is the main processing clock.

INFILE2SIM.vhd reads an input file. This component is used by the testbench to read a soft-quantized encoded bit stream generated by the `turbo.m` Matlab program for various Eb/No cases.

SIM2OUTFILE.vhd writes three 12-bit data variables to a tab delimited file which can be subsequently read by Matlab (load command) for plotting or analysis.

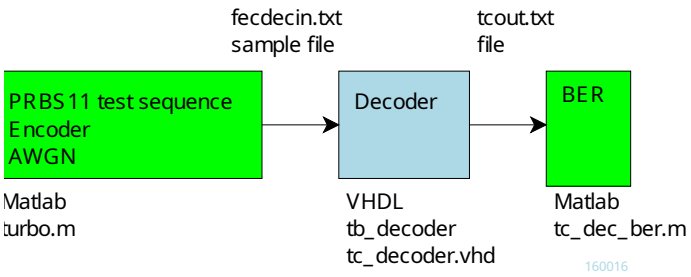
Matlab simulation

The `turbo.m` program

- generates a stimulus file `fecdecin.txt` for use as input to the decoder VHDL simulation. The file includes a frame of pseudo-random (PRBS11) data bits, turbo code encoding, additive white Gaussian noise and soft-quantization.
- Performs end-to-end BER performance analysis of the turbo-codec over a noisy (AWGN) channel.

The `turbo.m` program uses `treillis_diagram.m` to generate the treillis state diagram (input state, input data, output state, output parity bits).

The `tc_dec_ber.m` program reads a file of decoded data `tcout.txt` generated by VHDL simulation and compare it with the original PRBS-11 test sequence. It counts the number of bit errors.



Reference documents

[1] ETSI EN 301 545-2

“Digital Video Broadcasting (DVB); Second Generation DVB Interactive Satellite System (DVB-RCS2); Part 2: Lower Layers for Satellite standard” 7.3.5.1 Turbo FEC Encoder

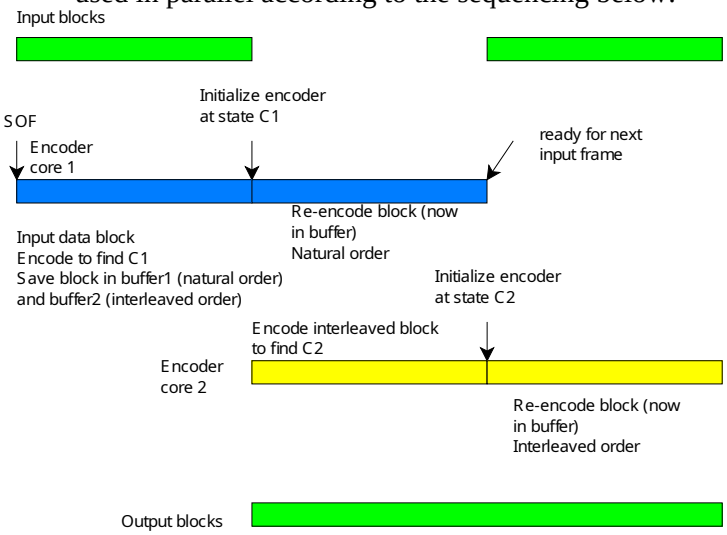
Implementation Overview

Turbo Code Encoder

Encoding requires four passes of the input block through an encoder core:

- pass #1: natural order. Determines the circulation state C1
- pass #2: natural order starting at encoder state C1
- pass #3: interleaved order. Determines the circulation state C2.
- Pass #4: interleaved order starting at encoder state C2.

For maximum throughput, two encoder cores are used in parallel according to the sequencing below:



ComBlock Ordering Information

COM-7003SOFT Turbo code encoder/decoder, VHDL source code / IP core

ECCN: EAR99

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