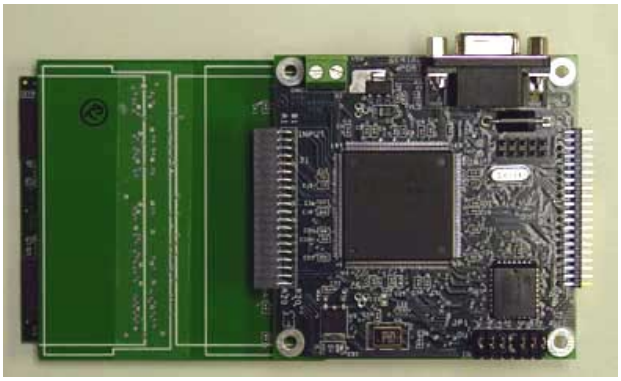
COM-8001
ARBITRARY WAVEFORM GENERATOR
256MB (-A) 1GB (-B) 40 Msamples/s

Key Features

- Stores 256 MB (-A option) or 1GB (-B option) of binary data in DRAM.
- High-speed upload over TCP-IP network or USB 2.0 using the COM-5003 TCP-IP / USB Gateway module.
- High-speed download examples:
  - 40 Msamples/s complex 10-bit D/A waveform generation @ baseband with COM-2001.
  - 20 Msamples/s complex 14-bit D/A waveform generation @ 70 MHz IF with COM-4004.
  - Digital device test
- Downloaded data is pushed to or pulled by output module. The download speed is selectable from 0 to 40 Msamples/s by steps of 5 Hz.
- Single run or continuous download.
- User control over memory segmentation (start address, upload/download window size).
- Sample Matlab programs to generate representative waveforms.
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.
- Connectorized 3”x 3” module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right). Single 5V supply with reverse voltage and overvoltage protection. Interfaces with 3.3V LVTTL logic.

COM-8001-A 256MB (bottom view)



COM-8001-B 1GB (top view)

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com8001.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .

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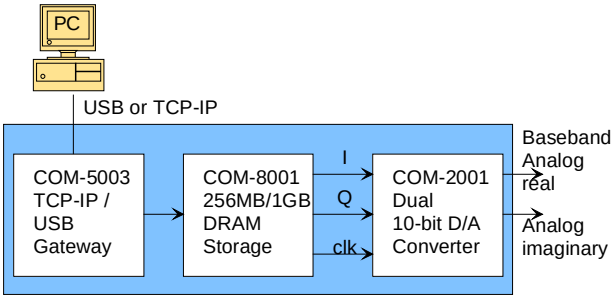
Typical Applications

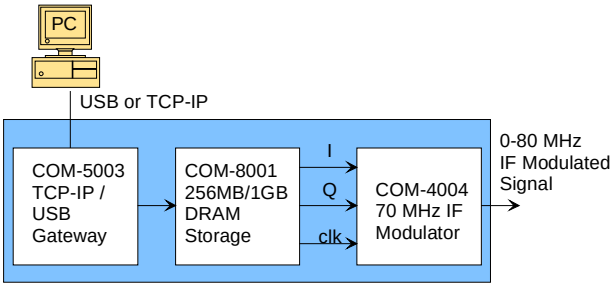
Baseband Analog Signal Generation

A complex frequency waveform is described by means of 2x10-bit wide samples. The samples are played back at a speed up to 40 Msamples/s and converted to two complex analog signals at zero center frequency.



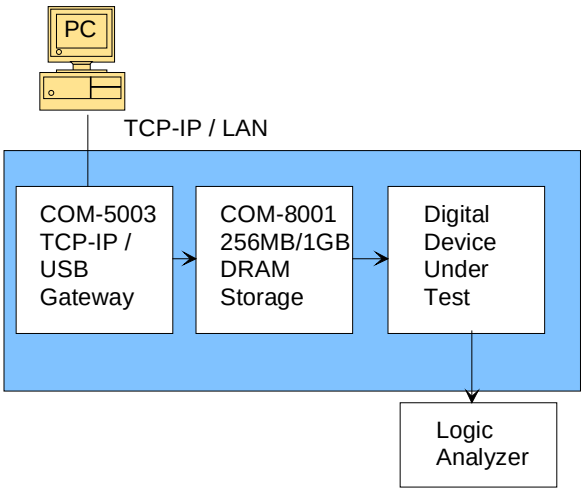
70 MHz IF Analog Signal Generation

A complex frequency waveform is described by means of 2x14-bit wide samples. The samples are played back at a speed up to 20 Msamples/s (complex samples) and converted (modulated) to an intermediate frequency analog signal. The modulated signal center frequency is programmable in the range 0 to 80 MHz.



Digital Signal Generation

Purely digital signals can also be stored and played back, to test digital modules for example. The digital data is organized into 1-bit, 2-bit, 8-bit, 16-bit or 20-bit wide words.



Electrical Interface

Inputs

Input Module Interface	Definition
DATA_IN[7:0]	8-bit data sample.
SAMPLE_CLK_IN	Read input sample at rising edge of CLK when SAMPLE_CLK_IN = '1'
CLK_IN	Input reference clock for synchronous I/O. DATA_IN, SAMPLE_CLK_IN and SYMBOL_CLK_IN are aread at the rising edge of CLK_IN. Maximum 40 MHz.
EXT_TRIGGER_IN	External trigger pulse. When the external trigger mechanism is enabled by software, download actions will be placed on hold until the falling edge of this signal. Works for single or continuous downloads. Input is ignored when disabled by software. This signal is internally pulled low. Its use is optional.

Outputs

There are two possible output configurations, depending on the application:

(a) 70 MHz IF waveform generation (COM-4004 module interface)

Output Module Interface	Definition
DATA_OUT[13:0]	Output. Quadrature baseband samples, up to 14-bit precision, 2's complement format. Bit 13 is the most significant bit. When a lesser precision is selected, the unused least significant bits are set to zero. The in-phase (I) and quadrature (Q) samples alternate. The samples are generated at the falling edge of SAMPLE_CLK_REQ_IN.
SAMPLE_CLK_REQ_IN	Input. Input samples are clocked at the rising edge of SAMPLE_CLK_REQ. I & Q samples alternate at each request. SAMPLE_CLK_REQ is a 100 MHz clock.
TX_ENABLE_OUT	Output. Transmit enable. Active high. The first sample after TX_ENABLE becomes active is an in-phase (I) sample. This signal is generated at the falling edge of SAMPLE_CLK_REQ_IN.
TRIGGER_OUT	Pulse indicating that the complex sample is the first in the selected download window. Synchronous with SAMPLE_CLK_REQ_IN.

(b) Digital signal playback

Output Module Interface	Definition
DATA_OUT[19:0]	Output. This digital sample width is programmable among 1,2,8,14[1],16 and 20-bit wide..
SAMPLE_CLK_REQ_IN / DAC_CLK_OUT	Signal direction depends on the output flow control configuration: Input when data is pulled out by the next module. Output when data is pushed out using the internal NCO. SAMPLE_CLK_REQ_IN: Sample request. Used when the sink module controls the throughput (i.e the data is pulled by the next module). DAC_CLK_OUT: Output sampling clock. The output samples are stable at the rising edge of DAC_CLK_OUT.
SAMPLE_CLK_OUT	Output. Pulse to indicate that DATA_OUT contains a new sample. Read DATA_OUT at the rising edge of CLK when SAMPLE_CLK_OUT = '1'.
TRIGGER_OUT	Pulse indicating that the complex sample is the first in the selected download window. Aligned with SAMPLE_CLK_OUT.

[1] 14-bit width only in conjunction with COM-4004 70 MHz modulator

Other I/Os

Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the CLK frequency. The maximum power consumption at 40 MHz is 600mA.

Important: I/O signals are 0-3.3V LVTTL. Inputs are NOT 5V tolerant!

Configuration (via Serial Link / LAN)

Complete assemblies can be monitored and controlled centrally over a single serial or LAN connection.

The module configuration parameters are stored in non-volatile memory. All control registers are read/write.

This module operates at an internal clock rate $\mathbf{f_{clk}}$ set by the external reference clock CLK_IN (40 MHz for most applications).

Parameters	Configuration
Download speed f_s	Output sampling frequency. Used when the data is pushed to the next module. (see flow control). Ignored when data is pulled by the next module. The sampling frequency f_s is expressed as f_s/f_{clk} * 2^23. Note: when selecting sampling frequencies close to f_{clk}, samples may be unevenly spaced in time. REG0 = bits 7-0 REG1 = bits 15-8 REG2 = bits 23 - 16
Upload start address	It is possible to upload the entire 256MB/1GB memory or a fraction thereof. The upload section is identified by its start address and length. It is expressed in bytes. The address increment is 32-bytes (i.e. 5 least significant bits are ignored) . REG3 = bit 7-0 REG4 = bit 15-8 REG5 = bit 23-16 REG6 bit 3-0 = bit 27-24
Upload window length	Upload window length., expressed in bytes. The size increment is 32-bytes (i.e. 5 least significant bits are ignored) . Wrapping around is not allowed, i.e. window start address + length must be less than the 256MB/1GB memory upper address. REG7 = bit 7-0 REG8 = bit 15-8 REG9 = bit 23-16 REG10 bit 3-0 = bit 27-24
Download start address	It is possible to download the entire 256MB/1GB memory or a fraction thereof. The download section is identified by its start address and length. It is expressed in bytes. The address increment is 32-bytes (i.e. 5 least significant bits are ignored) . REG11 = bit 7-0 REG12 = bit 15-8 REG13 = bit 23-16 REG14 bit 3-0 = bit 27-24
Download window length	Download window length., expressed in bytes. The size increment is 32-bytes (i.e. 5 least significant bits are ignored). Wrapping around is not allowed, i.e. window start address + length must be less than the 256MB/1GB memory upper address. REG15 = bit 7-0 REG16 = bit 15-8 REG17 = bit 23-16 REG18 bits 3-0 = bit 27-24
Upload / Download mode	000 = no change 001 = start upload 011 = start download (single run) 100 = start download (continuous run) 101 = stop current operation. Note: a mode change MUST be followed by writing to REG21 to become effective. REG19 bits 3-1
Output flow control	0 = data is pushed. The data throughput is controlled by the internal NCO, the frequency of which is programmable. 1 = data is pulled by the next module using the SAMPLE_CLK_REQ_IN signal. In both cases, output samples are to be read at the rising edge of CLK when SAMPLE_CLK_OUT = '1'. REG19 bit 4
Output format	00001 = 1-bit wide 00010 = 2-bit wide 00100 = 4-bit wide 01000 = 8-bit wide 01110 = 2*14-bit wide (only for interface with COM-4004) 10000 = 16-bit wide 10100 = 20-bit wide REG20 bits 4-0
Output pinout	000 = most ComBlock modules 001 = special case COM-4004 70 MHz module. (data flow control selection must be 'pushed'). 010 = special case, COM-7001 Turbo code encoder interface (Ouput format must be 1-bit wide only). REG20 bits 7-5
External Trigger Enable	Enable or disable the external trigger. When enabled, data download starts when the COM-8001 is in single or continuous download mode and when a pulse is received on the EXT_TRIGGER_IN input. 0 = disabled 1 = enabled. REG21 bit 0

Baseline configurations can be found at www.comblock.com/tsbasic_settings.htm and imported into the ComBlock assembly using the ComBlock Control Center File | Import menu.

Monitoring (via Serial Link / LAN)

Monitoring registers are read-only.

Parameters	Monitoring
Write pointer address	Current DRAM write pointer address. Used to monitor the upload progress. When finished, the write pointer will point to the last address written to plus one. The integrity of this 4-byte information is preserved when registers are read in sequence REG22/23/24/25 (data is frozen upon reading the first byte in REG22 and released upon reading the last byte in REG25). REG22 = bits 7-0 REG23 = bits 15-8 REG24 = bits 23 - 16 REG25 = bits 27 - 24
Read pointer address	Current DRAM read pointer address. Used to monitor the download progress. When finished, the read pointer will point to the last address read plus one. Expressed in bytes. The integrity of this 4-byte information is preserved when registers are read in sequence REG26/27/28/29 (data is frozen upon reading the first byte in REG26 and released upon reading the last byte in REG29). REG26 = bits 7-0 REG27 = bits 15-8 REG28 = bits 23 – 16 REG29 bits 3-0 = bits 27 - 24
Upload checksum	16-bit checksum obtained by unsigned sum of all bytes uploaded to the SDRAM. Wait until the upload completion to read this checksum. REG31 = bits 7-0 REG32 = bits 15-8
Download checksum	16-bit checksum obtained by unsigned sum of all bytes downloaded from the SDRAM. Wait until the single download completion to read this checksum. The download checksum should match the upload checksum if the sizes and start addresses match for the upload and the single download. Does not work with continuous download. REG33 = bits 7-0 REG34 = bits 15-8
Option o / Version v	Returns ‘8001ov’ when prompted for option o and version v numbers.

ComScope Monitoring

Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. The COM-8001 signal traces and trigger are defined as follows:

Trace 1 signals	Format	Nominal sampling rate	Buffer length (samples)
1: I-channel baseband output to COM-2001	8-bit unsigned (8MSB /10)	SAMPLE_CLK_OUT	512
2: DATA_OUT(7:0) 8-bit wide output samples. User defined format.	8-bit	SAMPLE_CLK_OUT	512
3: DATA_IN(7:0) Input samples from TCP-IP/LAN or other sources.	8-bit	SAMPLE_CLK_IN	512
4: DATA_OUT(0) Serial output stream.	binary	SAMPLE_CLK_OUT	4096
Trace 2 signals	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: Q-channel baseband output to COM-2001	8-bit unsigned (8MSB /10)	SAMPLE_CLK_OUT	512
Trigger Signal	**Format**		
1: EXT_TRIGGER_IN	binary		

Signals sampling rates can be changed under software control by adjusting the decimation factor and/or selecting the $\mathbf{f_{clk}}$ processing clock as real-time sampling clock.

In particular, selecting the $\mathbf{f_{clk}}$ processing clock as real-time sampling clock allows one to have the same time-scale for all signals.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.

Operation

Upload

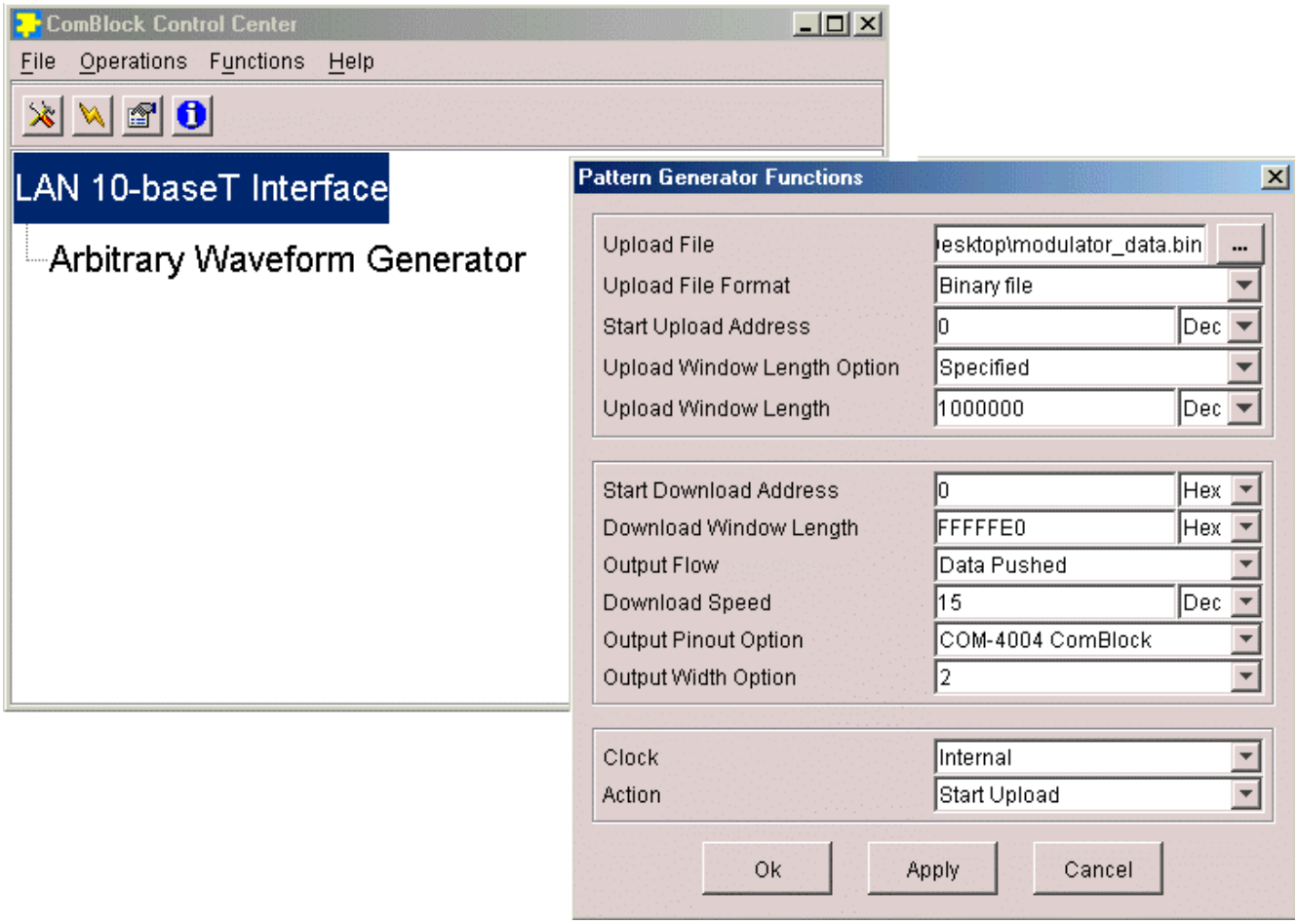
Step 1: Create a file containing the data samples. Two file types are currently supported:

- binary file: data samples are stored sequentially, most significant bit of the most significant byte first. Data samples are not necessarily aligned with byte boundaries.
- text file: each byte is represented by a number in the range 0 to 255. Each byte is delimited by a line feed, carriage return or a combination of carriage return / line feed.

Step 2: Using the ComBlock Control Center (Graphical User Interface), open the Pattern Generator Functions window (under the Functions menu). This menu is automatically enabled when the ComBlock Control Center detects the combination COM-5003 / COM-8001. The upper section of the window defines the upload parameters:

- Filename
- File type: binary or text
- Start upload address: where the first byte will be stored. Must be a multiple of 32.
- Window length: can be explicitely stated in bytes or implicitely specified by the file size.

Step 3: To start the upload, select the "Start Upload" action and press the Apply button. A progress bar shows the percentage of completion.



Download

Step 1: Using the ComBlock Control Center, configure the download parameters:

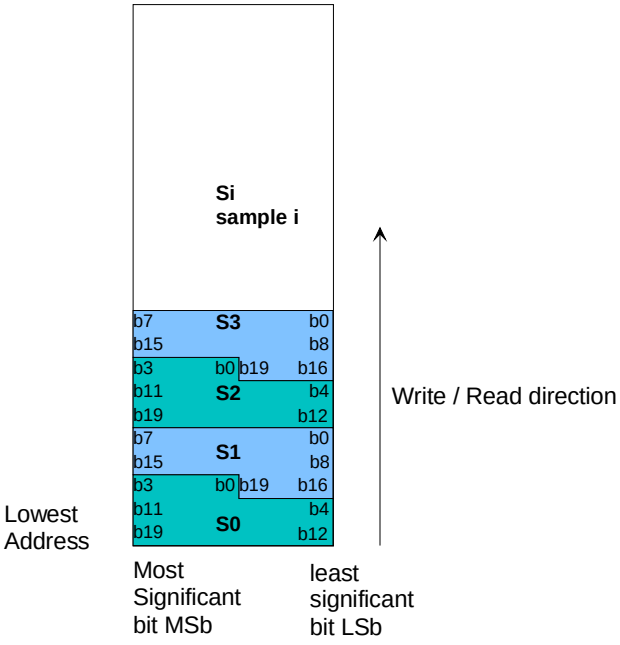
- The data to be downloaded can be segmented into distinct windows. A window can be the entire SDRAM memory or a fraction thereof. The download window is defined by its start address and a window length.
- Flow control: the download clock can be controlled by an internal numerical oscillator (data is "pushed out"), or by an external clock SAMPLE_CLK_REQ_IN which typically originates from the module to which data is sent (data is "pulled out").
- The width of the output samples is selectable among 1,2,8,14,16,20 bit.
- A variety of output interfaces are also supported, as defined in the Pinout section below.

Step 2: Using the ComBlock Control Center, start the download mode by selecting single run or continuous run. Press the Apply button.

Whenever the download starts or rewinds, a pulse will be generated on the TRIGGER_OUT output pin.

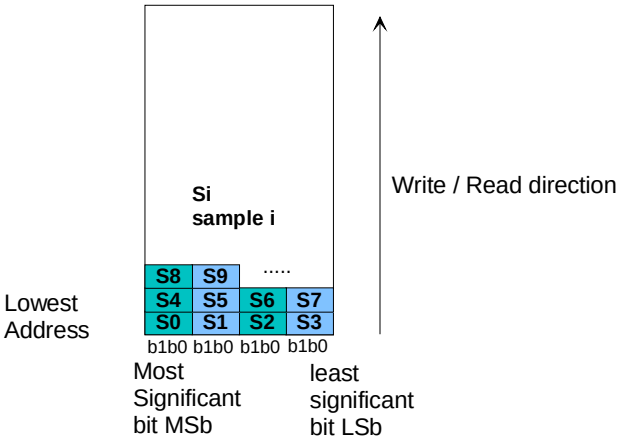
Output sample width & file format

The issue of packing n-bit wide samples in a byte-oriented file format must be given some consideration. The diagram below illustrates how 20-bit wide samples are stored in a file: S_i indicate the sample order, whereas b_i indicates the bit order within a sample.

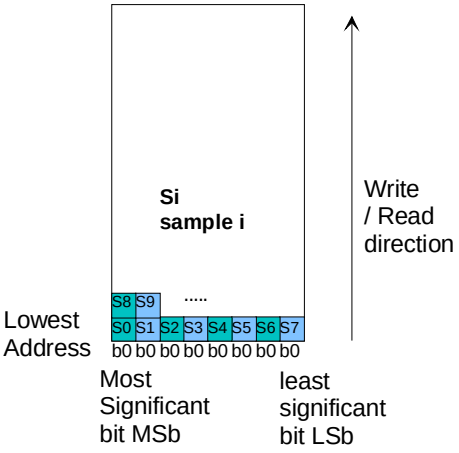


20-bit wide samples file format

Please be aware of possible bit reversal at the interface between the COM-8001 output and the follow-on module. For instance, the COM-2001 dual D/A converter module uses pins DATA_OUT(0) and DATA_OUT(10) as most significant bits for the I and Q samples respectively.



2-bit wide samples file format



1-bit wide samples file format

Waveform generation programs

Several examples of Matlab and C programs can be used to generate sample files to be uploaded into the COM-8001 module.

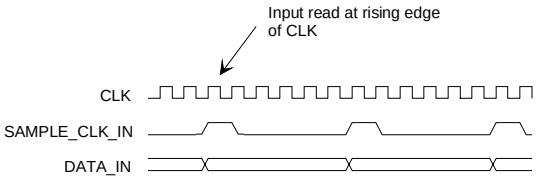
Program	Waveform
Com8001r1	Sinewave
Com8001r2	Two sinewaves
Com8001r3	Low data rate satellite signal consisting of a sinewave (beacon) + QPSK modulated signal (square root raised cosine filter).
com8001_large_sin_cos_20b_out	C program to create large sin/cos waveform, 2*10-bit wide samples..
Com8001_2bout	C program to create large file of 2-bit wide samples
com8001_PRBS11_out	C program to create large PRBS-11 files, with 1/2/8-bit wide output samples.

Source code for these sample programs can be downloaded from
http://www.comblock.com/download.htm - Utilities

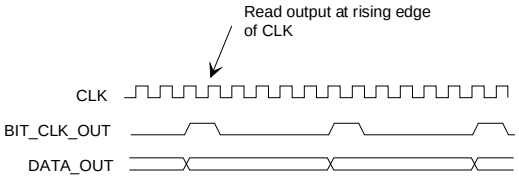
Timing

The I/O signals are synchronous with the rising edge of the reference clock CLK[2] (i.e. all signals are stable at the time of the rising edge of the reference clock CLK). The maximum CLK frequency is 40 MHz.

Input

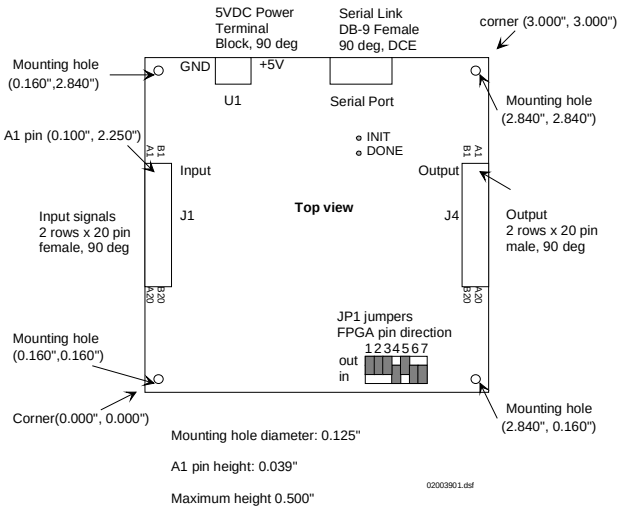


Output



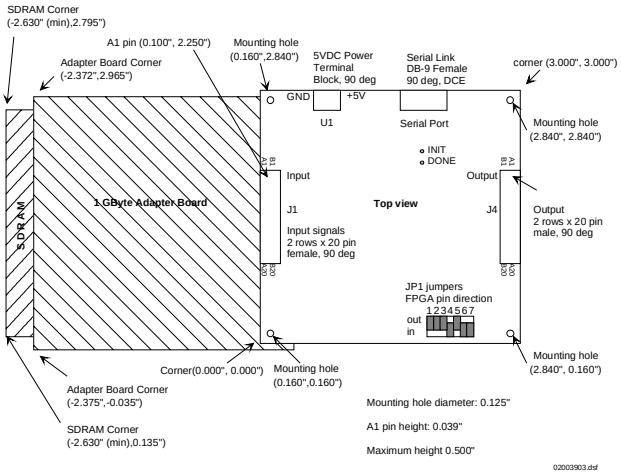
Mechanical Interface

(-A Option, 256 MB memory)



[2] The output timing for the interface with the COM-4004 module is synchronous with an external clock. For details, please refer to the COM-4004 specifications.

(-B Option, 1GB memory)



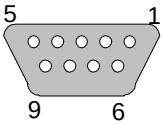
In order to increase the SDRAM memory to 1 GB an adapter board is used. The adapter board extends the 3”x3” ComBlock to the left. The adapter board is at a lower level and is designed to fit under another ComBlock (for example under a COM-5003 LAN interface module).

Note: All seven JP1 jumpers must be in the ‘OUT’ location.

Pinout

Serial Link P1

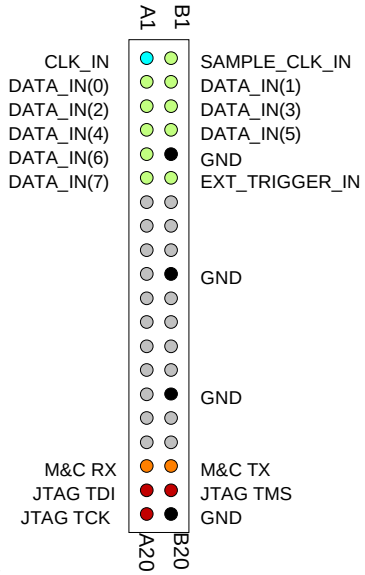
The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.



DB-9 Female

2 Transmit
3 Receive
5 Ground

Input Connector J1



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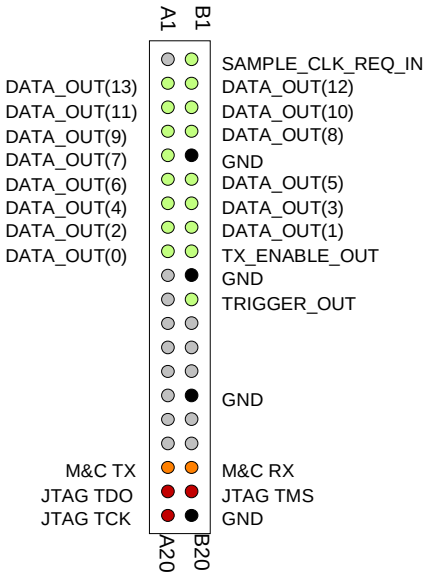
This input format is designed for direct connection to the following ComBlock module:

COM-5003 TCP-IP / USB Gateway
COM-5101 RS422 Interface

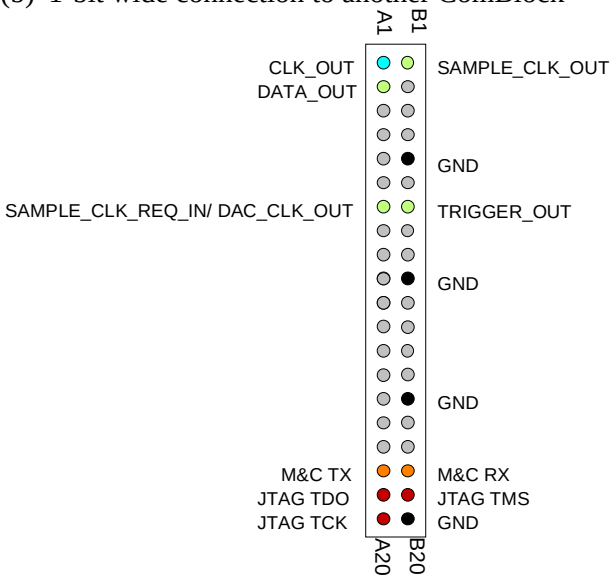
Output Connector J4

There are several possible output configurations, depending on the application:

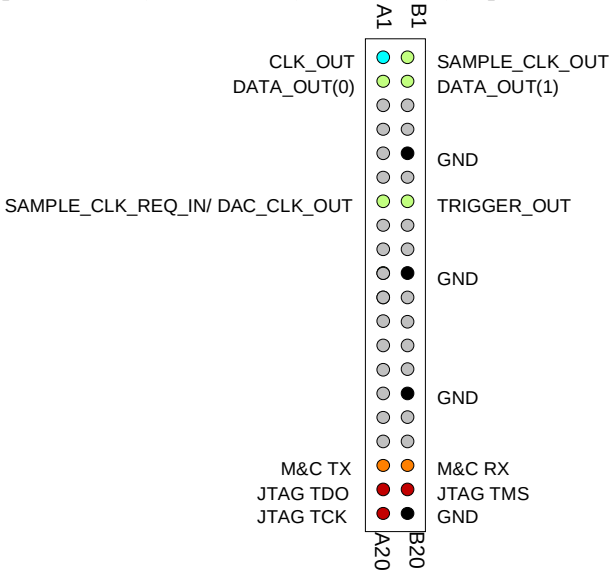
(a) connection to a COM-4004 70 MHz IF Modulator.



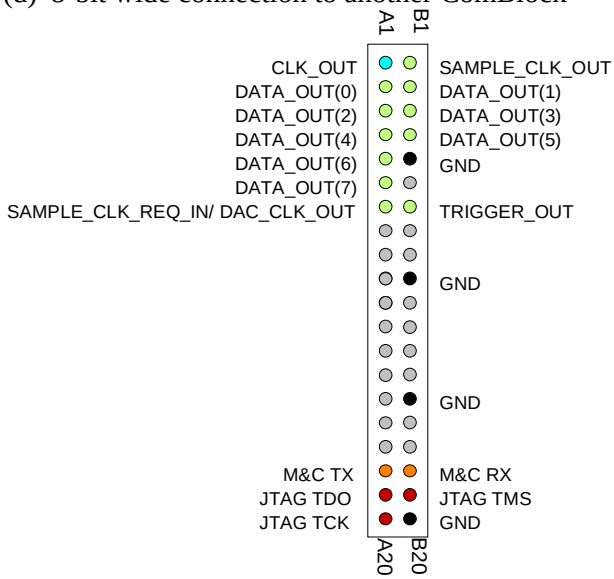
(b) 1-bit wide connection to another ComBlock



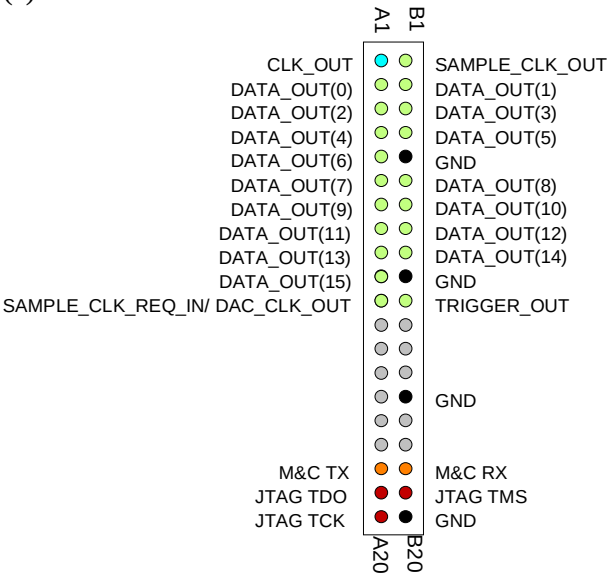
(c) 2-bit wide connection to another ComBlock [COM-1002, COM-1012, COM-1005,etc]



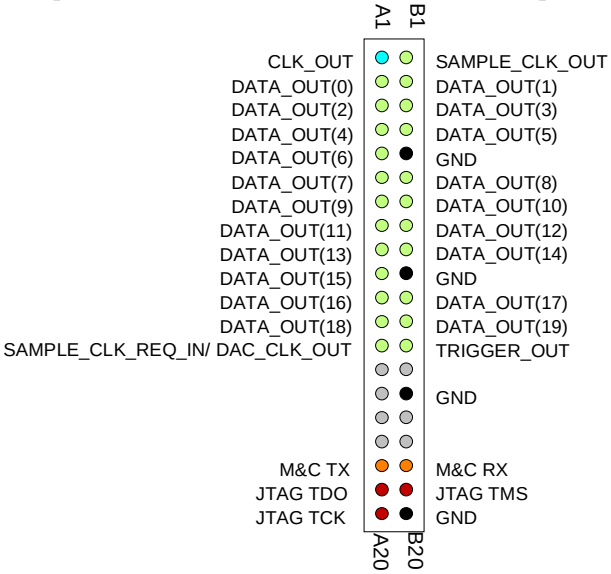
(d) 8-bit wide connection to another ComBlock



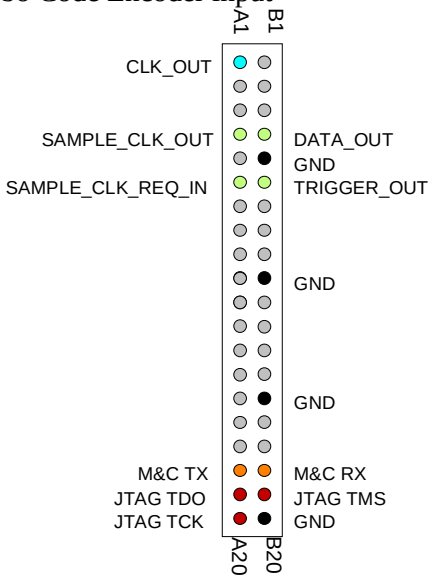
(e) 16-bit wide connection to another ComBlock



(f) 20-bit wide connection to another ComBlock [COM-1001, COM-1011, COM-2001,etc]



(g) Special case: connection to the COM-7001 Turbo Code Encoder input



I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-5003 TCP-IP / USB Gateway	COM-4004 70 MHz IF Modulator
COM-5101 Signal/Power conditioning & RS422 interface	COM-2001 Digital-to-Analog Conversion, Baseband
	COM-7001 Turbo-Code Encoder
	COM-1002 BPSK/QPSK/OQPSK digital Modulator
	COM-1012/1019 DSSS digital Modulator
	COM-1028 FSK/MSK/GFSK/GMSK digital Modulator
	COM-1001 BPSK/QPSK/OQPSK digital Demodulator
	COM-1011/1018 DSSS digital Demodulator
	COM-1027 FSK/MSK digital Demodulator

Troubleshooting

Symptom: The "Pattern Generation Functions" window behaves erratically.

This behavior may be due to erroneous control register values. Manually enter the following sequence in control registers REG0 through 21 using the settings window (third button from the left in the ComBlock Control Center):
D7 A3 00 00 00 00 00 E0 FF FF 0F 00 00 00 00 00 0A 00 00 03 14 00.

Configuration Management

This specification is to be used in conjunction with VHDL software revision 11 and ComBlock Control Center revision 2.31 and above.

ComBlock Ordering Information

COM-8001-A ARBITRARY WAVEFORM GENERATION 256MB, 40 Msamples/s.

COM-8001-B ARBITRARY WAVEFORM GENERATION 1GB, 40 Msamples/s.

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