COM-8002
HIGH-SPEED DATA ACQUISITION
256MB / 40 Msamples/s

Key Features

- Maximum sampling rate 40 MHz.
- Sample precision from 1 to 20-bit wide.
- 256 Mbytes storage.
- Download over TCP-IP network using the COM-5003 Network interface module.
- Seamless connection to ComBlock digital and RF receivers.
- Typical applications:
  - Logic analyzer
  - RF signal capture
  - Data logging
- External/Internal trigger selection
- User control over memory segmentation (start address, upload/download window size).
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.
- Connectorized 3”x 3” module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right). Single 5V supply with reverse voltage and overvoltage protection. Interfaces with 3.3V LVTTL logic.

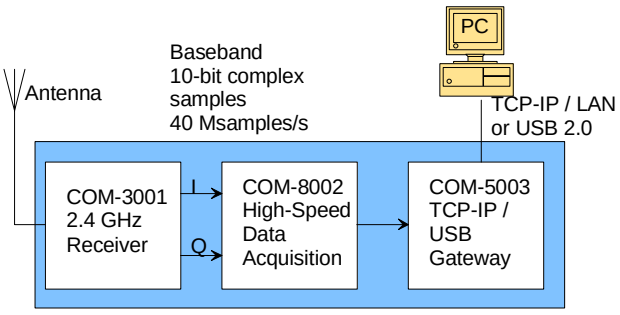
For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com8002.pdf.
These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .

Typical Applications

RF Signal Capture

In this example, a 2.4 GHz Radio-Frequency signal is first translated to near zero center frequency. After undergoing anti-aliasing filtering, the complex baseband samples are quantized at 40 Msamples/s with 10-bit precision. The resulting 800 Mbit/s stream is stored in real-time. The storage capacity is 100 million complex samples.



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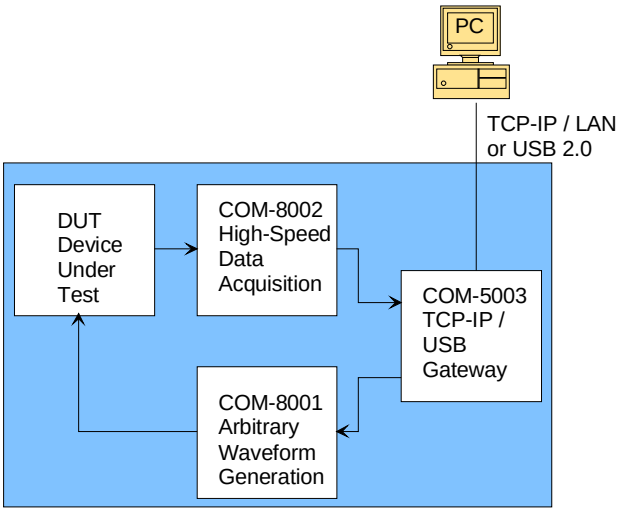
The samples can be read remotely over a TCP-IP link for further batch processing.

Logic Analyzer

The COM-8002 is perfectly suited as a high-speed, high-capacity logic analyzer. In the example illustrated below, the device under test receives its input signals from the COM-8001 arbitrary waveform generation module, while the output signals are collected by the COM-8002 module. Input stimulus and output samples are transferred from/to a remote computer over the network.



Electrical Interface

Inputs

Input Module Interface	Definition
DATA_IN[19:0]	Input data sample. The width is programmable among 1,2,8,16 and 20-bit wide. For width smaller than 20, the lower ranking bits (0,1,2…etc) are used.
SAMPLE_CLK_IN	Read input sample at rising edge of CLK when SAMPLE_CLK_IN = '1'
EXT_TRIGGER_IN	External trigger pulse. Indicates that the current input sample is the first in the selected upload window. The pulse is one CLK wide and is aligned with SAMPLE_CLK_IN.
AGC_OUT	Output. When the COM-8002 is connected directly to an analog / RF receiver, it generates a pulse-width modulated signal to control the analog gain prior to A/D conversion. The purpose is to use the maximum dynamic range while preventing saturation at the A/D converter.
CLK_IN	Input reference clock for synchronous I/O and internal processing clock $\mathbf{f_{clk}}$. DATA_IN and SAMPLE_CLK_IN are read at the rising edge of CLK_IN. Typically 40 MHz.

Outputs

Output Module Interface	Definition
DATA_OUT[7:0]	Output sample.
SAMPLE_CLK_OUT	Output. Pulse to indicate that DATA_OUT contains a new sample. Read DATA_OUT at the rising edge of CLK when SAMPLE_CLK_OUT = '1'.
SAMPLE_CLK_REQ_IN	Sample request input. Used for flow control.

Other I/Os

Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control. Used for ComBlock remote monitoring and control (no data stream).
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the CLK frequency.

	The maximum power consumption at 40 MHz is 600mA.

Important: I/O signals are 0-3.3V LVTTL. Inputs are NOT 5V tolerant!

Configuration (via Serial Link / LAN)

Complete assemblies can be monitored and controlled centrally over a single serial or LAN connection.

The module configuration parameters are stored in non-volatile memory. All control registers are read/write.

Parameters	Configuration
Upload start address	It is possible to upload the entire 256MB memory or a fraction thereof. The upload section is identified by its start address and length. It is expressed in bytes. The address increment is 32-bytes (i.e. 5 least significant bits are ignored). REG0 = bits 7-0 (LSB) REG1 = bits 15-8 REG2 = bits 23-16 REG3 bits 3-0 = bits 27-24
Upload window length	Upload window length, expressed in bytes. The size increment is 32-bytes (i.e. 5 least significant bits are ignored). REG4 = bits 7-0 REG5 = bits 15-8 REG6 = bits 23-16 REG7 bits 3-0 = bits 27-24
Download start address	It is possible to download the entire 256MB memory or a fraction thereof. The download section is identified by its start address and length. It is expressed in bytes. The address increment is 32-bytes (i.e. 5 least significant bits are ignored). REG8 = bits 7-0 REG9 = bits 15-8 REG10 = bits 23-16 REG11 bits 3-0 = bits 27-24
Download window length	Download window length, expressed in bytes. The size increment is 32-bytes (i.e. 5 least significant bits are ignored). REG12 = bits 7-0 REG13 = bits 15-8 REG14 = bits 23-16 REG15 bits 3-0 = bits 27-24
Upload / Download mode	000 = no change. 001 = start upload. 010 = stop upload. 011 = start download. 100 = stop download. Upon switching from download mode to upload mode, data collection starts until the upload window length is full. Note: a mode change MUST be followed by writing to REG18 to become effective. REG16 bits 3-1
External Trigger Enable	Enable or disable the external trigger. When enabled, data acquisition starts when the COM-8002 is in upload mode and when a pulse is received on the EXT_TRIGGER_IN input. 0 = disabled 1 = enabled. REG16 bit 4
AGC enabled	Enable or disable the automatic gain control for an external RF receiver. 0 = fixed at a preset level (see REG18) 1 = enabled (only if 20-bit wide input) REG16 bit 5
Input format	00001 = 1-bit wide 00010 = 2-bit wide 01000 = 8-bit wide 10000 = 16-bit wide 10100 = 20-bit wide REG17 bits 4-0
AGC gain	Gain settings for an external RF receiver. This setting is used when the AGC is disabled (for example during receiver level measurements). Unsigned 8-bit number. When used in conjunction with the COM-300x receivers, 255 represents the minimum gain, 0 the maximum gain. REG18 bits 7-0.
Input Decimation factor D	The input can be subsampled by saving only one in every D input samples, while the other samples are discarded. Valid range 0 – (2^{24}-1). Input decimation is disabled when when D = 0 or 1. REG19 = bits 7-0 (LSB) REG20 = bits 15-8 REG21 = bits 23-16 (MSB)

Baseline configurations can be found at www.comblock.com/tsbasic_settings.htm and imported into the ComBlock assembly using the ComBlock Control Center File | Import menu.

Monitoring (via Serial Link / LAN)

Monitoring registers are read-only.

Parameters	Monitoring
Write pointer address	Current DRAM write pointer address. Used to monitor the upload progress. When finished, the write pointer will point to the last address written to. The integrity of this 4-byte information is preserved when status registers are read in sequence SREG19/20/21/22 (data is frozen upon reading the first byte in SREG19 and released upon reading the last byte in SREG22). SREG19 = bits 7-0 SREG20 = bits 15-8 SREG21 = bits 23 – 16 SREG22 bits 3-0 = bits 27 – 24
Read pointer address	Current DRAM read pointer address. Used to monitor the download progress. When finished, the read pointer will point to the last address read. Expressed in bytes. The integrity of this 4-byte information is preserved when status registers are read in sequence SREG23/24/25/26 (data is frozen upon reading the first byte in SREG23 and released upon reading the last byte in REG26). SREG23 = bits 7-0 SREG24 = bits 15-8 SREG25 = bits 23 – 16 SREG26 bits 3-0 = bits 27 - 24

ComScope Monitoring

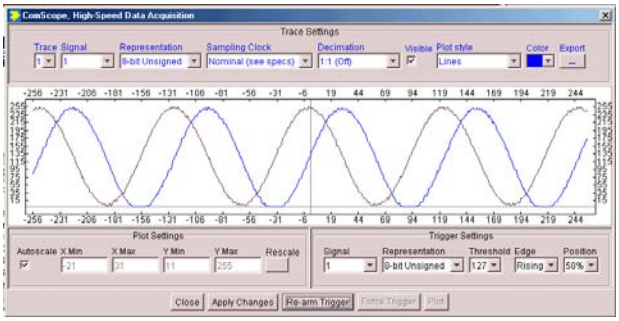
Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. The COM-8002 signal traces and trigger are defined as follows:

Trace 1 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: input from COM-300x receiver: I-channel DATA_IN(0:7)	8-bit unsigned (8MSB /10)	SAMPLE_CLK_IN	512
2: DATA_IN(0)	binary	SAMPLE_CLK_IN	4096
Trace 2 signals	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: input from COM-300x receiver: Q-channel DATA_IN(10:17)	8-bit unsigned. (8MSB /10)	SAMPLE_CLK_IN	512
2: DATA_IN(1)	binary	SAMPLE_CLK_IN	4096
3: input sampling clock SAMPLE_CLK_IN	binary	processing clock $\mathbf{f_{clk}}$	4096
Trigger Signal	**Format**		
1: input from COM-300x receiver: I-channel DATA_IN(0:7)	8-bit unsigned. (8MSB /10)		
2: DATA_IN(0)	binary		

Signals sampling rates can be changed under software control by adjusting the decimation factor and/or selecting the $\mathbf{f_{clk}}$ processing clock as real-time sampling clock.

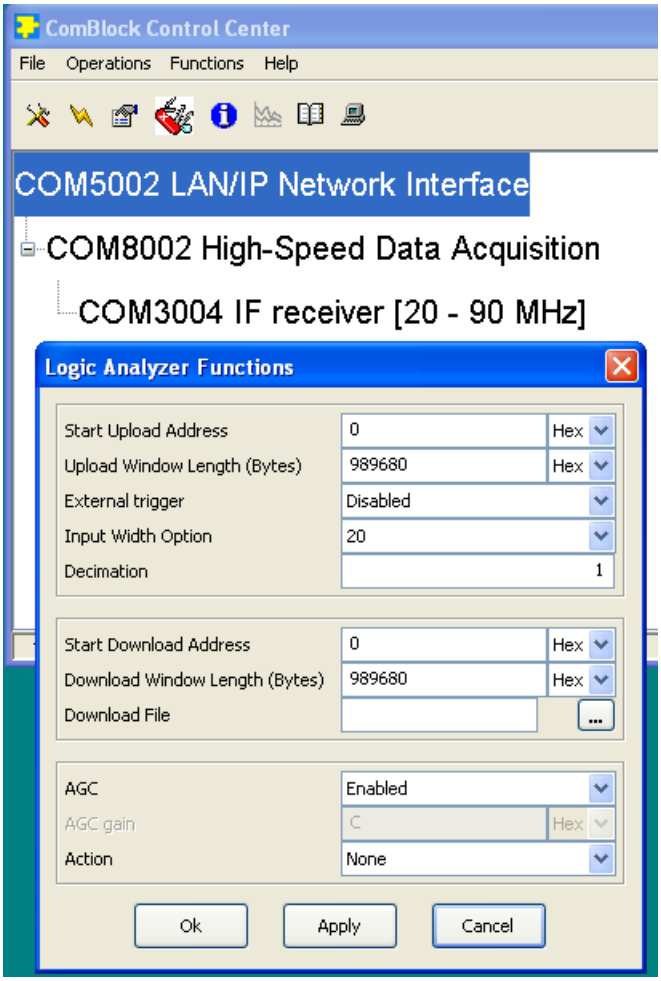
In particular, selecting the $\mathbf{f_{clk}}$ processing clock as real-time sampling clock allows one to have the same time-scale for all signals.

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.



ComScope Window Sample: showing I/Q baseband signal from RF receiver

Operation



Data Acquisition

Step1: Using the ComBlock Control Center (graphical user interface) configure the upload mode:

- define the upload start address and upload window length
- select the input format width.
- select the external trigger when applicable.
- press the 'Apply' button.

Step2: Using the ComBlock Control Center, start data acquisition:

- select the "Start upload" action.
- press the 'Apply' button.

When external trigger is selected, the data collection will wait until a pulse is present on the EXT_TRIGGER_IN input pin.

Data acquisition automatically stops when the specified upload window length is full.

Download

Step 1: Using the ComBlock Control Center, set the COM-8002 in download mode and define the start address where data is to be stored in memory.

Step 2: Using the ComBlock Control Center, download the binary file.

- select the "Start download" action.
- press the 'Apply' button.

A progress bar shows the percentage of completion.

AGC

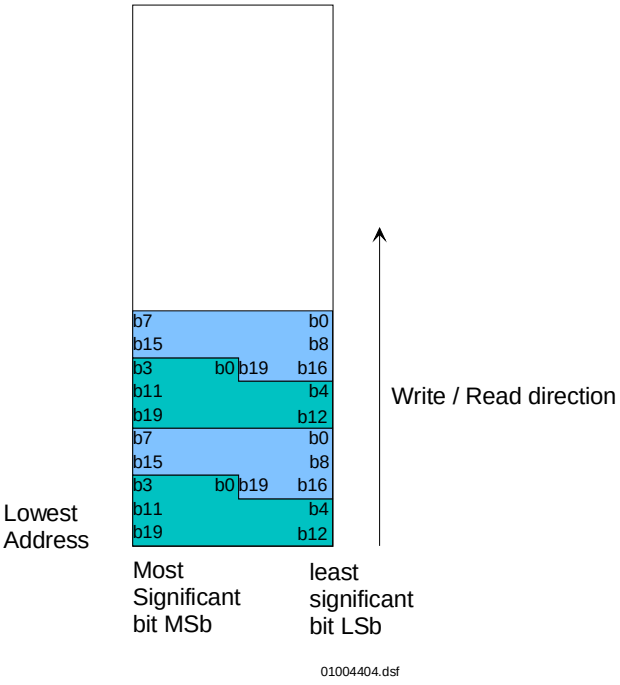
Because the COM-8002 can be connected directly to a RF receiver, it is capable of controlling the RF receiver gain. The purpose of the AGC is to make full use of the external A/D dynamic range while preventing saturation.

The AGC gain can be enabled or fixed at a given level (for example during level measurements).

The AGC circuit assumes that the input consists of two complex 10-bit samples, unsigned format (consistent with the COM-300x family of RF receivers).

Output sample width & file format

The issue of packing n-bit wide samples in a byte-oriented file format must be given some consideration. The diagram below illustrates how 20-bit wide samples are stored in a file:



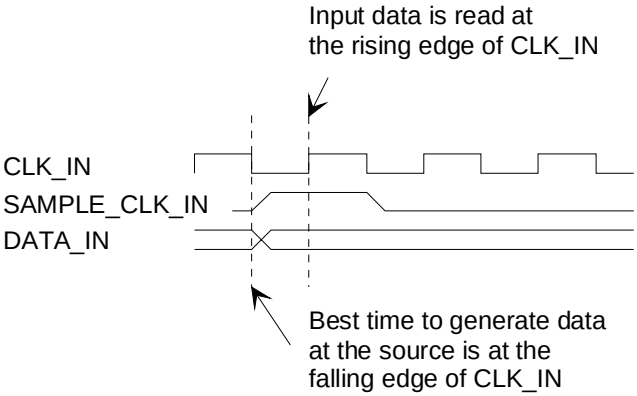
Please be aware of possible bit reversal at the interface between the COM-8002 input and the preceeding module's output. For instance, the COM-3001 dual band receiver module uses pins DATA_OUT(0) and DATA_OUT(10) as most significant bits for the I and Q output samples respectively.

Conversion utilities for the most common configuration are available in Matlab, C-language source codes and .exe executable forms. They can be downloaded from
www.comblock.com/download/com8002util_002.zip
The 'fileunpacker.exe' utility is recommended for ease of use and speed.

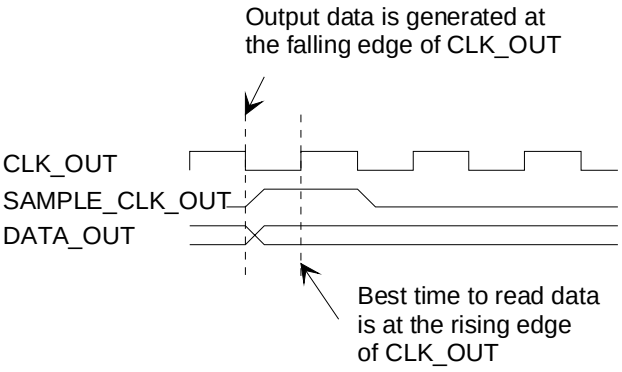
Timing

The I/O signals are synchronous with the rising edge of the reference clock CLK (i.e. all signals transitions always occur after the rising edge of the reference clock CLK). The maximum CLK frequency is 40 MHz.

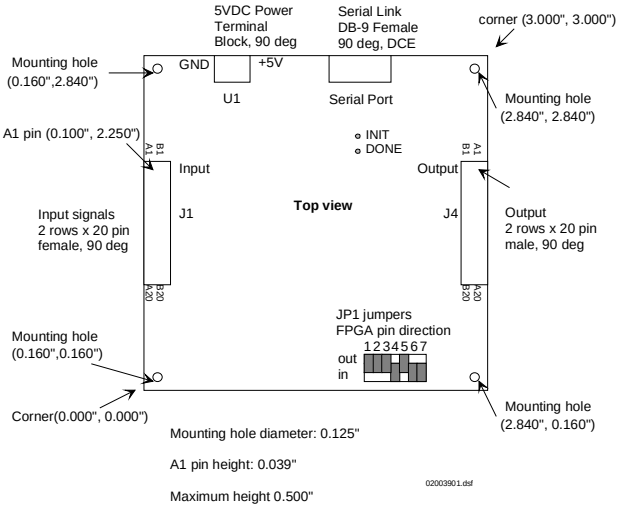
Input



Output



Mechanical Interface



Note: All seven JP1 jumpers must be in the 'IN' location.

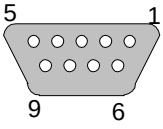
Schematics

The board schematics are available on-line at http://comblock.com/download/com_8001schematics.pdf

Pinout

Serial Link P1

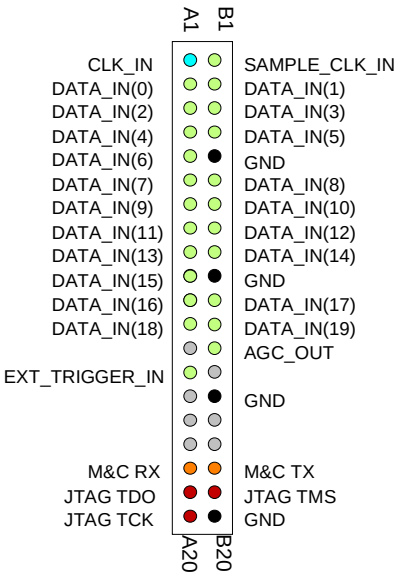
The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required. This connection can only be used for ComBlock remote monitoring and control. It cannot be used for data stream transfer.



DB-9 Female

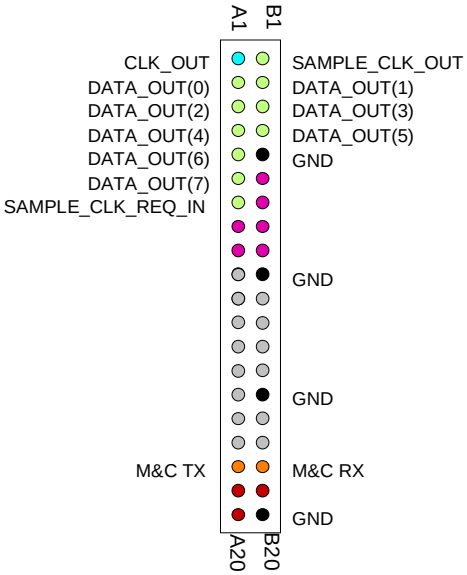
2 Transmit
3 Receive
5 Ground

Input Connector J1



When input sample precision of less than 20 bits is selected, the lower ranking bits are used. For example, for a 2-bit precision input sample, DATA_IN(0) and DATA_IN(1) are used.

Output Connector J4



I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-3001/2/3/4/5/6 RF receivers	COM-5003 TCP-IP / USB Gateway
COM-1001 BPSK/QPSK/OQPSK digital demodulator	
COM-1008 variable decimation	
COM-1011/1018 DS spread-spectrum demodulator	
COM-1027 FSK/MSK/GFSK/GMSK demodulator	
COM-7001 Turbo code decoder	

Configuration Management

This specification is to be used in conjunction with VHDL software revision 7.

It is possible to read back the option and version of the active software currently configuring the FPGA using the ComBlock Control Center. Highlight the COM-8002 module and click on the settings button (third from left). The option and version are listed at the bottom of the configuration panel.

ComBlock Ordering Information

COM-8002 HIGH SPEED DATA ACQUISITION, 256MB 40 MS/s.

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