COM-8004
SIGNAL DIVERSITY SPLITTER

Key Features

- Signal diversity splitter creates up to eight time-delayed replica at the transmitter to be used in conjunction with signal diversity combining techniques at the receiving end of the link.
- Large (256 MB) memory for very large time-diversity.
- Inserts periodic frame synchronization sequences at transmission.
- Maximum throughput is 20Mbit/s divided by the number of replica.

COM-8004 Signal Diversity Splitter

- Connectorized 3"x 3" module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right). Single 5V supply with reverse voltage and overvoltage protection. Interfaces with 3.3V LVTTL logic.

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com8004.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .

Typical Application

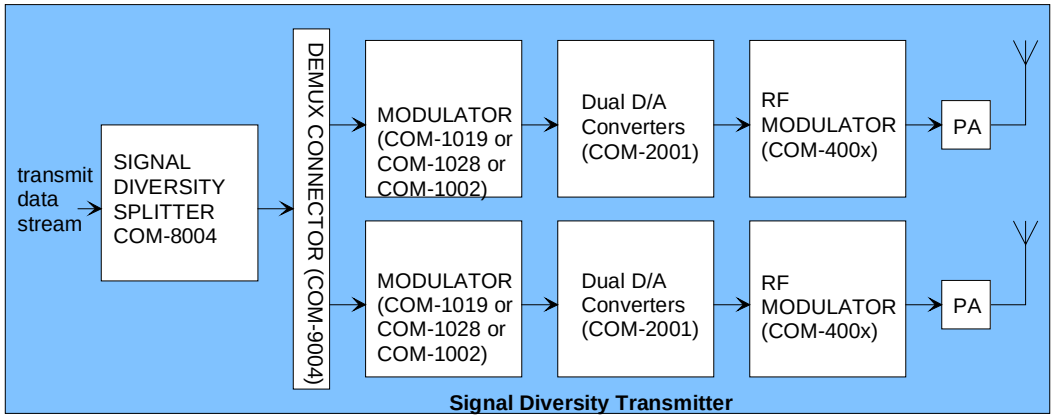
When used in conjunction with other ComBlocks, the COM-8004 is capable of implementing time-diversity, frequency-diversity, space-diversity and modulation-diversity schemes.

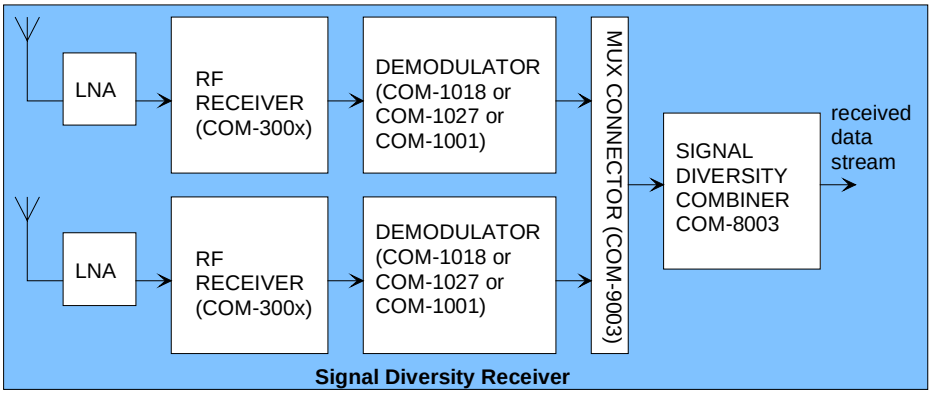
A typical setup to demonstrate multiple signal diversity combining techniques is shown below.

At the transmitter, the COM-8004 module splits an FEC encoded input data stream into two streams. Each stream is subject to a fixed independently programmable delay (for time diversity). In addition, periodic synchronization markers are inserted in each stream. Each stream replica is then modulated and transmitted at a distinct frequency (for frequency diversity). Two antenna can be used for space diversity.

At the receiver, two receivers/demodulator chains are used to recover two replica of the transmitted data stream(s). The COM-8003 recovers the frame synchronization for each stream, re-aligns the replicas in time by creating differential delays, then sums the two replicas to improve the signal to noise ratio. The resulting combined streams is then forwarded to a FEC decoder.

MSS • 18221 Flower Hill Way #A • Gaithersburg, Maryland 20879 • U.S.A.
Telephone: (240) 631-1111 Facsimile: (240) 631-1676 www.ComBlock.com





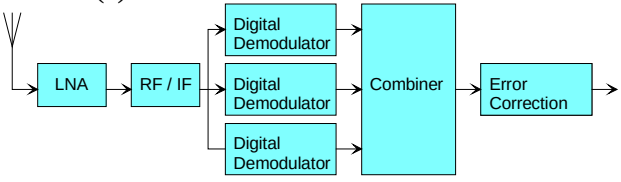
This generic assembly can be modified to implement a variety of other diversity techniques such as

- Single Input Multiple Output (SIMO) space diversity: one transmit chain only.
- modulation diversity: use different modulations for each replica.

Signal Diversity Combining Principle

Signal diversity combining is a method whereby a signal is transmitted over several media (satellite links for example) to improve the quality of service.

The receiver is a multi-channel receiver. It is designed to process multiple signals from the antenna(e) to the baseband demodulators.



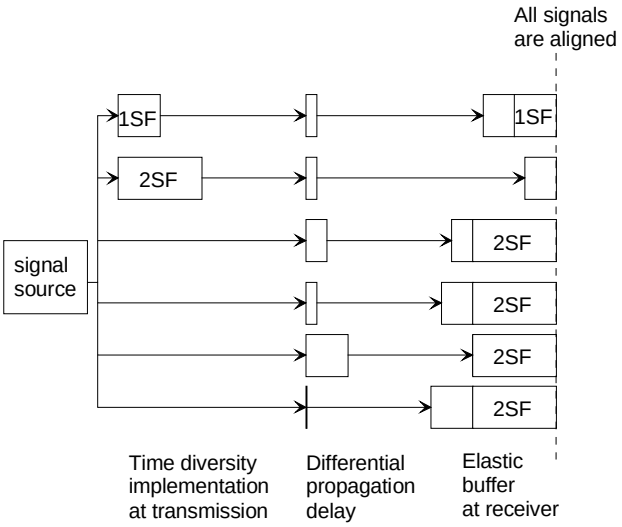
Receiver block diagram (3 signal diversity)

The COM-8003 combiner processes these demodulated signal replicas by removing the differential delay and summing the signals to yield the best signal to noise ratio.

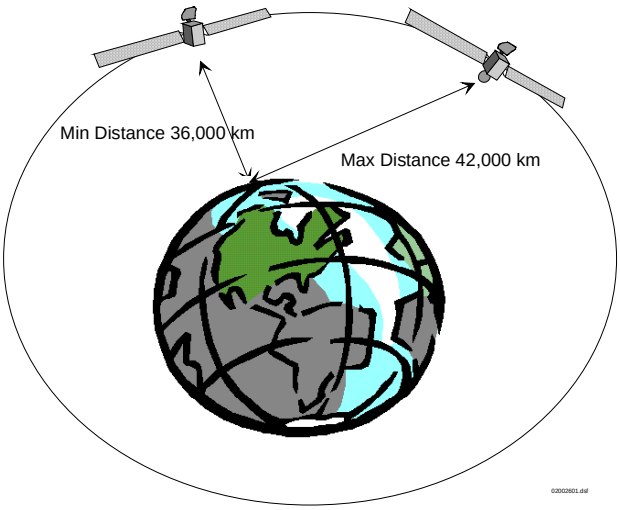
How does summing the received signals coherently improve the signal to noise ratio?
Let us consider the simplified case of two received signals of equal amplitude S and equal noise amplitude N. After summing in amplitude (coherently), the resulting signal has an amplitude $S_{sum} = 2S$ and noise amplitude $N_{sum} = sqrt(2).N$ (summing two independent random variables). The signal to noise ratio improvement is thus 3 dB.

A frame structure with synchronization header is used to synchronize all received signals.

Because of the propagation time difference, the received signals are offset in time. They must be re-aligned prior to combining. In order to help with the synchronization, a unique short synchronization sequence is inserted periodically in the transmitted data stream. A 32-bit synchronization sequence is typically a good tradeoff between probability of acquisition in extreme noise conditions and minimum overhead.



Delay considerations: there is no intrinsic processing delay associated with signal diversity combining. Received signals are only stored until the trailing replica is received (maximum one-way propagation time difference for GEO constellation is 40 ms).



maximum differential propagation delay is 12,000 km / 3 x 10^8 m/s = 40 ms (GEO)

Each signal is structured with a short frame and a longer superframe. The frame size is fixed at 4128 bits (4096 data bits plus 32 unique word bits) to minimize the sync pattern overhead (less than 1% overhead). A superframe structure comprising an integer number of frames is required to eliminate any time-of-arrival ambiguity.

The superframe size is defined by 2*(maximum differential propagation delay among replicas), rounded up to an integer number of frames. By consequence, the superframe size depends on the data rate.
Example:

- Data rate: 5 Kbps
- Maximum differential propagation delay among replicas: 4ms (12,000 km/c)
- Equivalent number of bits in differential delay: 20 bits
- Minimum superframe size = 1 frame = 4128 bits

There are, however, operational cases whereby a signal is transmitted n superframes earlier than the other replicas. This method can be used to provided time diversity in a broadcast network for example. In such a case, the SDRAM section for a given signal can be increased from 2 to n+2.

Electrical Interface

Inputs/Outputs

Input Module Interface	**Definition**
DATA_IN	Input serial data stream. Synchronous with CLK_IN.
SAMPLE_CLK_IN	Input bit clock. One CLK_IN wide pulse. Read the input data at the rising edge of CLK_IN when SAMPLE_CLK_IN = '1'.
SAMPLE_CLK_IN_REQ	Output. One CLK_IN-wide pulse. Requests a data bits from the module upstream. For flow-control purposes.
CLK_IN	Input reference clock for synchronous I/O. DATA_IN and SAMPLE_CLK_IN are aread at the rising edge of CLK_IN. Maximum 40 MHz.
Output Module Interface	**Definition**
BUS_CLK_OUT	40 MHz output reference clock for use on the synchronous bus.
BUS_ADDR[3:0]	Bus address. Output (since this module is the bus Master). Designates which slave module is targeted for this read or write transaction. All 1's indicates that the write data is to be broadcasted to all receiving slave modules. Read at the rising edge of BUS_CLK_OUT.
BUS_RWN	Read/Write#. Output (since this module is the bus Master). Indicates whether a read (1) or write (0) transaction is conducted. Read at the rising edge of BUS_CLK_OUT. Read and Write refer to the bus master's perspective.
BUS_DATA[15:0]	Bi-directional data bus. Output when BUS_RWN='0'. Input when BUS_RWN='1'. Read data latency is 2 clock periods after the read command. Functional definition during write: • bit 0 SAMPLE_CLK_OUT. '1' when DATA_OUT is available • bit 1 DATA_OUT data stream to modulator. • bits(15:2) undefined Functional definition during read: • bit 0 SAMPLE_CLK_OUT_REQ requests data from the source. Used for flow control. • bits(15:1) undefined

Other I/Os

Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control.
Power Interface	4.75 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the CLK frequency. The maximum power consumption at 40 MHz is 600mA.

Important: I/O signals are 0-3.3V LVTTL. Inputs are NOT 5V tolerant!

Configuration

Complete assemblies can be monitored and controlled centrally over a single serial or, when available through adjacent ComBlocks, LAN/TCP-IP, USB 2.0 or CardBus/PCMCIA connection.

The module configuration parameters are stored in non-volatile memory. All control registers are read/write.

This module operates at a fixed internal clock rate $\mathbf{f_{clk}}$ of 40 MHz.

Undefined control registers or register bits are for backward software compatibility and/or future use. They are ignored in the current firmware version.

Programmers developing custom applications (using the ComBlock API instead of the supplied ComBlock Control Center graphical user interface) should know that most changes are enacted upon (re-)writing to the last control register (REG16).

Parameters	**Configuration**
Active streams	Enable individual bit streams for combining/splitting. Bit 0 set to enable bit stream 0. Bit 1 set to enable bit stream 1. Bit 2 set to enable bit stream 2. Bit 3 set to enable bit stream 3.

	Bit 4 set to enable bit stream 4. Bit 5 set to enable bit stream 5. Bit 6 set to enable bit stream 6. Bit 7 set to enable bit stream 7. Any stream can be enabled or disabled, even stream 0. However, for proper operation, it is essential that all enabled streams are connected through the bus to active transmitters / modulators operating at exactly the same bit rate. REG0 bits 7-0
Super Frame Length	Number of frames per superframe. Expressed in integer multiples of frames. Unsigned value. Valid values are restricted to 2,4,8,16,32,64,128. The superframe length is generally selected to be the smallest value consistent with unambiguous time-of-arrival detection at the receiver. A length of 2 is not recommended if phase ambiguity is to be resolved for coherent n-PSK demodulators. REG1 bits 7-0
Delay Stream *n*	Time diversity differential delay for stream *n*. Expressed as number of super frames delayed with respect to stream 0. Stream 0 is the reference and is not subject to any delay. The delay is unsigned. 0 is a valid delay. The maximum delay is 256 MB. *n* BITS 15-8 BITS 7-0 1 REG3 REG2 2 REG5 REG4 3 REG7 REG6 4 REG9 REG8 5 REG11 REG10 6 REG13 REG12 7 REG15 REG14
Test mode	00 = disabled 01 = internal generation of 2047-bit periodic pseudo-random bit sequence. (overrides external input bit stream). REG16 bits 1-0
Bypass tx formatting	Bypass the transmit frame formatting. No unique word is inserted when bypassed. 0 = insert transmit frame format. 1 = bypass transmit frame formatting. REG16 bit 2

Baseline configurations can be found at www.comblock.com/tsbasic_settings.htm and imported into the ComBlock assembly using the ComBlock Control Center File | Import menu.

Test Points

Test points are provided for easy access by an oscilloscope probe.

Test Points	Definition
J1connector pin B7	PRBS-11 (test sequence) start of sequence. Useful as trigger to compare transmitted sequence and received sequence.
J1 connector pin B8	Start of frame pulse at the SDRAM input
J1 connector pin B9	Start of superframe at the SDRAM input
J1 connector pin A9	Output stream stream 0 (through SDRAM)
TP1	FPGA DONE pin. High indicates proper download of the FPGA configuration file.

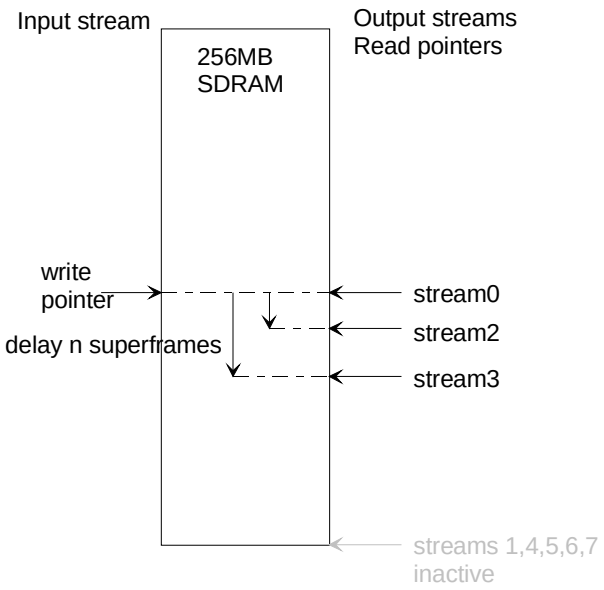
Operation

SDRAM Memory Map

The input serial data stream is packed into 64-bit words and written at sequentially incremented addresses within the 256MB SDRAM. The circular write pointer is reset to zero after a write transaction at the last word in the 256MB SDRAM memory.

Each 64-bit word write transaction is immediately followed by 64-bit read transactions for each of the active streams defined in control register REG0.

For a given stream, the SDRAM read pointer is equal to the input stream write pointer minus the user-defined delay for the associated stream. (see control registers 2 through 15). The delay is always an integer multiple of the superframe length. As stream 0 is the reference for the other streams, its offset is always zero. Zero relative delays are allowed for all streams.



SDRAM Memory Map illustration

Flow Control

A key requirement on the transmit side is that all active modulators must transmit signal replicas at exactly the same data rate. This means that all active modulators must use the same clock as timing reference for generating the modulation symbol rate.

In practice, the COM-9004 8:1 demultiplexing connector can be used to distribute the reference clock to all subsequent modulators. The modulators must be configured to use this clock as external timing reference.

The COM-8004 will hold the next SDRAM read/write transactions until all active modulators have signaled their ability to accept further data bits.

The following ComBlock modulators are designed to operate synchronously:

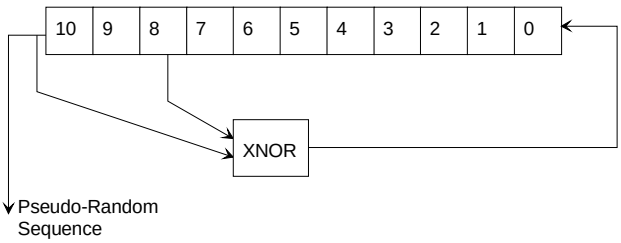
- COM-1002 BPSK/QPSK/OQPSK modulator
- COM-1019 DSSS modulator
- COM-1028 FSK/MSK/GFSK/GMSK modulator

Throughput

The maximum throughput is limited by the time-shared bus which has a total capacity of 20 Mbit/s. Therefore, the maximum throughput is 20 Mbit/s divided by the number of active streams, as defined in control register REG0.

Pseudo-Random Bit Stream (PRBS-11)

A periodic pseudo-random sequence can be used as internal test source instead of the input data stream. A typical use would be for end-to-end bit-error-rate measurement of a communication link. The sequence is 2047-bit long maximum length sequence generated by a 11-tap linear feedback shift register:

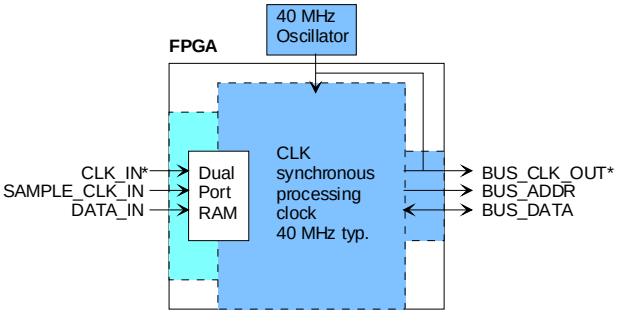


The first 100 bits of the PN sequence are as follows:
0000000000 0111111111 0011111110 0001111100 1100111000 0000010011 1111010001 1110110100 1101001100 0011000001

Timing

Clocks

The clock distribution scheme embodied in the COM-8004 is illustrated below.



Baseline clock architecture
Light blue = user defined input clock
Darker blue = internal 40 MHz clock
**** indicates edge-trigger signal***

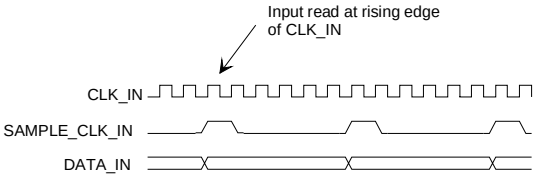
The core signal processing performed within the FPGA is synchronous with the 40 MHz processing clock locked onto a 40 MHz internal oscillator. The processing clock is not related to the CLK_IN clock.

A 4096-bit dual-port RAM elastic buffer is used at the boundary between input and internal processing area. Thus, the input clock frequency can be independent from the internal processing clock frequency.

The input signals at the J1 connector are synchronous with the CLK_IN clock at J1/A1. This clock can be up to 40 MHz.

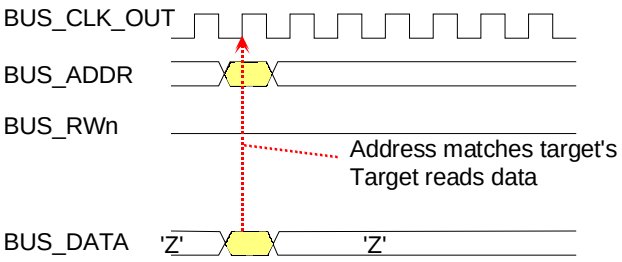
The output signals are synchronous with the rising edge of the 40 MHz reference clock BUS_CLK_OUT (i.e. all signals are stable at the rising edge of the reference clock BUS_CLK_OUT).

Input

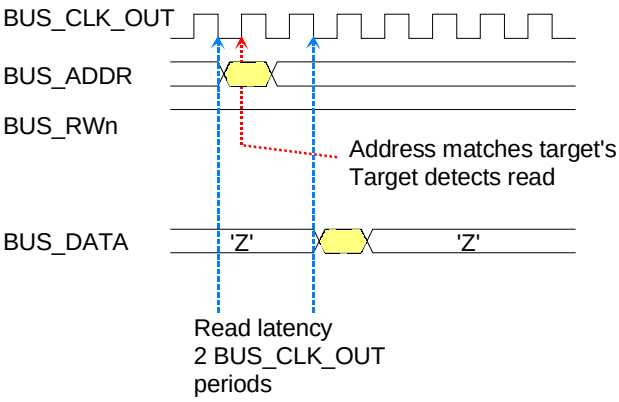


The two input signals DATA_IN and SAMPLE_CLK_IN are assessed by this ComBlock at the rising edge of the reference clock CLK_IN. Therefore, it is recommended that the source generates these two input signals at the falling edge of the reference clock CLK_IN to avoid any race condition.

Output Connector

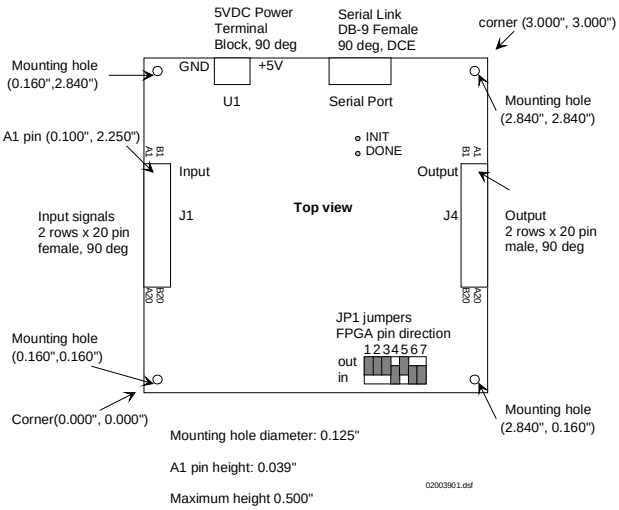


Master writes data streams to target(s)



Master reads flow control from target

Mechanical Interface

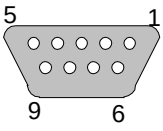


Note: All seven JP1 jumpers must be installed in the 'OUT' location.

Pinout

Serial Link P1

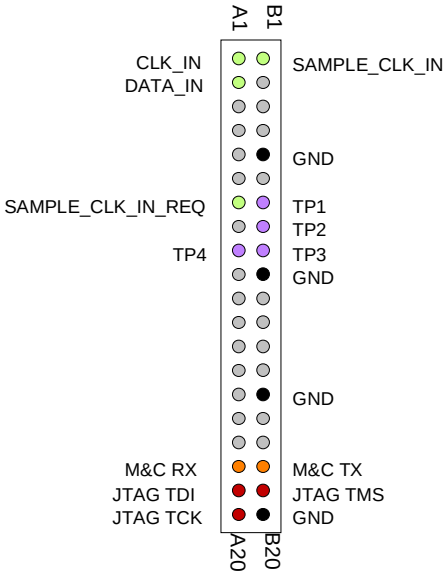
The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required.



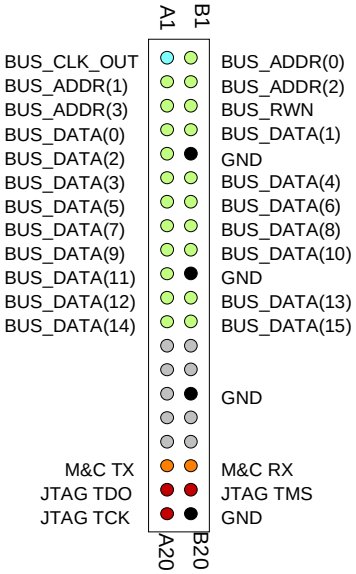
DB-9 Female

2 Transmit
3 Receive
5 Ground

Input Connector J1



Output Connector J4



COM-8004 is the bus master. It always drives BUS_CLK_OUT, BUS_ADDR and BUS_RWN.

I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-1010 Convolutional encoder	COM-9004 1:8 demultiplexing connector
COM-7001 Turbo code encoder	COM-1002 BPSK/QPSK/OQPSK modulator
COM-8001 Arbitrary Waveform Generator, 256 MB/ 1GB, 40 Msamples/s	COM-1019 Direct Sequence Spread-Spectrum Modulator
	COM-1028 FSK/MSK/GFSK/GMSK Modulator

Configuration Management

This specification is to be used in conjunction with VHDL software revision 2.

Acknowledgments

This product development was funded by SBIR Phase II research contract “Signal Diversity Combining for Improved Satellite Communications” awarded by the US Air Force Research Laboratory, Rome, NY.

ComBlock Ordering Information

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MSS • 18221 Flower Hill Way #A •
Gaithersburg, Maryland 20879 • U.S.A.
Telephone: (240) 631-1111
Facsimile: (240) 631-1676
E-mail: sales@comblock.com