COM-8005
SIGNAL DELAY / SATELLITE SIMULATOR

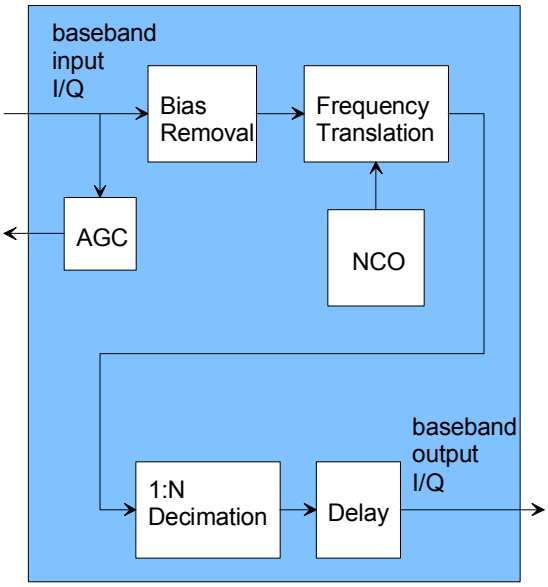
Key Features

- Programmable delay of a streaming baseband signal: up to 256MB
- Ancillary functions:
  - Frequency shift
  - AGC
  - Decimation
- Maximum sampling rate: 40 MSamples/s complex baseband signal
- Delay: 0 to 2.62 secs by steps of 0.625 µs (40Msamples/s)
- Seamless connection to ComBlock digital and RF receivers and DACs
- **ComScope** –enabled: key internal signals can be captured in real-time and displayed on host computer.
- Connectorized 3”x 3” module for ease of prototyping. Standard 40 pin 2mm dual row connectors (left, right). Single 5V supply with reverse voltage and overvoltage protection. Interfaces with 3.3V LVTTL logic.

For the latest data sheet, please refer to the **ComBlock** web site: www.comblock.com/download/com8005.pdf. These specifications are subject to change without notice.

For an up-to-date list of **ComBlock** modules, please refer to www.comblock.com/product_list.htm .

Functional Block Diagram



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Electrical Interface

Inputs

Input Module Interface	Definition
DATA_I_IN[9:0]	Modulated input signal, real axis. 10-bit precision. Format: 2's complement or unsigned.
DATA_Q_IN[9:0]	Modulated input signal, imaginary axis. 10-bit precision. Same format as DATA_I_IN.
SAMPLE_CLK_IN	Input signal sampling clock. One CLK-wide pulse. Read the input signal at the rising edge of CLK when SAMPLE_CLK_IN = '1'. Samples can be consecutive. For example, SAMPLE_CLK_IN can be fixed at '1' to indicate that new input samples are provided once per CLK_IN clock period. Signal is pulled-up.
AGC_OUT	Output. When the COM-8005 is connected directly to an analog receiver, it generates a pulse-width modulated signal to control the analog gain prior to A/D conversion. The purpose is to use the maximum dynamic range while preventing saturation at the A/D converter. 0 is the maximum gain, +3V is the minimum gain.
CLK_IN	Input reference clock for synchronous I/O. DATA_x_IN and SAMPLE_CLK_IN are read at the rising edge of CLK_IN. Maximum 40 MHz. Minimum frequency 25 MHz.

Outputs

There are two possible output formats, depending on the module connected to the output:

Complex baseband 2*10-bit I/Q (COM-2001 module interface) **Output Module Interface (Output data pushed out)**	**Definition**
DATA_I_OUT[9:0]	Modulated output signal, real axis. 10-bit precision. Format: 2's complement or unsigned, selected by configuration bit 1.
DATA_Q_OUT[9:0]	Modulated output signal, imaginary axis. 10-bit precision. Same format as DATA_I_OUT.
SAMPLE_CLK_OUT	Output signal sampling clock. Read the output signal at the rising edge of CLK when SAMPLE_CLK_OUT = '1'. SAMPLE_CLK_OUT is fixed at '1' when the modulator is enabled. Fixed at '0' otherwise.
DAC_CLK_OUT	Output sampling clock for Digital to Analog Converters. DAC reads the output sample at the rising edge.
CLK_OUT	40 MHz output reference clock. Exact same frequency as CLK_IN.

(a) 70 MHz IF waveform generation (COM-4004 module interface)

Output Module Interface	Definition
DATA_OUT[13:0]	Output. Quadrature baseband samples, up to 14-bit precision, 2's complement format. Bit 13 is the most significant bit. When a lesser precision is selected, the unused least significant bits are set to zero. The in-phase (I) and quadrature (Q) samples alternate. The samples are generated at the falling edge of SAMPLE_CLK_REQ_IN.
SAMPLE_CLK_REQ_IN	Input. Input samples are clocked at the rising edge of SAMPLE_CLK_REQ. I & Q samples alternate at each request. SAMPLE_CLK_REQ is a 100 MHz clock.
TX_ENABLE_OUT	Output. Transmit enable. Active high. The first sample after TX_ENABLE becomes active is an in-phase (I) sample. This signal is generated at the falling edge of SAMPLE_CLK_REQ_IN.

Other I/Os

Serial Monitoring & Control	DB9 connector. 115 Kbaud/s. 8-bit, no parity, one stop bit. No flow control. Used for ComBlock remote monitoring and control (no data stream).
Power Interface	4.90 – 5.25VDC. Terminal block. Power consumption is approximately proportional to the CLK frequency. The maximum power consumption at 40 MHz is 600mA.

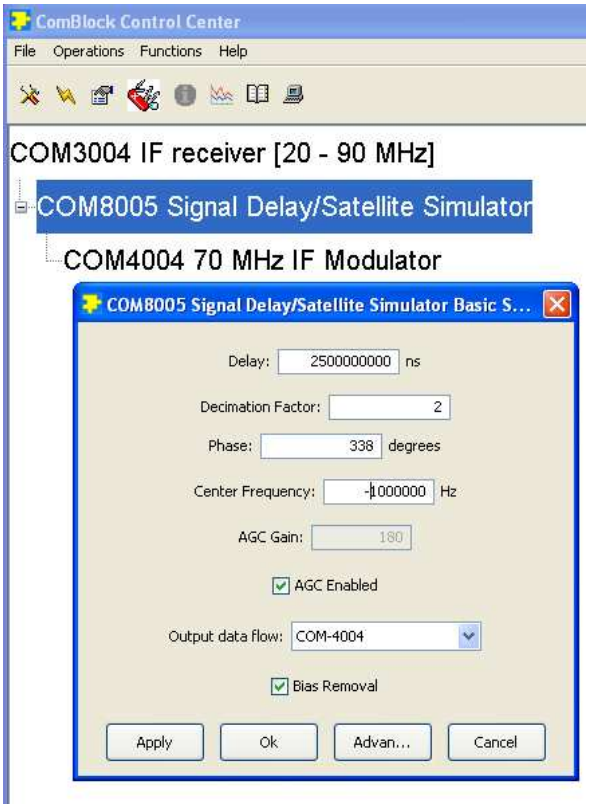
Important: I/O signals are 0-3.3V LVTTL. Inputs are NOT 5V tolerant!

Configuration

Complete assemblies can be monitored and controlled centrally over a single serial connection or, via adjacent ComBlocks, LAN, USB, or CardBus connection.

Configuration (Basic)

The easiest way to configure the COM-8005 is to use the ComBlock Control Center software supplied with the module(s). After detecting the ComBlock modules (2nd button from left), highlight the COM-8005 module to be configured. Then press the settings button (3rd button from the left).



Configuration (Advanced)

Alternatively, users can access the full set of configuration features by specifying 8-bit control registers as listed below. These control registers can be set manually through the ComBlock Control Center or by software using the ComBlock API (see www.comblock.com/download/M&C_reference.pdf)

All control registers are read/write.

Undefined control registers or register bits are for backward software compatibility and/or future use. They are ignored in the current firmware version.

This module operates at an internal processing clock rate f_{CLK_IN} (typically 40 MHz) set by the input module.

Parameters	Configuration
Delay	The output delay with respect to the input is expressed in multiple of 25 baseband input samples (after decimation). Therefore the minimum delay increment is 625ns for 40 MSamples/s, no decimation. The maximum delay is 2.62 sec for 40 MSamples/s, no decimation. Of course, the delay can be much longer when decimation is used. 0 is a valid entry. REG0 = bits 7-0 (LSB) REG1 = bits 15-8 REG2(5:0) = bits 21-16
Input Decimation factor D	The input can be subsampled by saving only one in every D input samples, while the other samples are discarded. Valid range 0 – (2^{24}-1). Input decimation is disabled when when D = 0 or 1. REG4 = bits 7-0 (LSB) REG5 = bits 15-8 REG6 = bits 23-16 (MSB)
Phase rotation	Rotate input samples in phase by increments of 360 * REG3/256 degrees. REG3
Center frequency ($\mathbf{f_c}$)	Nominal center frequency. This value is subtracted from the received signal actual center frequency. 32-bit signed integer (2's complement representation) expressed as $\mathbf{f_c} * 2^{32} / f_{CLK\_IN}$ REG7 = bits 7 – 0 (LSB) REG8 = bits 15 – 8

	REG9 = bits 23 – 16 REG10 = bits 31 – 24 (MSB)
AGC gain	Gain settings for an external RF receiver. This setting is used when the AGC is disabled. Unsigned 8-bit number. When used in conjunction with the COM-300x receivers, 255 represents the minimum gain, 0 the maximum gain. REG11
AGC enabled	Enable or disable the automatic gain control for an external RF receiver. 0 = fixed at a preset level (see REG10) 1 = enabled REG12(0)
Output data flow	0 = output data is pushed to the next module (for example to COM-2001) 1 = output data is pulled by next module (for example by the COM-4004) REG12(1)
Reserved	REG12(2) must be 0 for normal operation (1 is reserved for tests)
Bias removal	In cases where the input samples (from an external A/D converter) are biased, it can be helpful to remove the bias using a low-pass filter. If not removed, the bias may degrade the "LO leakage" performance as a spectral line will be noticeable at the output center frequency. DC biases are removed independently on the I and Q channels. The bias removal averages the bias over 1024 consecutive input samples after decimation D. 0 = disabled 1 = enabled REG12(3)
Spectrum Inversion	Invert baseband spectrum at the input (or not) to compensate for any spectrum inversion occurring prior to the COM-8005 (for example in a COM-30xx receiver). 0 = no spectrum inversion 1 = spectrum inversion REG12(4)

Writing to REG12 resets the output interface. When interfacing with the COM-4004 70 MHz modulator, any configuration change in the COM-4004 should be followed by an interface reset.

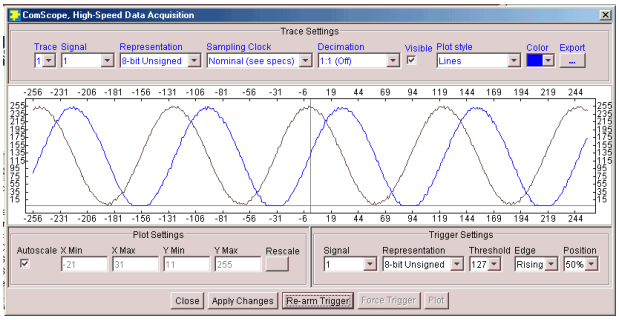
Baseline configurations can be found at www.comblock.com/tsbasic_settings.htm and imported into the ComBlock assembly using the ComBlock Control Center File | Import menu.

ComScope Monitoring

Key internal signals can be captured in real-time and displayed on a host computer using the ComScope feature of the ComBlock Control Center. The COM-8005 signal traces are defined as follows:

Trace 1 signals	**Format**	**Nominal sampling rate**	**Buffer length (samples)**
1: input from COM-300x receiver: I-channel	8-bit unsigned (8MSB /10)	f_{CLK_IN}	512
2: I-channel after frequency translation and decimation	8-bit signed (8MSB /10)	f_{CLK_IN} /decimation	512
3: Q-channel after frequency translation, decimation and delay	8-bit signed (8MSB /10)	f_{CLK_IN}	512
Trace 2 signals	**Format**	**Nominal sampling rate**	**Capture length (samples)**
1: input from COM-300x receiver: Q-channel	8-bit unsigned. (8MSB /10)	f_{CLK_IN}	512
2: Q-channel after frequency translation and decimation	8-bit signed (8MSB /10)	f_{CLK_IN} /decimation	512
3: I-channel after frequency translation, decimation and delay	8-bit signed (8MSB /10)	f_{CLK_IN}	512

The ComScope user manual is available at www.comblock.com/download/comscope.pdf.



ComScope Window Sample: showing I/Q baseband input signal from RF receiver

Operation

AGC

Because the COM-8005 can be connected directly to a RF receiver, it is capable of controlling the RF receiver gain. The purpose of the AGC is to make full use of the external A/D dynamic range while preventing saturation.

The AGC gain can be enabled or fixed at a given level (for example during level measurements).

The AGC circuit assumes that the input consists of two complex 10-bit samples, unsigned format (consistent with the COM-300x family of RF receivers).

Troubleshooting

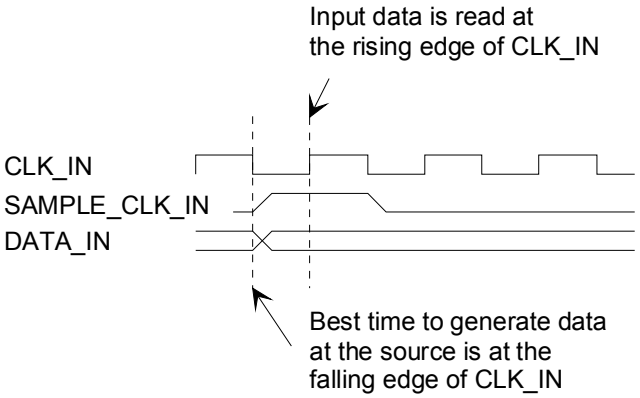
Cannot detect COM-8005 from the ComBlock Control Center

Please check that there is an input module connected to connector J1 and that there is an input clock on pin A1 (CLK_IN).

Timing

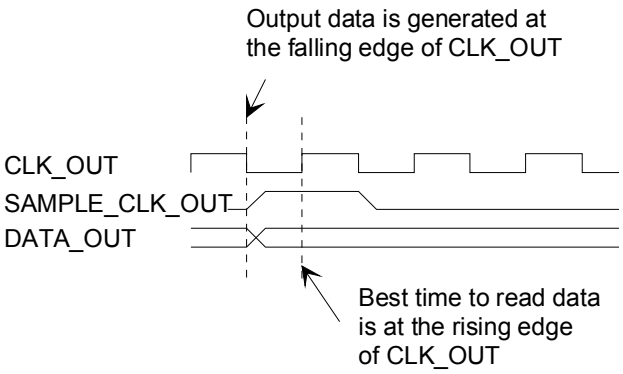
The I/O signals are synchronous with the rising edge of the reference clock CLK (i.e. all signals transitions always occur after the rising edge of the reference clock CLK). The maximum CLK frequency is 40 MHz.

Input

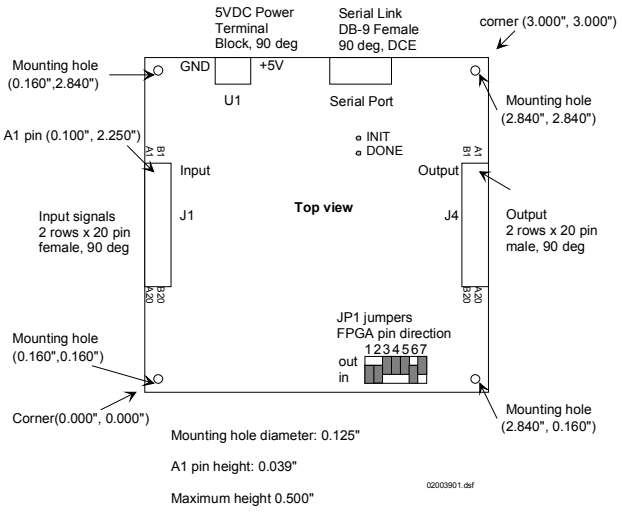


Output

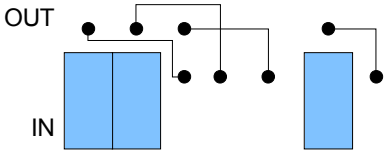
(REG11 bit1 = 0)



Mechanical Interface



Note: the JP1 jumpers must be configured as shown below



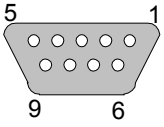
Schematics

The board schematics are available on-line at http://comblock.com/download/com_8001schematics.pdf

Pinout

Serial Link P1

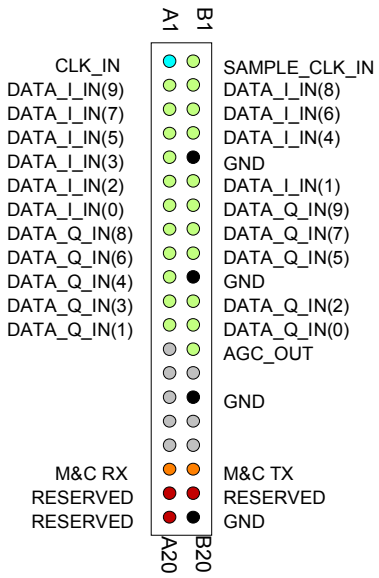
The DB-9 connector is wired as data circuit terminating equipment (DCE). Connection to a PC is over a straight-through cable. No null modem or gender changer is required. This connection can only be used for ComBlock remote monitoring and control. It cannot be used for data stream transfer.



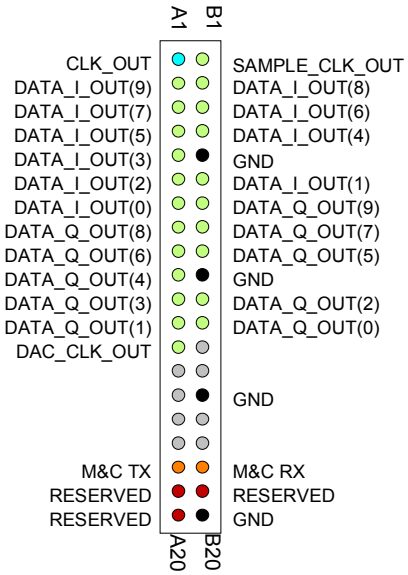
DB-9 Female

2 Transmit
3 Receive
5 Ground

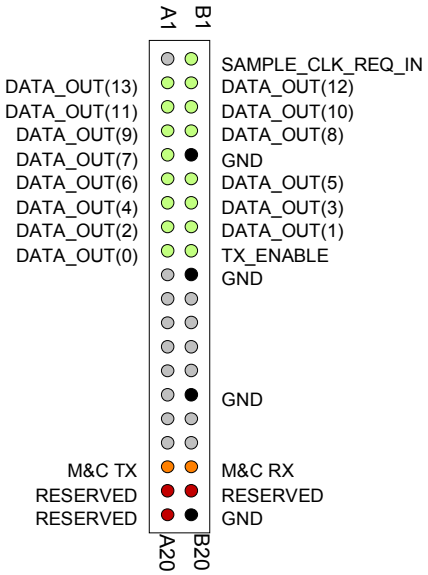
Input Connector J1



Output Connector J4



This connector is used when output data is pushed out (configuration REG11 bit1 = 0).



This connector is used when output data is pulled out by the next module (configuration REG11 bit 1 = 1).

I/O Compatibility List

(not an exhaustive list)

Input	Output
COM-3001/2/3/4/5/6/7/8/9 RF / IF / baseband receivers	COM-2001 Digital-to-Analog Conversion, Baseband
	COM-4004 70 MHz IF Modulator
	COM-1023 BER generator, Additive White Gaussian Noise Generator
	COM-1024 Multipath simulator.

Configuration Management

This specification is to be used in conjunction with VHDL software revision 4

It is possible to read back the option and version of the active software currently configuring the FPGA using the ComBlock Control Center. Highlight the COM-8005 module and click on the settings button (third from left). The option and version are listed at the bottom of the (advanced) configuration panel.

ComBlock Ordering Information

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