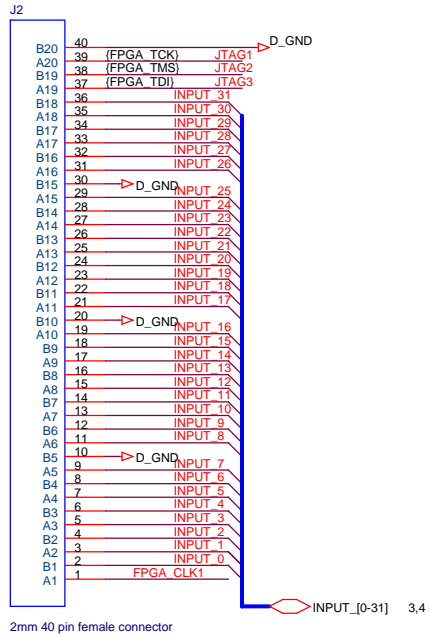


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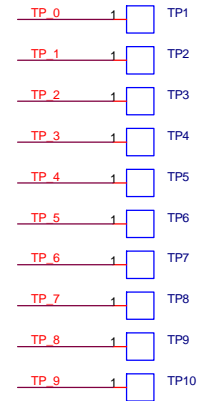
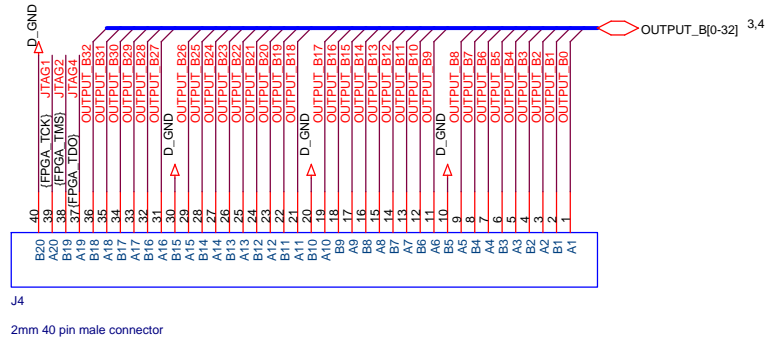
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CONNECTOR	2	+3.3V & +2.5V	5
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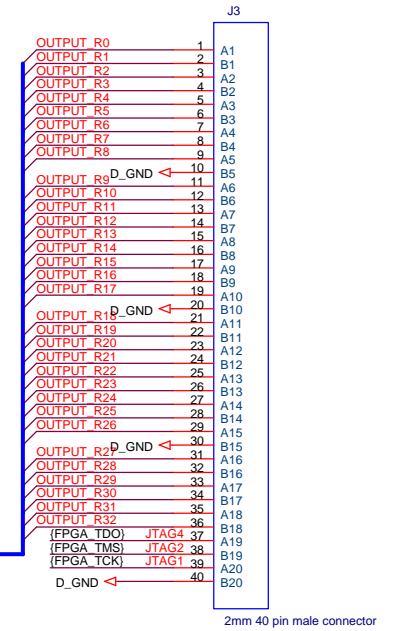
### 40 Pin INPUT - Left



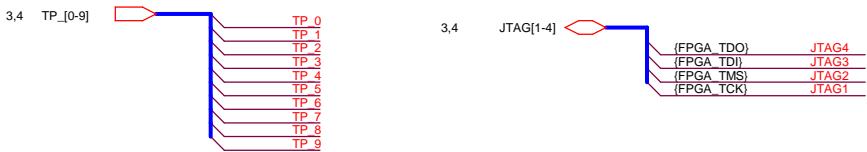
### 40 Pin OUTPUT - Bottom



### 40 Pin OUTPUT - Right

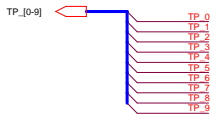


### TEST POINTS

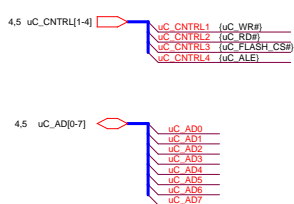


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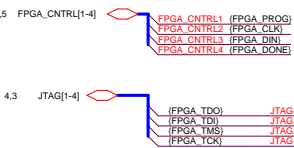
### TEST POINTS



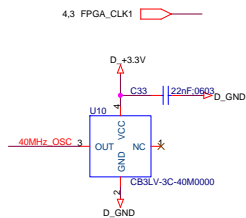
### uC INTERFACE



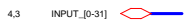
### FPGA CONFIGURATION



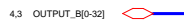
### FPGA CLOCKS



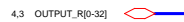
### 40 PIN INPUT - RIGHT



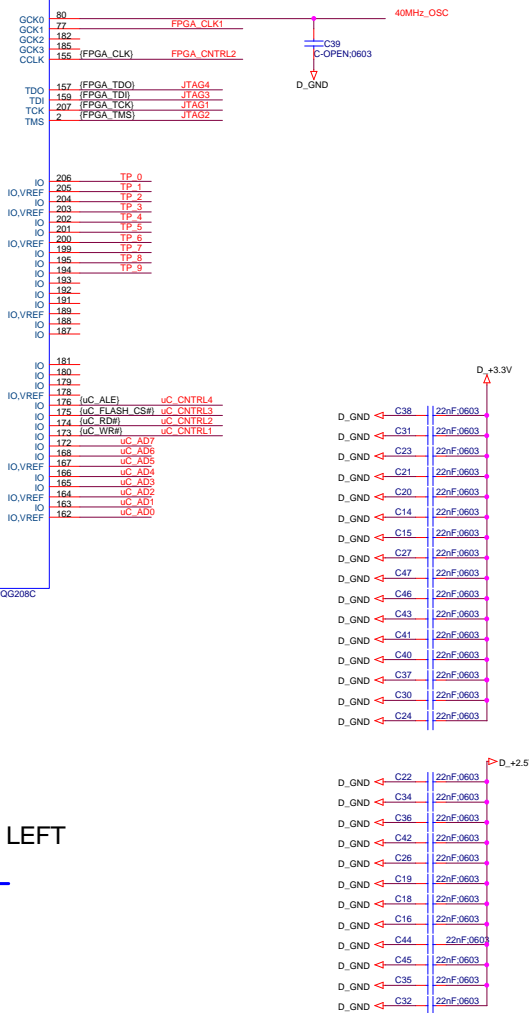
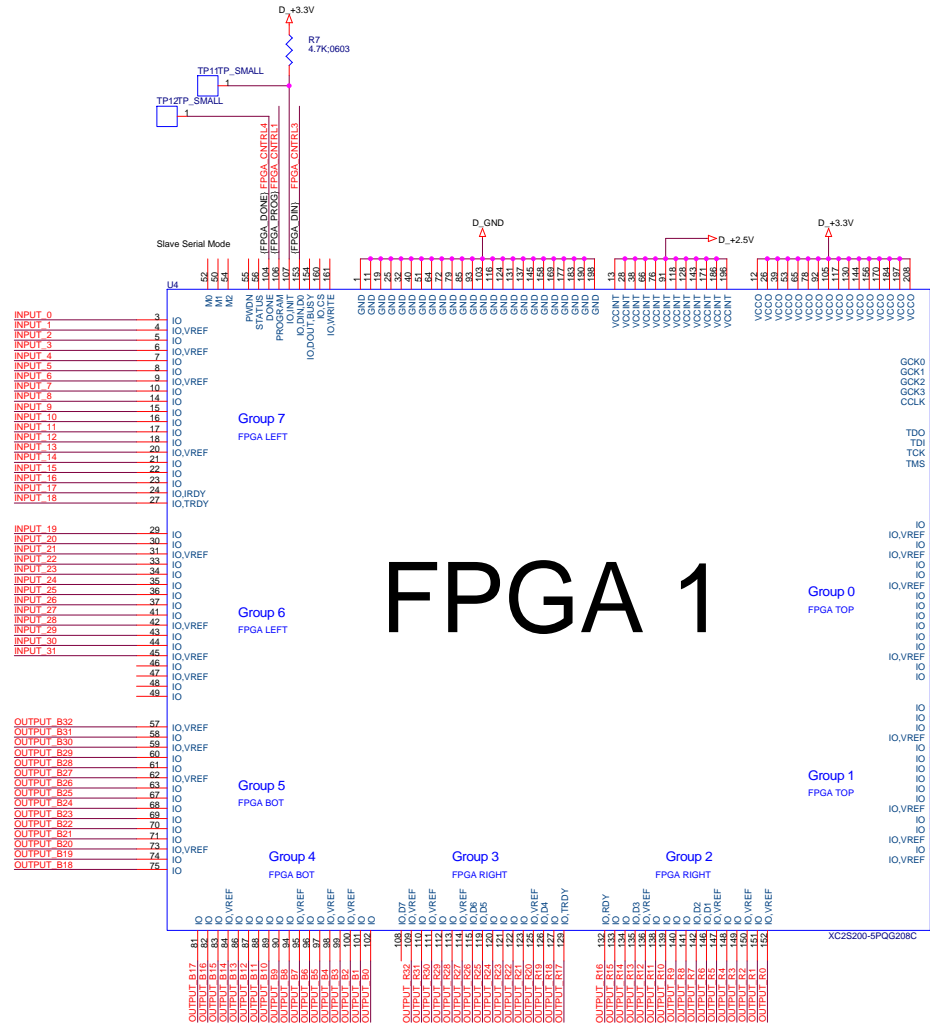
### 40 PIN OUTPUT - BOTTOM



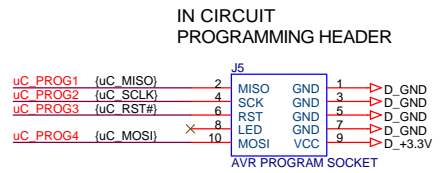
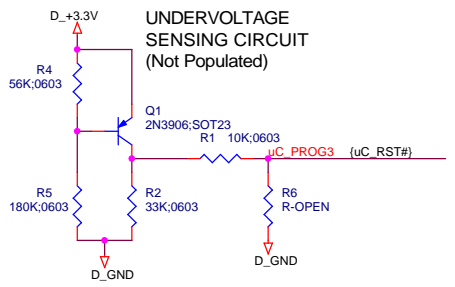
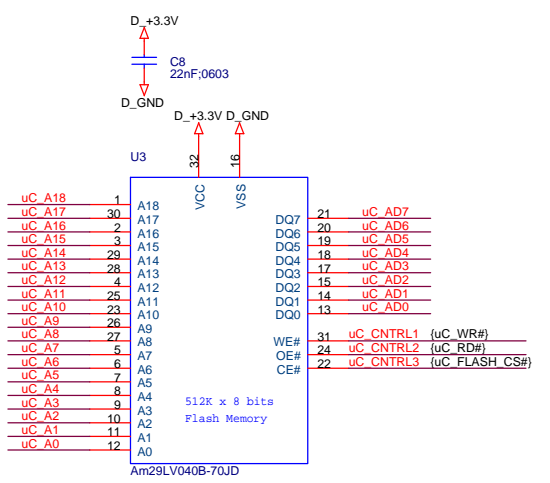
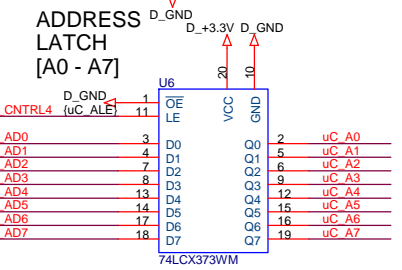
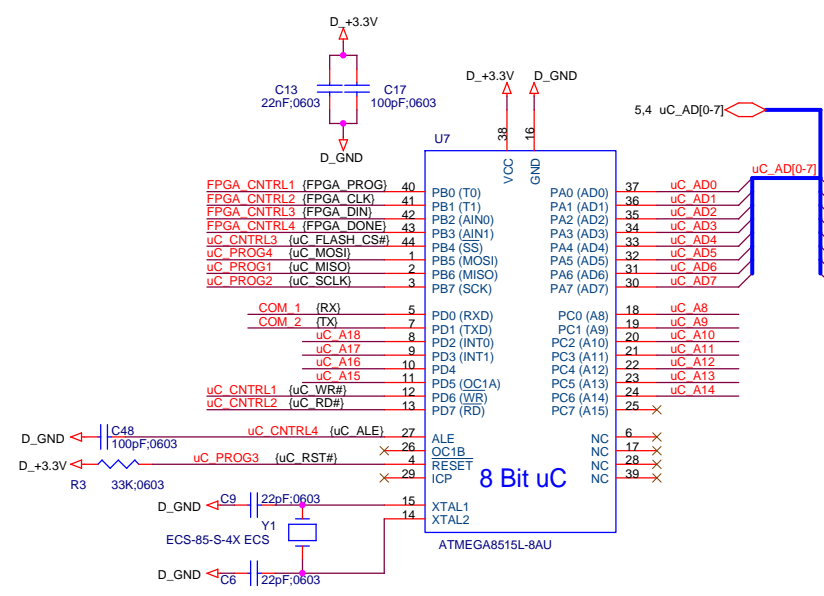
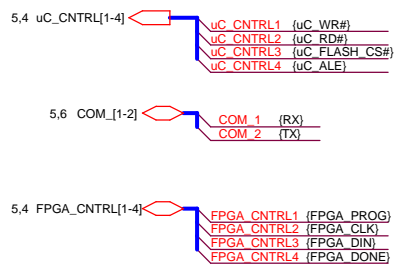
### 40 PIN OUTPUT - LEFT



# FPGA 1



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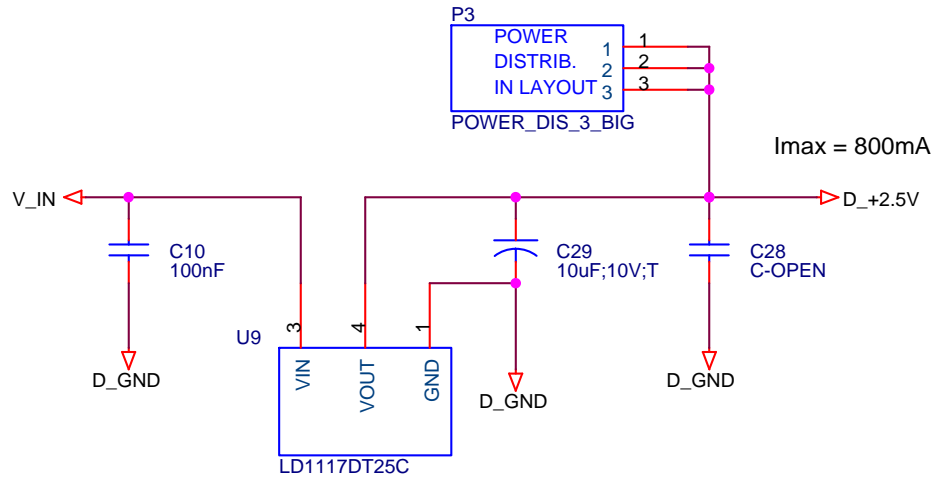
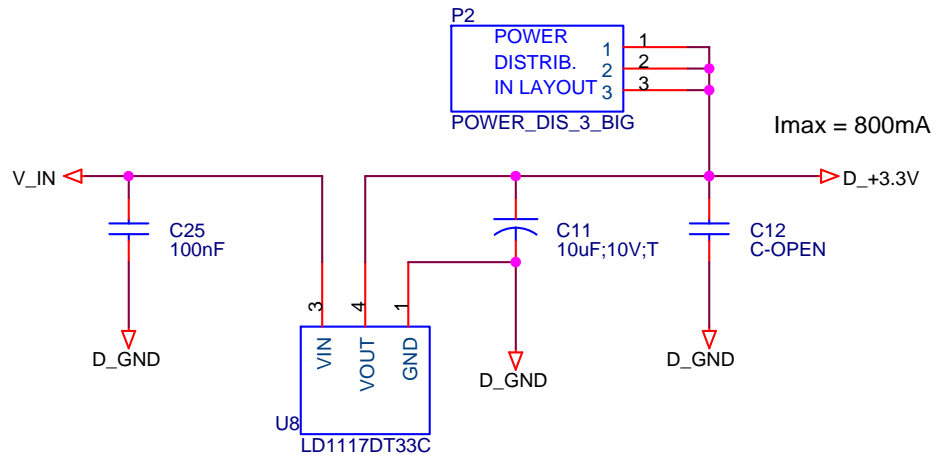
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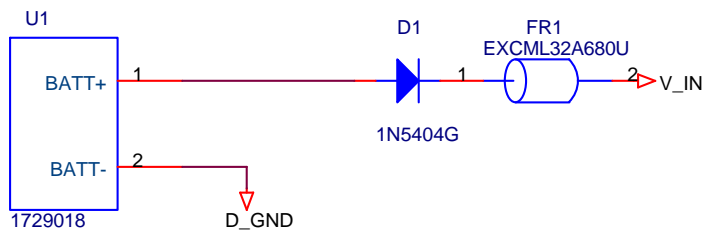
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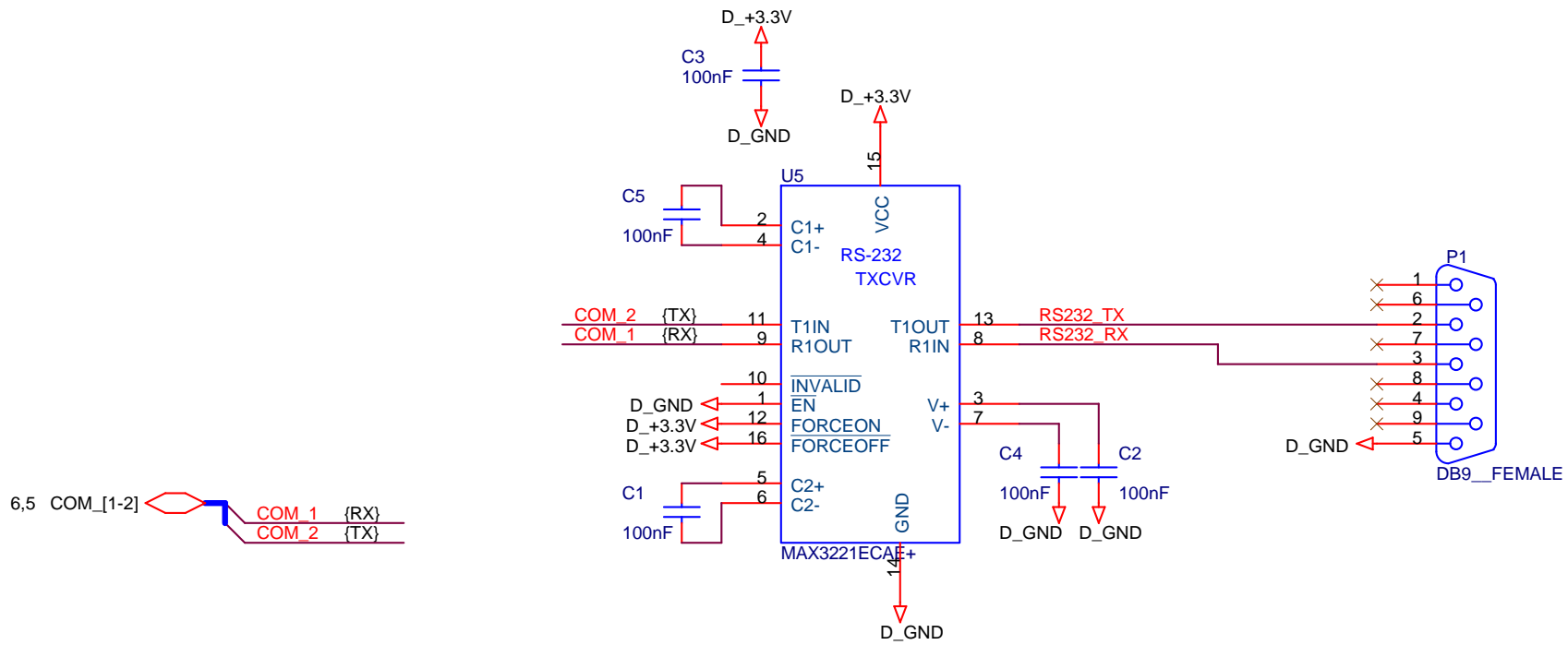
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**+5 V Supply**



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