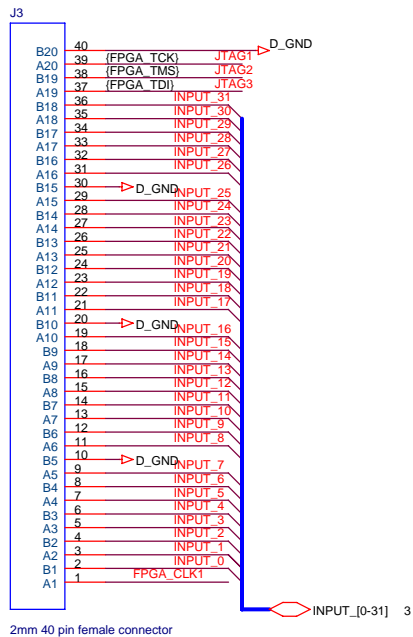


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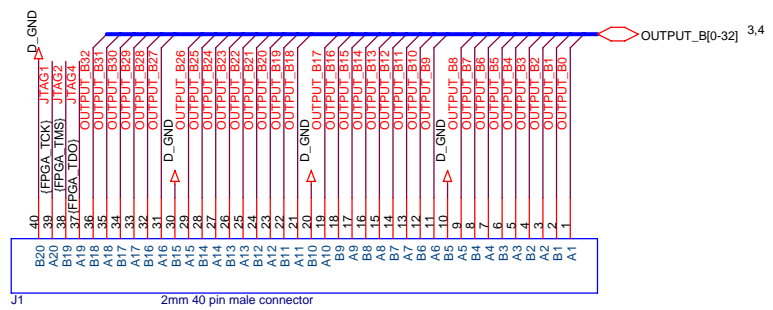
MAIN.....1	MICRO.....4
CONNECTOR.....2	POWER.....5
FPGA.....3	USB.....6

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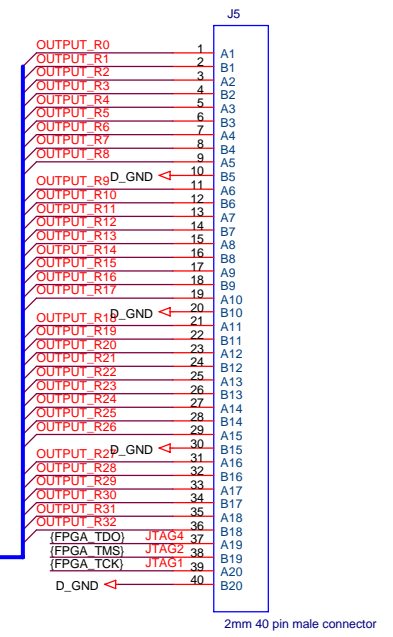
40 Pin INPUT - Left



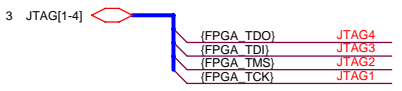
40 Pin OUTPUT - Bottom



40 Pin OUTPUT - Right



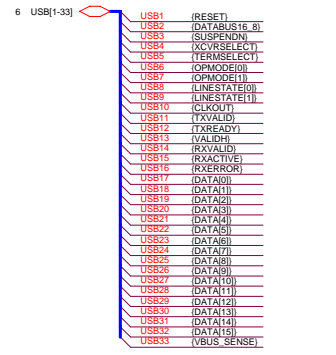
3 FPGA_CLK1



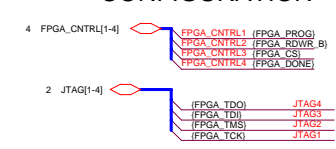
3 OUTPUT_R[0-32]

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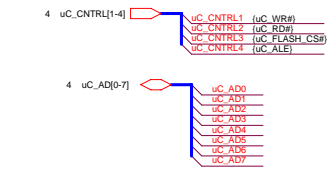
USB INTERFACE



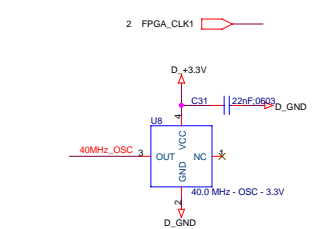
FPGA CONFIGURATION



uC INTERFACE



FPGA CLOCKS

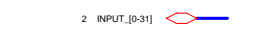


FPGA

40 PIN OUTPUT - BOTTOM



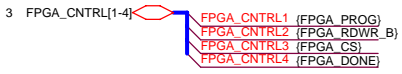
40 PIN INPUT - RIGHT



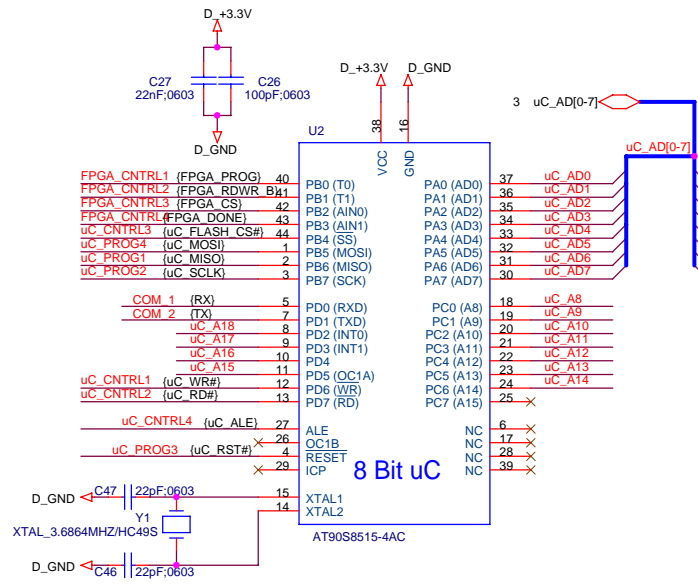
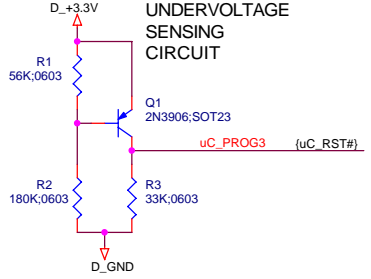
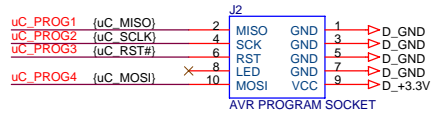
40 PIN OUTPUT - LEFT



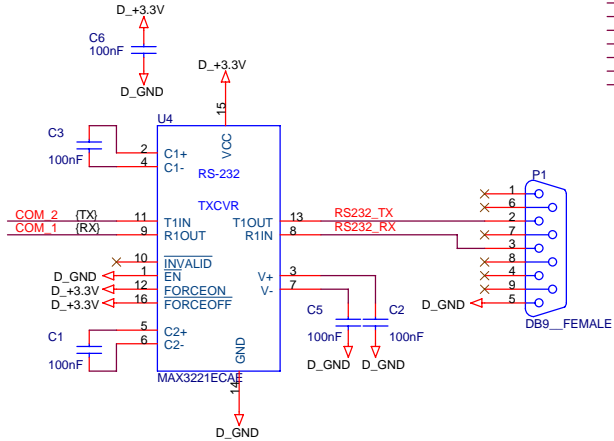
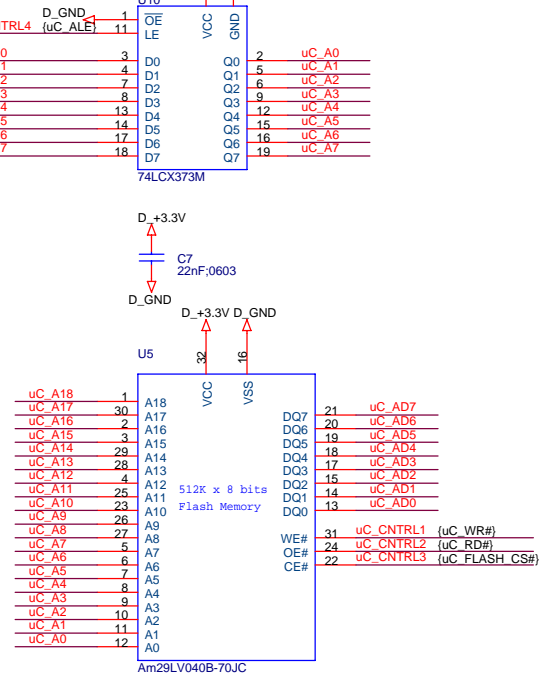
FPGA TP1	1	1	10	FPGA TP10
FPGA TP2	2	2	9	FPGA TP9
FPGA TP3	3	3	8	FPGA TP8
FPGA TP4	4	4	7	FPGA TP7
FPGA TP5	5	5	6	FPGA TP6



IN CIRCUIT PROGRAMMING HEADER



ADDRESS LATCH [A0 - A7]



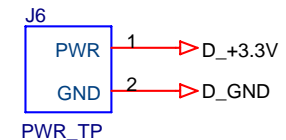
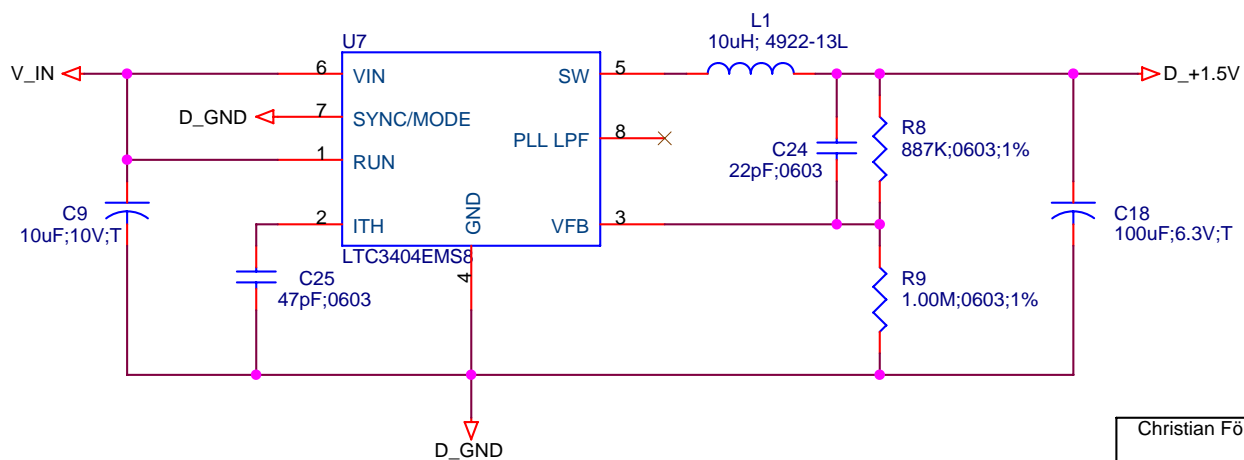
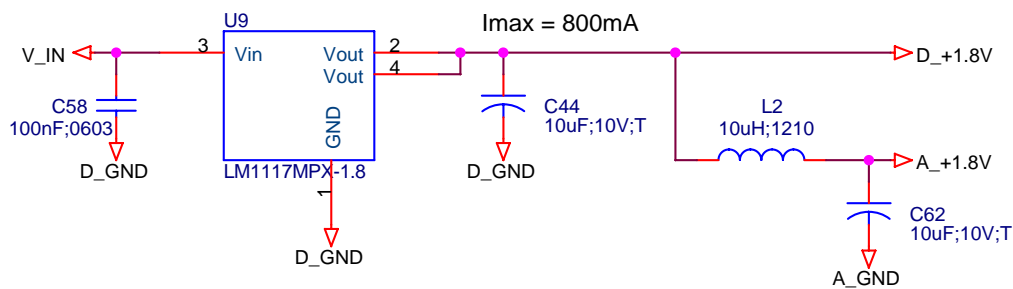
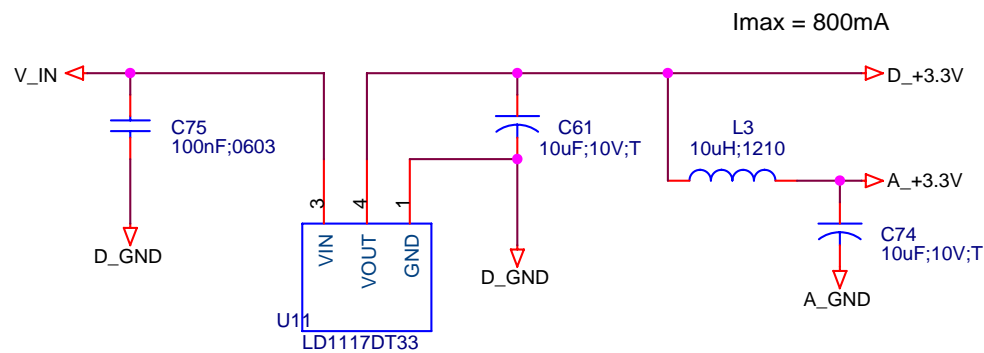
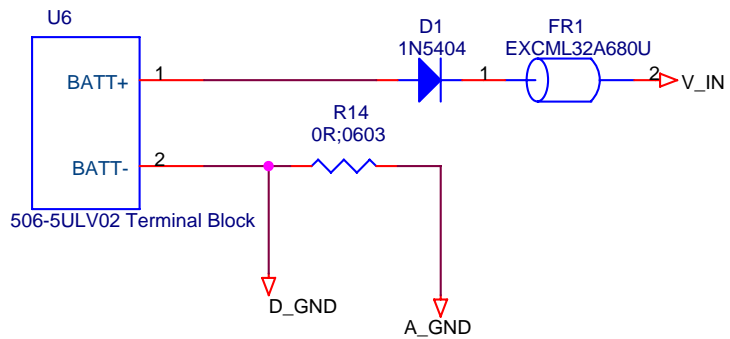
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+5 V Supply



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