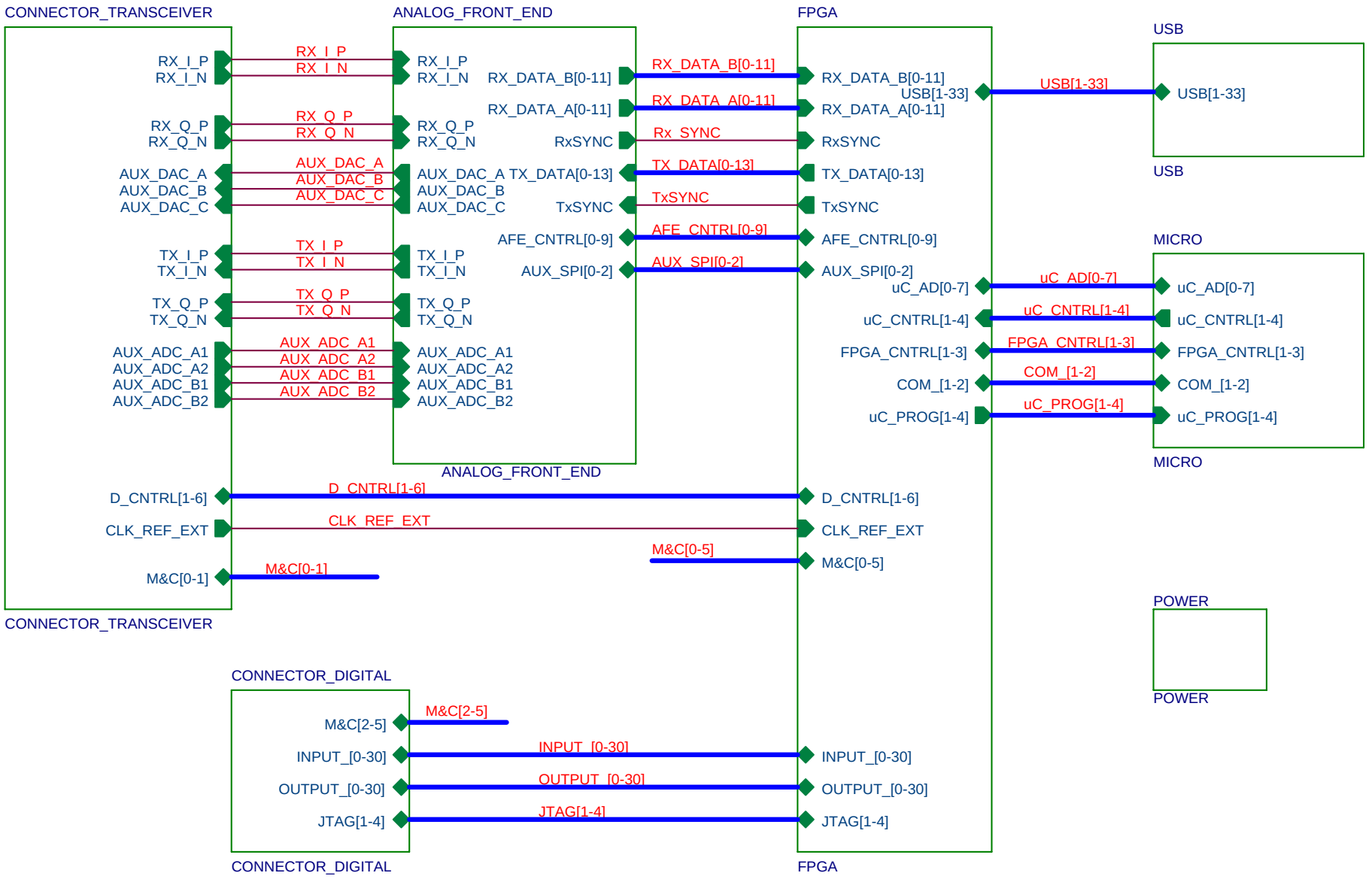

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Michael J. Yoha & Adam Kwiatkowski

Mobile Satellite Services
18221A Flower Hill Way
Gaithersburg, MD 20879

Title: COM-1200 / MAIN

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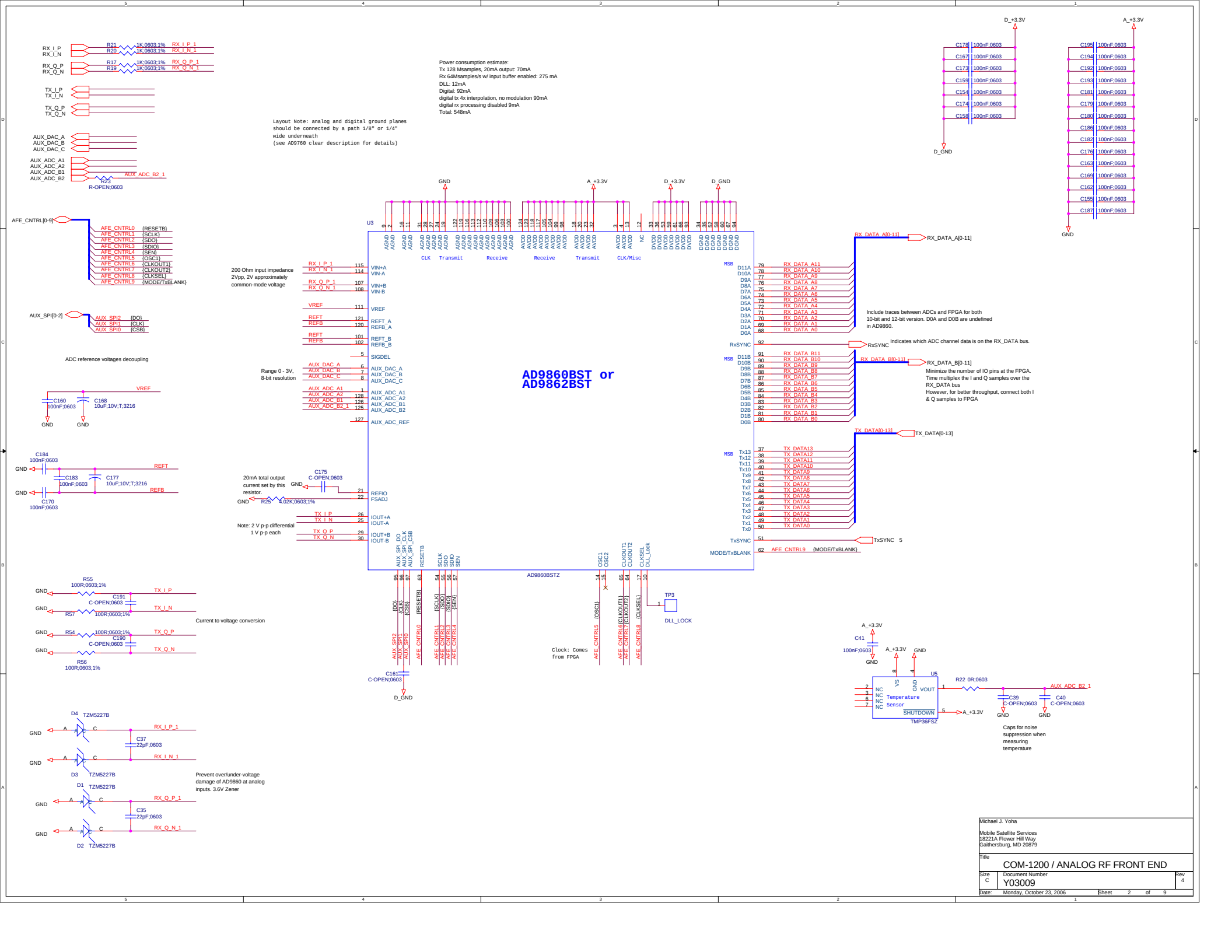
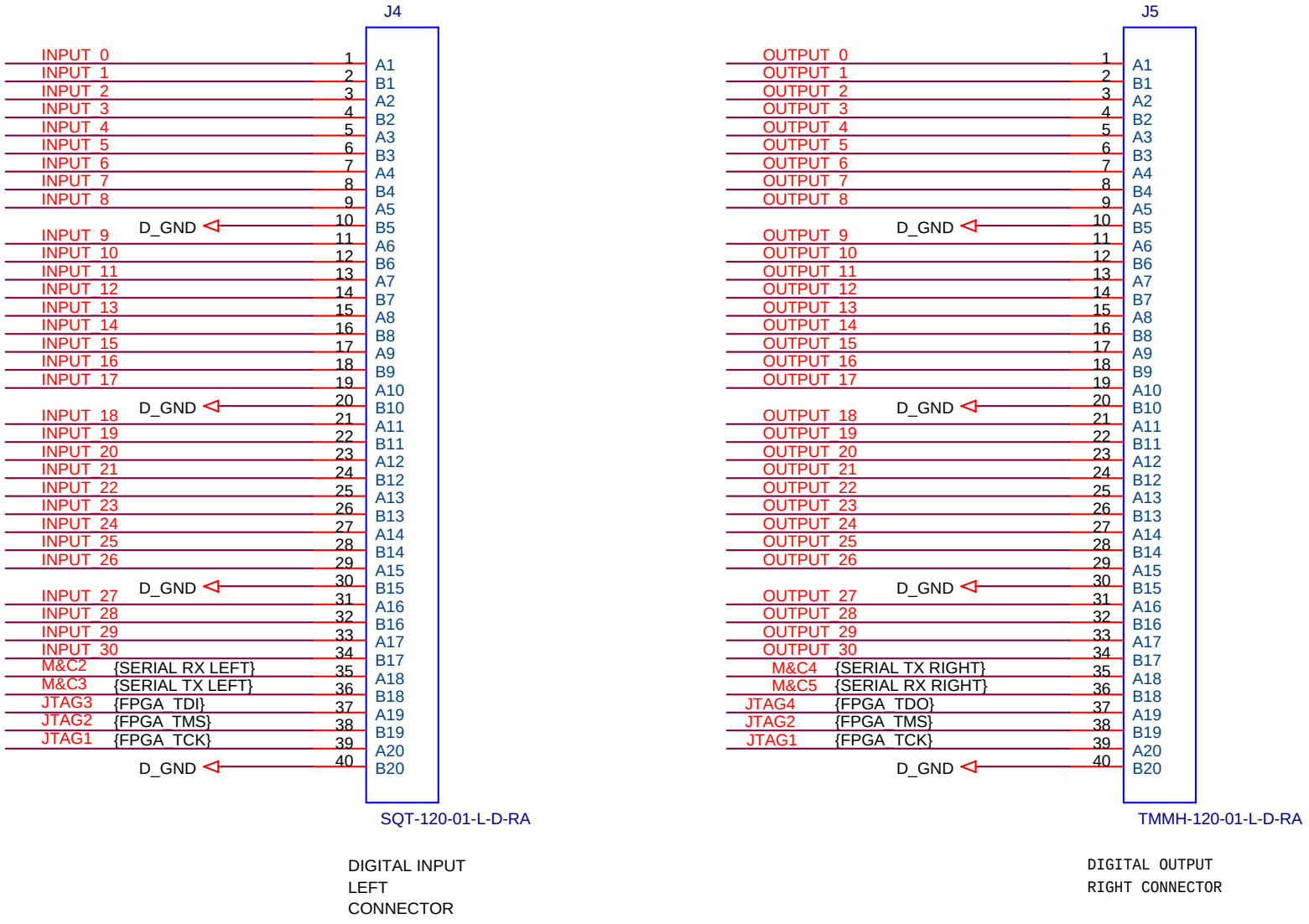

RX_I_P
RX_I_N
R21 1K;0603;1% RX_I_P_1
R20 1K;0603;1% RX_I_N_1
RX_Q_P
RX_Q_N
R17 1K;0603;1% RX_Q_P_1
R19 1K;0603;1% RX_Q_N_1
TX_I_P
TX_I_N
TX_Q_P
TX_Q_N
AUX_DAC_A
AUX_DAC_B
AUX_DAC_C
AUX_ADC_A1
AUX_ADC_A2
AUX_ADC_B1
AUX_ADC_B2
AUX_ADC_B2_1
R23
R-OPEN;0603
Layout Note: analog and digital ground planes should be connected by a path 1/8" or 1/4" wide underneath (see AD9760 clear description for details)
Power consumption estimate:
Tx 128 Msamples, 20mA output: 70mA
Rx 64Msamples/s w/ input buffer enabled: 275 mA
DLL: 12mA
Digital: 92mA
digital tx 4x interpolation, no modulation 90mA
digital rx processing disabled 9mA
Total: 548mA
D_+3.3V
C178 100nF;0603
C167 100nF;0603
C173 100nF;0603
C159 100nF;0603
C154 100nF;0603
C174 100nF;0603
C158 100nF;0603
D_GND
A_+3.3V
C195 100nF;0603
C194 100nF;0603
C192 100nF;0603
C193 100nF;0603
C181 100nF;0603
C179 100nF;0603
C180 100nF;0603
C186 100nF;0603
C182 100nF;0603
C176 100nF;0603
C163 100nF;0603
C169 100nF;0603
C162 100nF;0603
C155 100nF;0603
C187 100nF;0603
GND
AFE_CNTRL[0-9]
AFE_CNTRL0 (RESETB)
AFE_CNTRL1 (SCLK)
AFE_CNTRL2 (SDO)
AFE_CNTRL3 (SDIO)
AFE_CNTRL4 (SEN)
AFE_CNTRL5 (OSC1)
AFE_CNTRL6 (CLKOUT1)
AFE_CNTRL7 (CLKOUT2)
AFE_CNTRL8 (CLKSEL)
AFE_CNTRL9 (MODE/TxBLANK)
AUX_SPI[0-2]
AUX_SPI2 (DO)
AUX_SPI1 (CLK)
AUX_SPI0 (CSB)
ADC reference voltages decoupling
VREF
C160 100nF;0603
C168 10uF;10V;T;3216
GND
C184 100nF;0603
C183 100nF;0603
C177 10uF;10V;T;3216
C170 100nF;0603
REFT
REFB
R55 100R;0603;1%
C191 C-OPEN;0603
R57 100R;0603;1%
R54 100R;0603;1%
C190 C-OPEN;0603
R56 100R;0603;1%
Current to voltage conversion
D4 TZM5227B
D3 TZM5227B
D1 TZM5227B
D2 TZM5227B
C37 22pF;0603
C35 22pF;0603
Prevent over/under-voltage damage of AD9860 at analog inputs. 3.6V Zener
U3
AD9860BSTZ
AD9860BST or AD9862BST
CLK
Transmit
Receive
Receive
Transmit
CLK/Misc
200 Ohm input impedance 2Vpp, 2V approximately common-mode voltage
Range 0 - 3V, 8-bit resolution
20mA total output current set by this resistor.
C175 C-OPEN;0603
R25 4.02K;0603;1%
Note: 2 V p-p differential 1 V p-p each
C161 C-OPEN;0603
Clock: Comes from FPGA
TP3
DLL_LOCK
RX_DATA_A[0-11]
RX_DATA_B[0-11]
RxSYNC
TX_DATA[0-13]
TxSYNC
MODE/TxBLANK
Include traces between ADCs and FPGA for both 10-bit and 12-bit version. D0A and D0B are undefined in AD9860.
Indicates which ADC channel data is on the RX_DATA bus.
Minimize the number of IO pins at the FPGA. Time multiplex the I and Q samples over the RX_DATA bus
However, for better throughput, connect both I & Q samples to FPGA
A_+3.3V
C41 100nF;0603
U5
TMP36FSZ
Temperature Sensor
R22 0R;0603
C39 C-OPEN;0603
C40 C-OPEN;0603
Caps for noise suppression when measuring temperature
Michael J. Yoha
Mobile Satellite Services
18221A Flower Hill Way
Gaithersburg, MD 20879
Title
COM-1200 / ANALOG RF FRONT END
Size C
Document Number Y03009
Rev 4
Date: Monday, October 23, 2006
Sheet 2 of 9



DIGITAL INPUT
LEFT
CONNECTOR

DIGITAL OUTPUT
RIGHT CONNECTOR

4,5 INPUT_[0-30]

5 M&C[2-5]

5 OUTPUT_[0-30]

5 JTAG[1-4]

Michael J. Yoha

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COM-1200 / DIGITAL CONNECTOR

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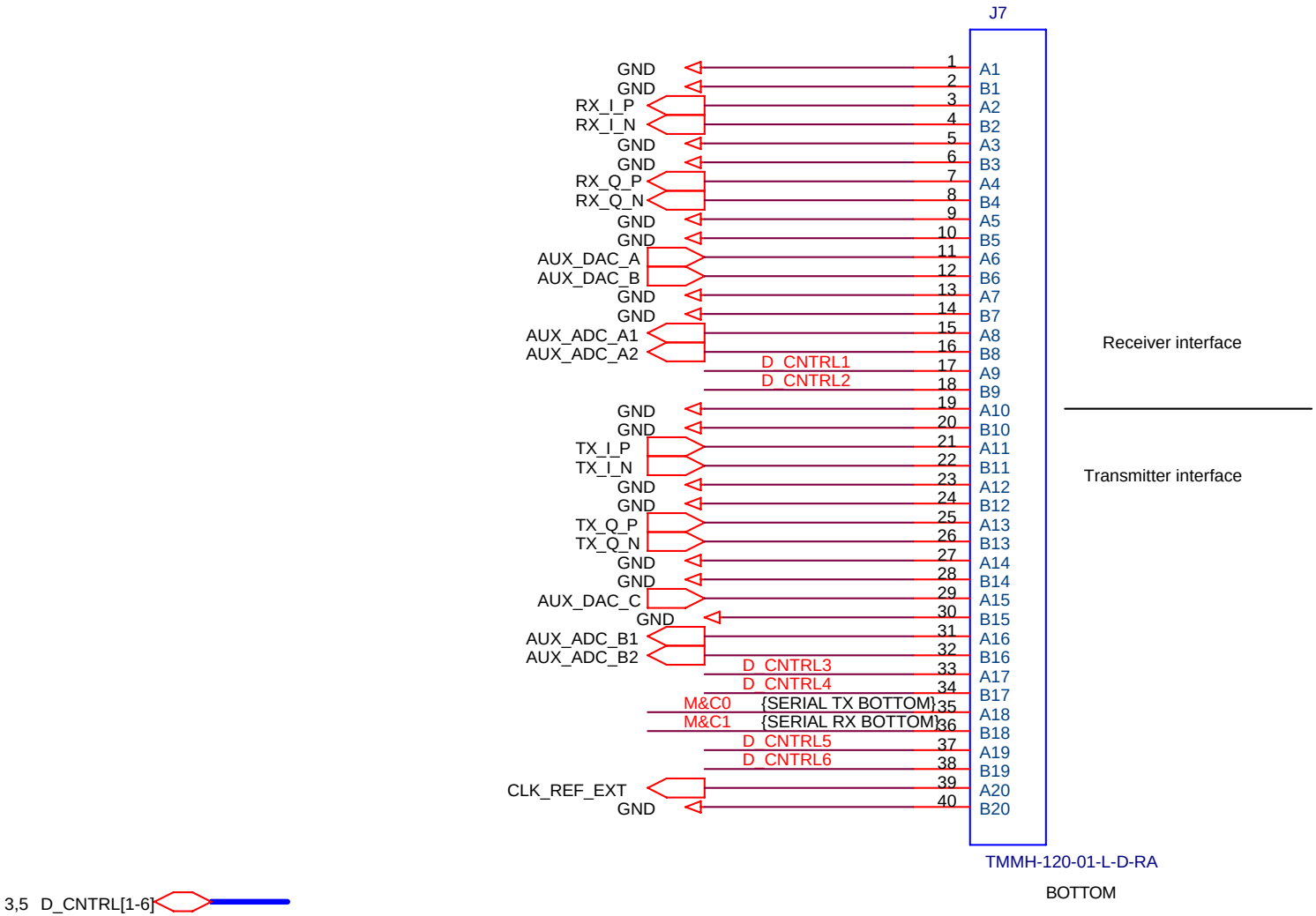

3,5 D_CNTRL[1-6]

5 M&C[0-1]

M&C0 {SERIAL TX BOTTOM}
M&C1 {SERIAL RX BOTTOM}

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COM-1200 / CONNECTOR_TRANSCEIVER

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FOR LVDS CHANGE VOLTAGE OF:
INPUT BANK 7 to 2.5V
OUTPUT BANK 2 to 2.5V

USB INTERFACE

FPGA CONFIGURATION

uC INTERFACE

40 PIN DIGITAL INPUT - LEFT CONNECTOR

40 PIN DIGITAL OUTPUT - RIGHT CONNECTOR

CARD EDGE CONNECTOR

JTAG header for Xilinx Parallel Cable IV Model DLC7

Please note: Serial link is NTTL, NOT RS232

Programming mode

Slave Parallel

Option to ground TCK for solder-capacity if not using JTAG

When Configured for LVDS:
Pin VBP tied to ground through a 180 ohm resistor
Pin VBN tied to VCC_O (3.3V) through a 180 ohm resistor

When Configured for LVDS:
Pin VBP tied to ground through a 180 ohm resistor
Pin VBN tied to VCC_O (3.3V) through a 180 ohm resistor

Pin A22 not connected on XC3S1500

Pin AA6 not connected on XC3S1500

Input pins are connected to low voltage differential signal pins on the FPGA at 2.5V. Designated by N or P on the FPGA pin number's.
OHM: Impedance controlled traces.

Output pins are connected to low voltage differential signal pins on the FPGA at 2.5V. Designated by N or P on the FPGA pin number's.
OHM: Impedance controlled traces.

FPGA

BANK 0
BANK 1
BANK 2
BANK 3
BANK 4
BANK 5
BANK 6
BANK 7

Constraints:

Pins	Voltage	Bank
Input	2.5V LVDS	0
USB	3.3V	1
Output	2.5V LVDS	2
Din/Dout	3.3V	4 & 5
JTAG	2.5V VCCAUX	N/A
PROG#	2.5V VCCAUX	N/A
CCLK	2.5V VCCAUX	N/A
DONE	2.5V VCCAUX	N/A
MODE	2.5V VCCAUX	N/A

Michael J. Yoho
Mobile Satellite Services
22214 Flower Hill Way
Gaithersburg, MD 20876

COM-1200 / FPGA

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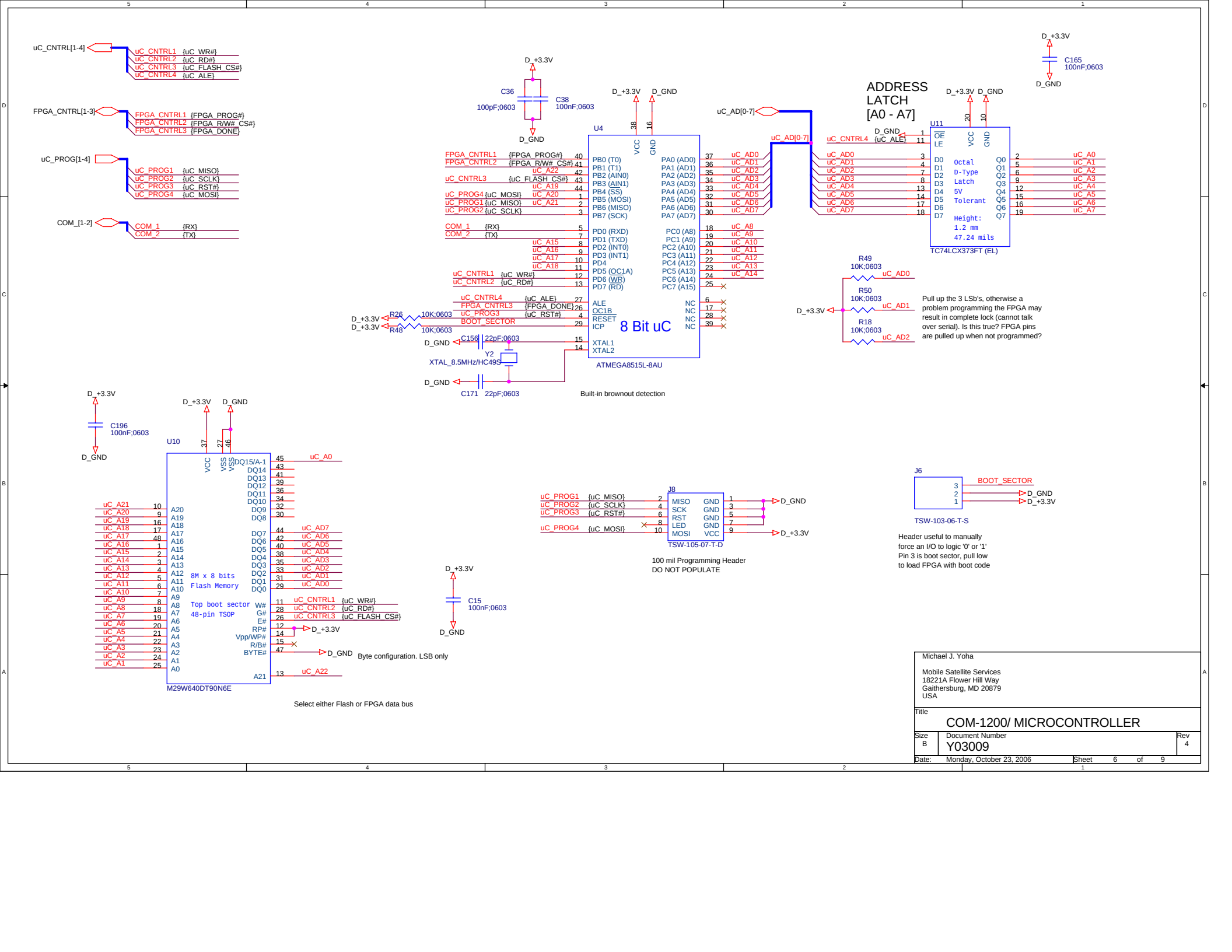
uC_CNTRL[1-4]
uC_CNTRL1 {uC_WR#}
uC_CNTRL2 {uC_RD#}
uC_CNTRL3 {uC_FLASH_CS#}
uC_CNTRL4 {uC_ALE}
FPGA_CNTRL[1-3]
FPGA_CNTRL1 {FPGA_PROG#}
FPGA_CNTRL2 {FPGA_R/W# CS#}
FPGA_CNTRL3 {FPGA_DONE}
uC_PROG[1-4]
uC_PROG1 {uC_MISO}
uC_PROG2 {uC_SCLK}
uC_PROG3 {uC_RST#}
uC_PROG4 {uC_MOSI}
COM_[1-2]
COM_1 {RX}
COM_2 {TX}
D_+3.3V
D_GND
C36
100pF;0603
C38
100nF;0603
U4
8 Bit uC
ATMEGA8515L-8AU
Built-in brownout detection
R26
R48
10K;0603
C156
22pF;0603
Y2
XTAL_8.5MHz/HC49S
C171
22pF;0603
ADDRESS
LATCH
[A0 - A7]
U11
TC74LCX373FT (EL)
C165
100nF;0603
R49
R50
R18
10K;0603
Pull up the 3 LSb's, otherwise a problem programming the FPGA may result in complete lock (cannot talk over serial). Is this true? FPGA pins are pulled up when not programmed?
C196
100nF;0603
U10
M29W640DT90N6E
8M x 8 bits
Flash Memory
Top boot sector
48-pin TSOP
Byte configuration. LSB only
Select either Flash or FPGA data bus
C15
100nF;0603
J8
TSW-105-07-T-D
100 mil Programming Header
DO NOT POPULATE
J6
TSW-103-06-T-S
BOOT_SECTOR
Header useful to manually force an I/O to logic '0' or '1'
Pin 3 is boot sector, pull low to load FPGA with boot code
Michael J. Yoha
Mobile Satellite Services
18221A Flower Hill Way
Gaithersburg, MD 20879
USA
Title
COM-1200/ MICROCONTROLLER
Size B
Document Number Y03009
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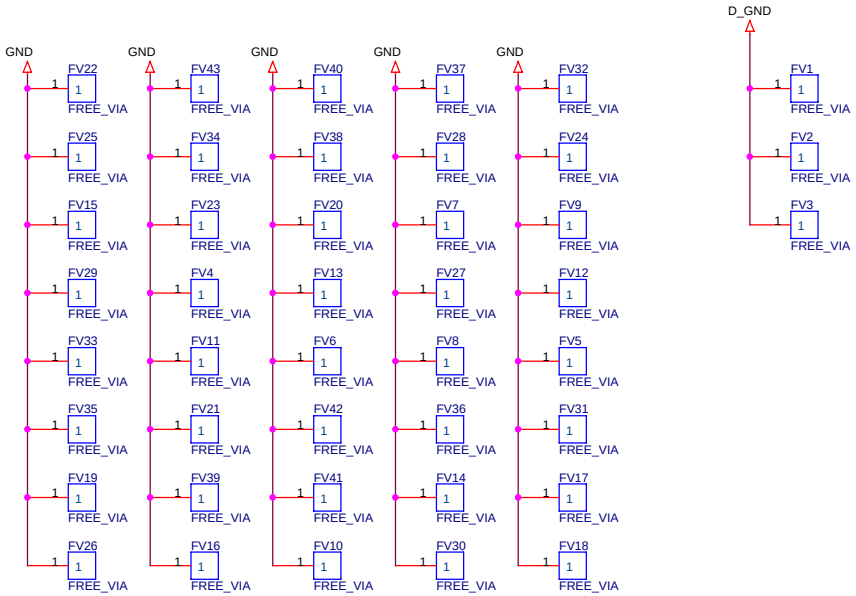

Michael J. Yoha

Mobile Satellite Services
18221A Flower Hill Way
Gaithersburg, MD 20879
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COM-1200 / LAYOUT

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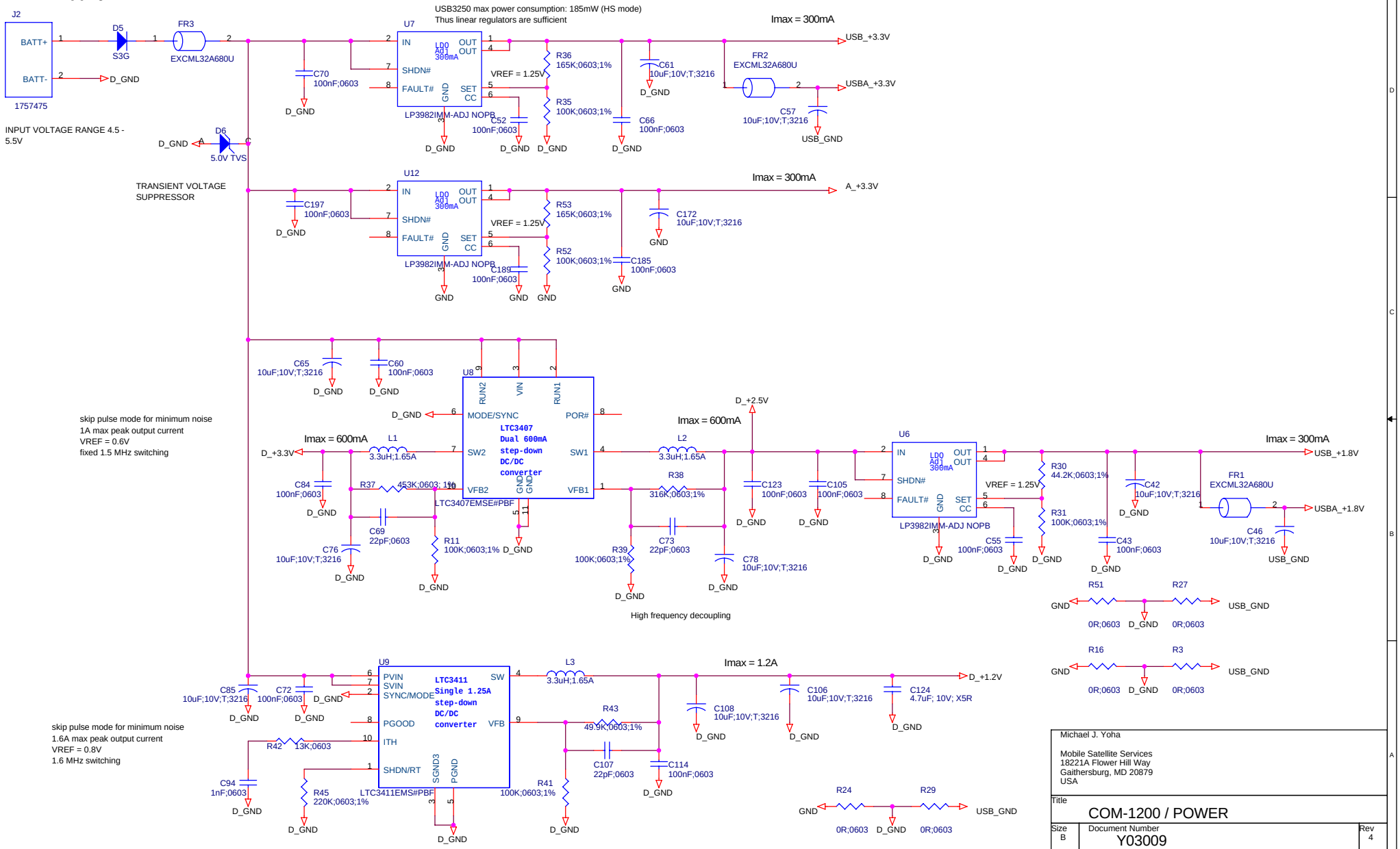
+5 V Supply



Michael J. Yoha

Mobile Satellite Services
18221A Flower Hill Way
Gaithersburg, MD 20879
USA

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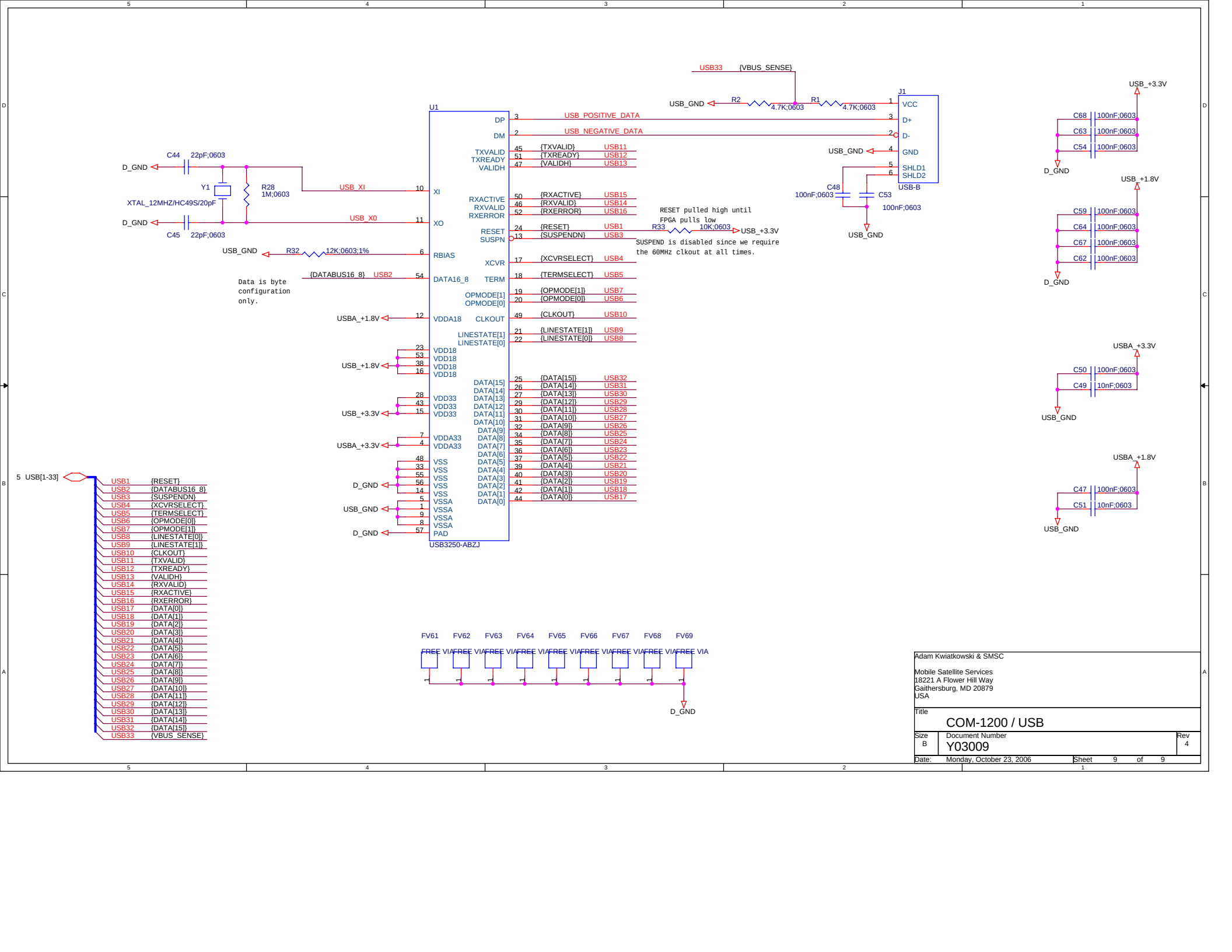

Adam Kwiatkowski & SMSC

Mobile Satellite Services
18221 A Flower Hill Way
Gaithersburg, MD 20879
USA

Title: COM-1200 / USB

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