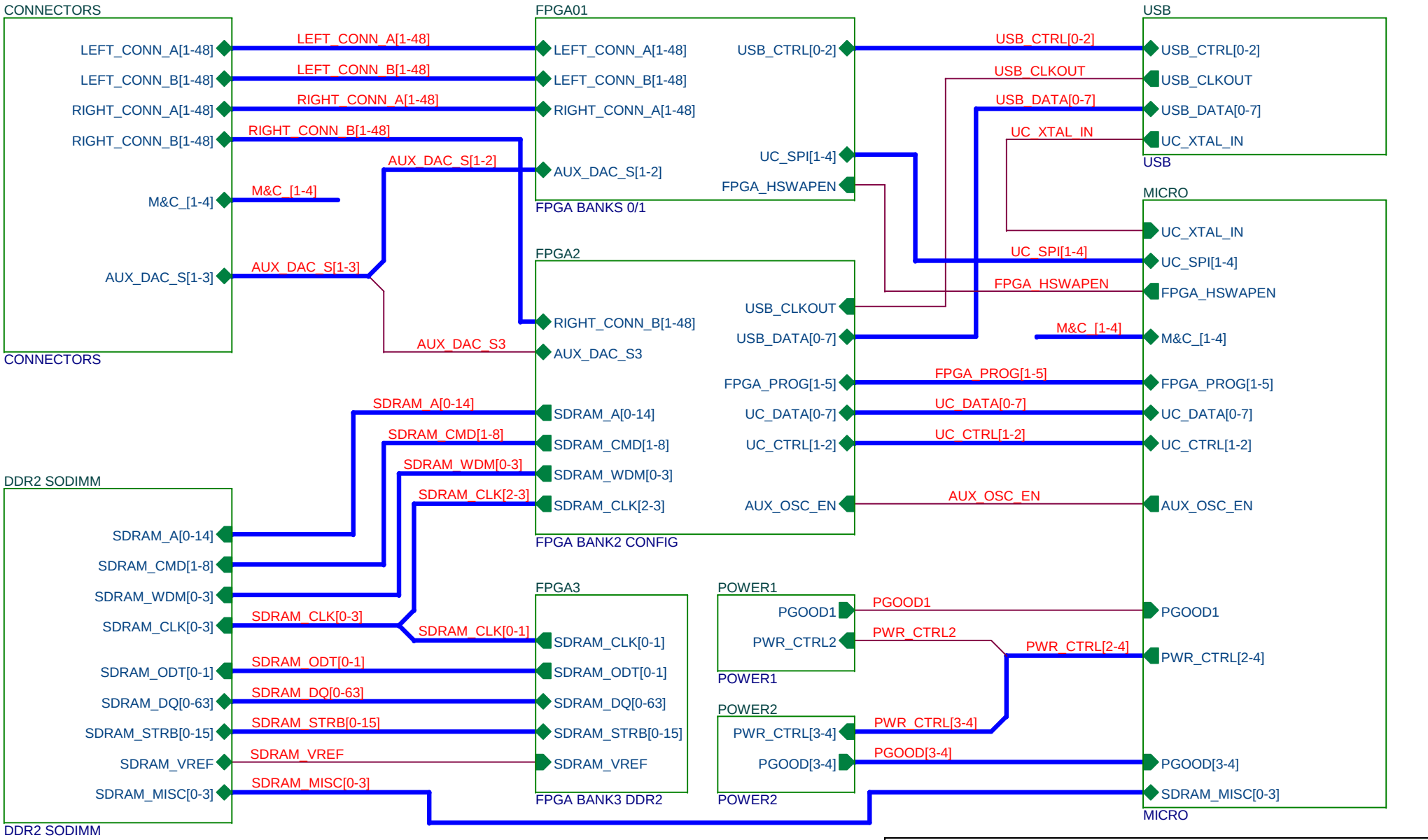

TABLE OF CONTENTS

General Layout Notes:
- use c0603 for all 0603
- use RC0402 for all 0402
- Label all TPs' names on SST

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Title: COM-1500 / MAIN

Size	Document Number	Rev
A	Y10008	1

Date: Friday, February 25, 2011 Sheet 1 of 10

HIGH-SPEED LVDS I/Os

LEFT_CONN_A[1-48]
LEFT_CONN_B[1-48]
RIGHT_CONN_A[1-48]
RIGHT_CONN_B[1-48]

MONITORING & CONTROL

M&C_[1-4]

M&C_1	{LEFT_RX}
M&C_2	{LEFT_TX}
M&C_3	{RIGHT_RX}
M&C_4	{RIGHT_TX}

Left Side Connector

J6 — 98-PIN STRADDLE MOUNT CONNECTOR — NWE49DHRN-T941

PCB TOP SIDE			PCB BOTTOM SIDE		
LEFT_CONN_A1	{LA1N}	1	50	LEFT_CONN_B1	{LB1N}
LEFT_CONN_A2	{LA1P}	2	51	LEFT_CONN_B2	{LB1P}
LEFT_CONN_A3	{LA2N}	3	52	LEFT_CONN_B3	{LB2N}
LEFT_CONN_A4	{LA2P}	4	53	LEFT_CONN_B4	{LB2P}
LEFT_CONN_A5	{LA3N}	5	54		D_GND
LEFT_CONN_A6	{LA3P}	6	55	LEFT_CONN_B6	{LB3N}
LEFT_CONN_A7	{LA4N}	7	56	LEFT_CONN_B7	{LB3P}
LEFT_CONN_A8	{LA4P}	8	57	LEFT_CONN_B8	{LB4N}
LEFT_CONN_A9	{LA5N}	9	58	LEFT_CONN_B9	{LB4P}
LEFT_CONN_A10	{LA5P}	10	59	LEFT_CONN_B10	{LB5N}
LEFT_CONN_A11	{LA6N}	11	60	LEFT_CONN_B11	{LB5P}
LEFT_CONN_A12	{LA6P}	12	61	LEFT_CONN_B12	{LB6N}
LEFT_CONN_A13	{LA7N}	13	62	LEFT_CONN_B13	{LB6P}
LEFT_CONN_A14	{LA7P}	14	63	LEFT_CONN_B14	{LB7N}
LEFT_CONN_A15	{LA8N}	15	64	LEFT_CONN_B15	{LB7P}
LEFT_CONN_A16	{LA8P}	16	65	LEFT_CONN_B16	{LB8N}
LEFT_CONN_A17	{LA9N}	17	66	LEFT_CONN_B17	{LB8P}
LEFT_CONN_A18	{LA9P}	18	67	LEFT_CONN_B18	{LB9N}
LEFT_CONN_A19	{LA10N}	19	68	LEFT_CONN_B19	{LB9P}
LEFT_CONN_A20	{LA10P}	20	69		D_GND
LEFT_CONN_A21	{LA11N}	21	70	LEFT_CONN_B21	{LB10N}
LEFT_CONN_A22	{LA11P}	22	71	LEFT_CONN_B22	{LB10P}
LEFT_CONN_A23	{LA12N}	23	72	LEFT_CONN_B23	{LB11N}
LEFT_CONN_A24	{LA12P}	24	73	LEFT_CONN_B24	{LB11P}
LEFT_CONN_A25	{LA13N}	25	74	LEFT_CONN_B25	{LB12N}
LEFT_CONN_A26	{LA13P}	26	75	LEFT_CONN_B26	{LB12P}
LEFT_CONN_A27	{LA14N}	27	76	LEFT_CONN_B27	{LB13N}
LEFT_CONN_A28	{LA14P}	28	77	LEFT_CONN_B28	{LB13P}
LEFT_CONN_A29	{LA15N}	29	78	LEFT_CONN_B29	{LB14N}
LEFT_CONN_A30	{LA15P}	30	79	LEFT_CONN_B30	{LB14P}
LEFT_CONN_A31	{LA16N}	31	80		D_GND
LEFT_CONN_A32	{LA16P}	32	81	LEFT_CONN_B32	{LB15N}
LEFT_CONN_A33	{LA17N}	33	82	LEFT_CONN_B33	{LB15P}
LEFT_CONN_A34	{LA17P}	34	83	LEFT_CONN_B34	{LB16N}
LEFT_CONN_A35	{LA18N}	35	84	LEFT_CONN_B35	{LB16P}
LEFT_CONN_A36	{LA18P}	36	85	LEFT_CONN_B36	{LB17N}
LEFT_CONN_A37	{LA19N}	37	86	LEFT_CONN_B37	{LB17P}
LEFT_CONN_A38	{LA19P}	38	87	LEFT_CONN_B38	{LB18N}
LEFT_CONN_A39	{LA20N}	39	88	LEFT_CONN_B39	{LB18P}
LEFT_CONN_A40	{LA20P}	40	89	LEFT_CONN_B40	{LB19N}
LEFT_CONN_A41	{LA21N}	41	90	LEFT_CONN_B41	{LB19P}
LEFT_CONN_A42	{LA21P}	42	91		D_GND
LEFT_CONN_A43	{LA22N}	43	92	LEFT_CONN_B43	{LB20N}
LEFT_CONN_A44	{LA22P}	44	93	LEFT_CONN_B44	{LB20P}
LEFT_CONN_A45	{LA23N}	45	94	LEFT_CONN_B45	{LB21N}
LEFT_CONN_A46	{LA23P}	46	95	LEFT_CONN_B46	{LB21P}
LEFT_CONN_A47	{LA24N}	47	96	LEFT_CONN_B47	{LB22N}
LEFT_CONN_A48	{LA24P}	48	97	LEFT_CONN_B48	{LB22P}
M&C_1	{LEFT_RX}	49	98	M&C_2	{LEFT_TX}

{LA20 through 24 available only with option -B. LX150)

Layout Note:
Place large ground vias near the connectors' ground pins

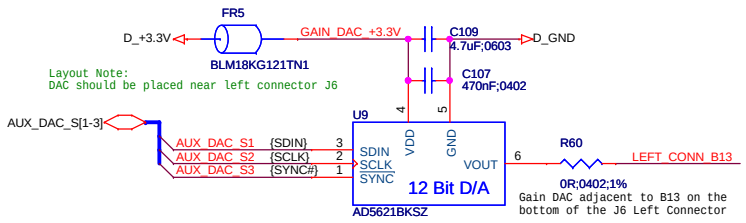
Right Side Connector

J9 — 98-PIN STRADDLE MOUNT CONNECTOR — NWE49DHRN-T941

PCB TOP SIDE			PCB BOTTOM SIDE		
RIGHT_CONN_A1	{RA1N}	50	1	RIGHT_CONN_B1	{RB1N}
RIGHT_CONN_A2	{RA1P}	51	2	RIGHT_CONN_B2	{RB1P}
RIGHT_CONN_A3	{RA2N}	52	3	RIGHT_CONN_B3	{RB2N}
RIGHT_CONN_A4	{RA2P}	53	4	RIGHT_CONN_B4	{RB2P}
RIGHT_CONN_A5	{RA3N}	54	5		D_GND
RIGHT_CONN_A6	{RA3P}	55	6	RIGHT_CONN_B6	{RB3N}
RIGHT_CONN_A7	{RA4N}	56	7	RIGHT_CONN_B7	{RB3P}
RIGHT_CONN_A8	{RA4P}	57	8	RIGHT_CONN_B8	{RB4N}
RIGHT_CONN_A9	{RA5N}	58	9	RIGHT_CONN_B9	{RB4P}
RIGHT_CONN_A10	{RA5P}	59	10	RIGHT_CONN_B10	{RB5N}
RIGHT_CONN_A11	{RA6N}	60	11	RIGHT_CONN_B11	{RB5P}
RIGHT_CONN_A12	{RA6P}	61	12	RIGHT_CONN_B12	{RB6N}
RIGHT_CONN_A13	{RA7N}	62	13	RIGHT_CONN_B13	{RB6P}
RIGHT_CONN_A14	{RA7P}	63	14	RIGHT_CONN_B14	{RB7N}
RIGHT_CONN_A15	{RA8N}	64	15	RIGHT_CONN_B15	{RB7P}
RIGHT_CONN_A16	{RA8P}	65	16	RIGHT_CONN_B16	{RB8N}
RIGHT_CONN_A17	{RA9N}	66	17	RIGHT_CONN_B17	{RB8P}
RIGHT_CONN_A18	{RA9P}	67	18	RIGHT_CONN_B18	{RB9N}
RIGHT_CONN_A19	{RA10N}	68	19	RIGHT_CONN_B19	{RB9P}
RIGHT_CONN_A20	{RA10P}	69	20		D_GND
RIGHT_CONN_A21	{RA11N}	70	21	RIGHT_CONN_B21	{RB10N}
RIGHT_CONN_A22	{RA11P}	71	22	RIGHT_CONN_B22	{RB10P}
RIGHT_CONN_A23	{RA12N}	72	23	RIGHT_CONN_B23	{RB11N}
RIGHT_CONN_A24	{RA12P}	73	24	RIGHT_CONN_B24	{RB11P}
RIGHT_CONN_A25	{RA13N}	74	25	RIGHT_CONN_B25	{RB12N}
RIGHT_CONN_A26	{RA13P}	75	26	RIGHT_CONN_B26	{RB12P}
RIGHT_CONN_A27	{RA14N}	76	27	RIGHT_CONN_B27	{RB13N}
RIGHT_CONN_A28	{RA14P}	77	28	RIGHT_CONN_B28	{RB13P}
RIGHT_CONN_A29	{RA15N}	78	29	RIGHT_CONN_B29	{RB14N}
RIGHT_CONN_A30	{RA15P}	79	30	RIGHT_CONN_B30	{RB14P}
RIGHT_CONN_A31	{RA16N}	80	31		D_GND
RIGHT_CONN_A32	{RA16P}	81	32	RIGHT_CONN_B32	{RB15N}
RIGHT_CONN_A33	{RA17N}	82	33	RIGHT_CONN_B33	{RB15P}
RIGHT_CONN_A34	{RA17P}	83	34	RIGHT_CONN_B34	{RB16N}
RIGHT_CONN_A35	{RA18N}	84	35	RIGHT_CONN_B35	{RB16P}
RIGHT_CONN_A36	{RA18P}	85	36	RIGHT_CONN_B36	{RB17N}
RIGHT_CONN_A37	{RA19N}	86	37	RIGHT_CONN_B37	{RB17P}
RIGHT_CONN_A38	{RA19P}	87	38	RIGHT_CONN_B38	{RB18N}
RIGHT_CONN_A39	{RA20N}	88	39	RIGHT_CONN_B39	{RB18P}
RIGHT_CONN_A40	{RA20P}	89	40	RIGHT_CONN_B40	{RB19N}
RIGHT_CONN_A41	{RA21N}	90	41	RIGHT_CONN_B41	{RB19P}
RIGHT_CONN_A42	{RA21P}	91	42		D_GND
RIGHT_CONN_A43	{RA22N}	92	43	RIGHT_CONN_B43	{RB20N}
RIGHT_CONN_A44	{RA22P}	93	44	RIGHT_CONN_B44	{RB20P}
RIGHT_CONN_A45	{RA23N}	94	45	RIGHT_CONN_B45	{RB21N}
RIGHT_CONN_A46	{RA23P}	95	46	RIGHT_CONN_B46	{RB21P}
RIGHT_CONN_A47	{RA24N}	96	47	RIGHT_CONN_B47	{RB22N}
RIGHT_CONN_A48	{RA24P}	97	48	RIGHT_CONN_B48	{RB22P}
M&C_4	{RIGHT_TX}	98	49	M&C_3	{RIGHT_RX}

Note to User:
'A' NETS are always on the top side physically of the PCB and 'B' on the bottom, contrary to the Right side connector's pin (not net) names.

GAIN CONTROL DAC



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Title: COM-1500 / CONNECTORS

Size	Document Number	Rev
B	Y10008	1

Date: Friday, February 25, 2011 Sheet 2 of 10

DDR2-SDRAM

Clock Enables and ODT signals must remain LOW during initialization => FPGA HSWAP_EN must be enabled

Layout note: split to CK0/CK1 pins into two equal-length branches near FPGA. Place 100 Ohm and 5pF differential termination at the split. Ref: Micron TN4720 App Note

3 SDRAM_A[0-14]
3 SDRAM_STRB[0-15]
3 SDRAM_CMD[1-8]
3 SDRAM_ODT[0-1]
3 SDRAM_WDM[0-3]
3 SDRAM_CLK[0-3]

Unregistered dual-rank DIMMs use both CK0/CK1 but not enough FPGA I/Os.

3 SDRAM_MISC[0-3]
SODIMM presence detect

Termination Resistors

Word (not byte) data mask. Write to a given 16-bit word is inhibited when high (masked).

Second part of the resistor divider to lower the 3.3V signals from the FPGA to 1.8V.

Layout note: Place 59Rs close to SODIMM socket. Replace with resistor array if it simplies trace routing.

Differential Data Strobe (DQS) traces routed close and inline with corresponding data byte (DQ) signals.

Two ODTs for rank-by-rank control

R66 4.7K;0402;1%
R61 4.7K;0402;1%

D_+1.8V
SDRAM_VREF
D_GND

J8

SODIMM 200P DDR2 SOCKET

Clocks: CK0, CK0#, CKE0, CK1, CK1#, CKE1/NC
Command: S0, S1/NC, RAS, CAS, WE, BA0, BA1, BA2/NC
Data Mask: DM0, DM1, DM2, DM3, DM4, DM5, DM6, DM7
Address: A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10/AP, A11, A12, A13/NC, A14/NC, A15/NC
Data Strobe: DQS0, DQS0#, DQS1, DQS1#, DQS2, DQS2#, DQS3, DQS3#, DQS4, DQS4#, DQS5, DQS5#, DQS6, DQS6#, DQS7, DQS7#
Serial Presence-Detect: SCL, SDA, SA0, SA1
On Die Termination: ODT0, ODT1/NC
TEST/NC, NC1, NC2, NC3, NC4

Data Byte 0: DQ0–DQ7
Data Byte 1: DQ8–DQ15
Data Byte 2: DQ16–DQ23
Data Byte 3: DQ24–DQ31
Data Byte 4: DQ32–DQ39
Data Byte 5: DQ40–DQ47
Data Byte 6: DQ48–DQ55
Data Byte 7: DQ56–DQ63

SDRAM_DQ[0-63] 3

SDRAM_VREF
Max Current Requirements:

FPGA Iref total = +/-150uA
SODIMM Iref = +/-32uA

Iref total = +/-182uA

R130 1K;0402;1%
R131 1K;0402;1%
C170 4.7uF;0603

C48 C34 C36 C42 C44 C49 C126 C111 C133 C143 C150 C110 470nF;0402

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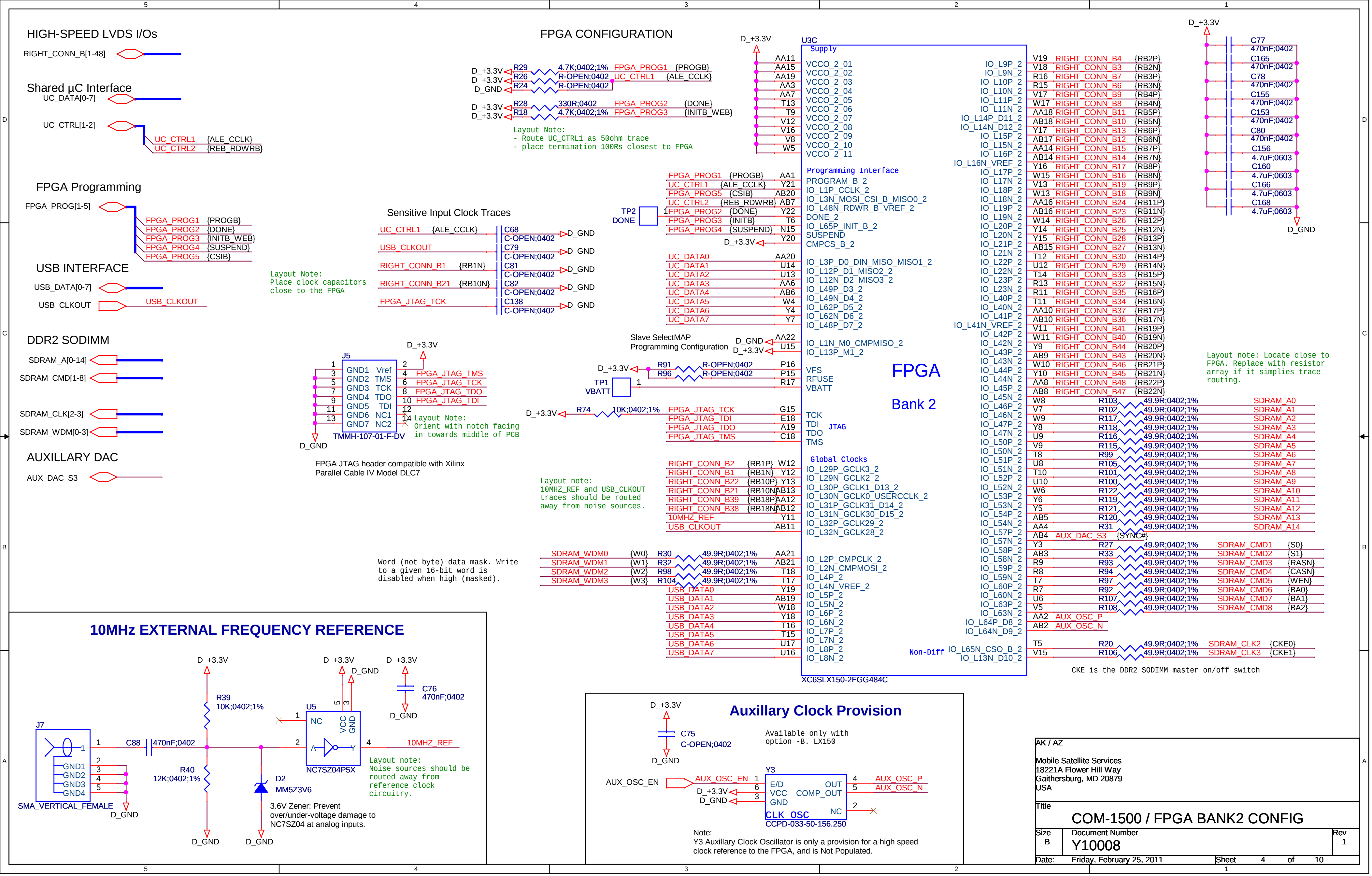
Title: COM-1500 / DDR2 SODIMM

Size: B
Document Number: Y10008
Rev: 1

Date: Monday, December 19, 2011
Sheet 3 of 10


HIGH-SPEED LVDS I/Os
RIGHT_CONN_B[1-48]
Shared µC Interface
UC_DATA[0-7]
UC_CTRL[1-2]
UC_CTRL1 {ALE_CCLK}
UC_CTRL2 {REB_RDWRB}
FPGA Programming
FPGA_PROG[1-5]
FPGA_PROG1 {PROGB}
FPGA_PROG2 {DONE}
FPGA_PROG3 {INITB_WEB}
FPGA_PROG4 {SUSPEND}
FPGA_PROG5 {CSIB}
USB INTERFACE
USB_DATA[0-7]
USB_CLKOUT
DDR2 SODIMM
SDRAM_A[0-14]
SDRAM_CMD[1-8]
SDRAM_CLK[2-3]
SDRAM_WDM[0-3]
AUXILLARY DAC
AUX_DAC_S3
FPGA CONFIGURATION
R29 4.7K;0402;1% FPGA_PROG1 {PROGB}
R26 R-OPEN;0402 UC_CTRL1 {ALE_CCLK}
R24 R-OPEN;0402
R28 330R;0402 FPGA_PROG2 {DONE}
R18 4.7K;0402;1% FPGA_PROG3 {INITB_WEB}
Layout Note:
- Route UC_CTRL1 as 50ohm trace
- place termination 100Rs closest to FPGA
Sensitive Input Clock Traces
Layout Note:
Place clock capacitors
close to the FPGA
C68 C-OPEN;0402
C79 C-OPEN;0402
C81 C-OPEN;0402
C82 C-OPEN;0402
C138 C-OPEN;0402
J5
TMMH-107-01-F-DV
Layout Note:
Orient with notch facing
in towards middle of PCB
FPGA JTAG header compatible with Xilinx
Parallel Cable IV Model DLC7
Slave SelectMAP
Programming Configuration
Layout note:
10MHZ_REF and USB_CLKOUT
traces should be routed
away from noise sources.
Word (not byte) data mask. Write
to a given 16-bit word is
disabled when high (masked).
U3C
Supply
Programming Interface
JTAG
Global Clocks
FPGA
Bank 2
Non-Diff
XC6SLX150-2FGG484C
Layout note: Locate close to
FPGA. Replace with resistor
array if it simplies trace
routing.
CKE is the DDR2 SODIMM master on/off switch
10MHz EXTERNAL FREQUENCY REFERENCE
J7
SMA_VERTICAL_FEMALE
C88 470nF;0402
R39 10K;0402;1%
R40 12K;0402;1%
D2 MM5Z3V6
3.6V Zener: Prevent
over/under-voltage damage to
NC7SZ04 at analog inputs.
U5 NC7SZ04P5X
C76 470nF;0402
10MHZ_REF
Layout note:
Noise sources should be
routed away from
reference clock
circuitry.
Auxillary Clock Provision
C75 C-OPEN;0402
Available only with
option -B. LX150
Y3
CCPD-033-50-156.250
AUX_OSC_EN
AUX_OSC_P
AUX_OSC_N
Note:
Y3 Auxillary Clock Oscillator is only a provision for a high speed
clock reference to the FPGA, and is Not Populated.
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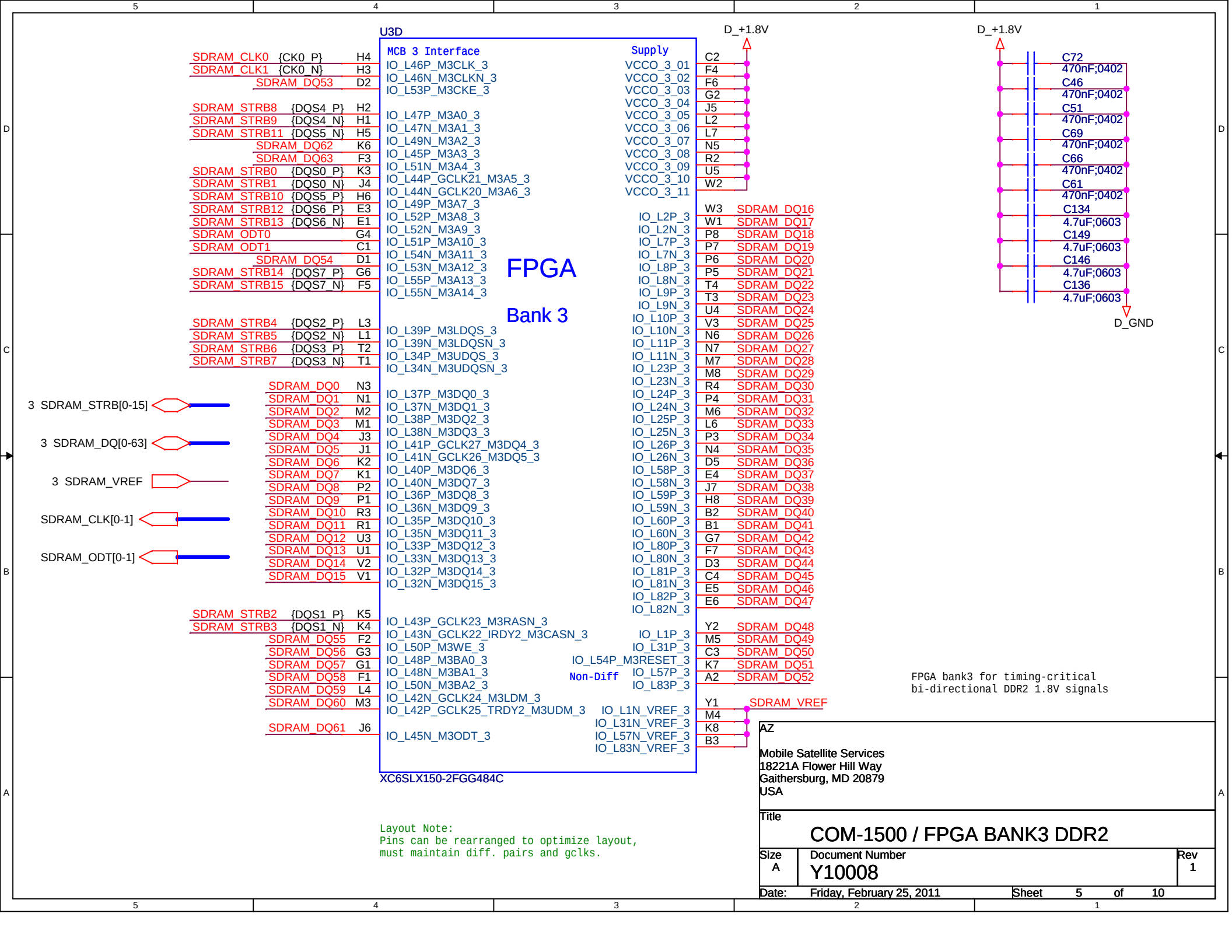
Mobile Satellite Services
18221A Flower Hill Way
Gaithersburg, MD 20879
USA
Title
COM-1500 / FPGA BANK2 CONFIG
Size B
Document Number Y10008
Rev 1
Date: Friday, February 25, 2011
Sheet 4 of 10


U3D
MCB 3 Interface
Supply
FPGA
Bank 3
XC6SLX150-2FGG484C
SDRAM_CLK0 {CK0_P} H4
SDRAM_CLK1 {CK0_N} H3
SDRAM_DQ53 D2
SDRAM_STRB8 {DQS4_P} H2
SDRAM_STRB9 {DQS4_N} H1
SDRAM_STRB11 {DQS5_N} H5
SDRAM_DQ62 K6
SDRAM_DQ63 F3
SDRAM_STRB0 {DQS0_P} K3
SDRAM_STRB1 {DQS0_N} J4
SDRAM_STRB10 {DQS5_P} H6
SDRAM_STRB12 {DQS6_P} E3
SDRAM_STRB13 {DQS6_N} E1
SDRAM_ODT0 G4
SDRAM_ODT1 C1
SDRAM_DQ54 D1
SDRAM_STRB14 {DQS7_P} G6
SDRAM_STRB15 {DQS7_N} F5
SDRAM_STRB4 {DQS2_P} L3
SDRAM_STRB5 {DQS2_N} L1
SDRAM_STRB6 {DQS3_P} T2
SDRAM_STRB7 {DQS3_N} T1
SDRAM_DQ0 N3
SDRAM_DQ1 N1
SDRAM_DQ2 M2
SDRAM_DQ3 M1
SDRAM_DQ4 J3
SDRAM_DQ5 J1
SDRAM_DQ6 K2
SDRAM_DQ7 K1
SDRAM_DQ8 P2
SDRAM_DQ9 P1
SDRAM_DQ10 R3
SDRAM_DQ11 R1
SDRAM_DQ12 U3
SDRAM_DQ13 U1
SDRAM_DQ14 V2
SDRAM_DQ15 V1
SDRAM_STRB2 {DQS1_P} K5
SDRAM_STRB3 {DQS1_N} K4
SDRAM_DQ55 F2
SDRAM_DQ56 G3
SDRAM_DQ57 G1
SDRAM_DQ58 F1
SDRAM_DQ59 L4
SDRAM_DQ60 M3
SDRAM_DQ61 J6
IO_L46P_M3CLK_3
IO_L46N_M3CLKN_3
IO_L53P_M3CKE_3
IO_L47P_M3A0_3
IO_L47N_M3A1_3
IO_L49N_M3A2_3
IO_L45P_M3A3_3
IO_L51N_M3A4_3
IO_L44P_GCLK21_M3A5_3
IO_L44N_GCLK20_M3A6_3
IO_L49P_M3A7_3
IO_L52P_M3A8_3
IO_L52N_M3A9_3
IO_L51P_M3A10_3
IO_L54N_M3A11_3
IO_L53N_M3A12_3
IO_L55P_M3A13_3
IO_L55N_M3A14_3
IO_L39P_M3LDQS_3
IO_L39N_M3LDQSN_3
IO_L34P_M3UDQS_3
IO_L34N_M3UDQSN_3
IO_L37P_M3DQ0_3
IO_L37N_M3DQ1_3
IO_L38P_M3DQ2_3
IO_L38N_M3DQ3_3
IO_L41P_GCLK27_M3DQ4_3
IO_L41N_GCLK26_M3DQ5_3
IO_L40P_M3DQ6_3
IO_L40N_M3DQ7_3
IO_L36P_M3DQ8_3
IO_L36N_M3DQ9_3
IO_L35P_M3DQ10_3
IO_L35N_M3DQ11_3
IO_L33P_M3DQ12_3
IO_L33N_M3DQ13_3
IO_L32P_M3DQ14_3
IO_L32N_M3DQ15_3
IO_L43P_GCLK23_M3RASN_3
IO_L43N_GCLK22_IRDY2_M3CASN_3
IO_L50P_M3WE_3
IO_L48P_M3BA0_3
IO_L48N_M3BA1_3
IO_L50N_M3BA2_3
IO_L42N_GCLK24_M3LDM_3
IO_L42P_GCLK25_TRDY2_M3UDM_3
IO_L45N_M3ODT_3
VCCO_3_01 C2
VCCO_3_02 F4
VCCO_3_03 F6
VCCO_3_04 G2
VCCO_3_05 J5
VCCO_3_06 L2
VCCO_3_07 L7
VCCO_3_08 N5
VCCO_3_09 R2
VCCO_3_10 U5
VCCO_3_11 W2
IO_L2P_3 W3 SDRAM_DQ16
IO_L2N_3 W1 SDRAM_DQ17
IO_L7P_3 P8 SDRAM_DQ18
IO_L7N_3 P7 SDRAM_DQ19
IO_L8P_3 P6 SDRAM_DQ20
IO_L8N_3 P5 SDRAM_DQ21
IO_L9P_3 T4 SDRAM_DQ22
IO_L9N_3 T3 SDRAM_DQ23
IO_L10P_3 U4 SDRAM_DQ24
IO_L10N_3 V3 SDRAM_DQ25
IO_L11P_3 N6 SDRAM_DQ26
IO_L11N_3 N7 SDRAM_DQ27
IO_L23P_3 M7 SDRAM_DQ28
IO_L23N_3 M8 SDRAM_DQ29
IO_L24P_3 R4 SDRAM_DQ30
IO_L24N_3 P4 SDRAM_DQ31
IO_L25P_3 M6 SDRAM_DQ32
IO_L25N_3 L6 SDRAM_DQ33
IO_L26P_3 P3 SDRAM_DQ34
IO_L26N_3 N4 SDRAM_DQ35
IO_L58P_3 D5 SDRAM_DQ36
IO_L58N_3 E4 SDRAM_DQ37
IO_L59P_3 J7 SDRAM_DQ38
IO_L59N_3 H8 SDRAM_DQ39
IO_L60P_3 B2 SDRAM_DQ40
IO_L60N_3 B1 SDRAM_DQ41
IO_L80P_3 G7 SDRAM_DQ42
IO_L80N_3 F7 SDRAM_DQ43
IO_L81P_3 D3 SDRAM_DQ44
IO_L81N_3 C4 SDRAM_DQ45
IO_L82P_3 E5 SDRAM_DQ46
IO_L82N_3 E6 SDRAM_DQ47
IO_L1P_3 Y2 SDRAM_DQ48
IO_L31P_3 M5 SDRAM_DQ49
IO_L54P_M3RESET_3 C3 SDRAM_DQ50
IO_L57P_3 K7 SDRAM_DQ51
IO_L83P_3 A2 SDRAM_DQ52
Non-Diff
IO_L1N_VREF_3 Y1 SDRAM_VREF
IO_L31N_VREF_3 M4
IO_L57N_VREF_3 K8
IO_L83N_VREF_3 B3
3 SDRAM_STRB[0-15]
3 SDRAM_DQ[0-63]
3 SDRAM_VREF
SDRAM_CLK[0-1]
SDRAM_ODT[0-1]
D_+1.8V
D_+1.8V
C72 470nF;0402
C46 470nF;0402
C51 470nF;0402
C69 470nF;0402
C66 470nF;0402
C61 470nF;0402
C134 4.7uF;0603
C149 4.7uF;0603
C146 4.7uF;0603
C136 4.7uF;0603
D_GND
FPGA bank3 for timing-critical
bi-directional DDR2 1.8V signals
Layout Note:
Pins can be rearranged to optimize layout,
must maintain diff. pairs and gclks.
AZ
Mobile Satellite Services
18221A Flower Hill Way
Gaithersburg, MD 20879
USA
Title
COM-1500 / FPGA BANK3 DDR2
Size A
Document Number
Y10008
Rev 1
Date: Friday, February 25, 2011
Sheet 5 of 10

HIGH-SPEED LVDS I/Os

LEFT_CONN_A[1-48]

LEFT_CONN_B[1-48]

RIGHT_CONN_A[1-48]

Miscellaneous Digital I/O

USB_CTRL[0-2]

USB_CTRL0 {NXT}
USB_CTRL1 {DIR}
USB_CTRL2 {STP}

FPGA_HSWAPEN

FPGA_HSWAPEN

AUX_DAC_S[1-2]

AUX_DAC_S1 {SDIN}
AUX_DAC_S2 {SCLK}

High-speed SPI to ARM microcontroller

UC_SPI[1-4]

UC_SPI1 {SCK0}
UC_SPI2 {SSEL0}
UC_SPI3 {MISO0}
UC_SPI4 {MOSI0}

Layout Note:
R55 is a low priority
placement near the FPGA

D_GND — R55 R-OPEN;0402 — FPGA_HSWAPEN A3

U3A

USB_CTRL0	{NXT}	A4	IO_L1P_HSWAPEN_0
USB_CTRL2	{STP}	C5	IO_L1N_VREF_0
USB_CTRL1	{DIR}	A5	IO_L2P_0
LEFT_CONN_A4	{LA2P}	D6	IO_L2N_0
LEFT_CONN_A3	{LA2N}	C6	IO_L3P_0
LEFT_CONN_A6	{LA3P}	B6	IO_L3N_0
LEFT_CONN_A5	{LA3N}	A6	IO_L4P_0
LEFT_CONN_A8	{LA4P}	C7	IO_L4N_0
LEFT_CONN_A7	{LA4N}	A7	IO_L5P_0
LEFT_CONN_A10	{LA5P}	B8	IO_L5N_0
LEFT_CONN_A9	{LA5N}	A8	IO_L6P_0
LEFT_CONN_A12	{LA6P}	D9	IO_L6N_0
LEFT_CONN_A11	{LA6N}	C8	IO_L7P_0
LEFT_CONN_A14	{LA7P}	C9	IO_L7N_0
LEFT_CONN_A13	{LA7N}	A9	IO_L8P_0
LEFT_CONN_A40	{LA20P}	E8	IO_L8N_VREF_0
LEFT_CONN_A39	{LA20N}	F8	IO_L14P_0
LEFT_CONN_A42	{LA21P}	G8	IO_L14N_0
LEFT_CONN_A41	{LA21N}	F9	IO_L15P_0
LEFT_CONN_A44	{LA22P}	G9	IO_L15N_0
LEFT_CONN_A43	{LA22N}	H10	IO_L16P_0
LEFT_CONN_A46	{LA23P}	E10	IO_L16N_0
LEFT_CONN_A45	{LA23N}	F10	IO_L17P_0
LEFT_CONN_A48	{LA24P}	G11	IO_L17N_0
LEFT_CONN_A47	{LA24N}	H11	IO_L18P_0
LEFT_CONN_A16	{LA8P}	D7	IO_L18N_0
LEFT_CONN_A15	{LA8N}	D8	IO_L32P_0
LEFT_CONN_A18	{LA9P}	D10	IO_L32N_0
LEFT_CONN_A17	{LA9N}	C10	IO_L33P_0
			IO_L33N_0

Global Clocks

LEFT_CONN_A2	{LA1P}	B10	IO_L34P_GCLK19_0
LEFT_CONN_A1	{LA1N}	A10	IO_L34N_GCLK18_0
LEFT_CONN_A20	{LA10P}	C11	IO_L35P_GCLK17_0
LEFT_CONN_A19	{LA10N}	A11	IO_L35N_GCLK16_0
LEFT_CONN_B2	{LB1P}	D11	IO_L36P_GCLK15_0
LEFT_CONN_B1	{LB1N}	C12	IO_L36N_GCLK14_0
LEFT_CONN_A38	{LA19P}	B12	IO_L37P_GCLK13_0
LEFT_CONN_A37	{LA19N}	A12	IO_L37N_GCLK12_0

Supply

VCCO_0_01	B11	
VCCO_0_02	B15	
VCCO_0_03	B19	
VCCO_0_04	B4	
VCCO_0_05	B7	
VCCO_0_06	E13	
VCCO_0_07	E17	
VCCO_0_08	E9	
VCCO_0_09	G10	
VCCO_0_10	G14	

FPGA Bank 0

XC6SLX150-2FGG484C

LA20 through 24 available only with option -B. LX150

IO_L38P_0	C13	LEFT_CONN_A22	{LA11P}
IO_L38N_VREF_0	A13	LEFT_CONN_A21	{LA11N}
IO_L43P_0	E12	LEFT_CONN_B41	{LB19P}
IO_L43N_0	D12	LEFT_CONN_B40	{LB19N}
IO_L44P_0	H12	LEFT_CONN_B44	{LB20P}
IO_L44N_0	F12	LEFT_CONN_B43	{LB20N}
IO_L45P_0	F13	LEFT_CONN_B46	{LB21P}
IO_L45N_0	D13	LEFT_CONN_B45	{LB21N}
IO_L46P_0	H13	LEFT_CONN_B48	{LB22P}
IO_L46N_0	G13	LEFT_CONN_B47	{LB22N}
IO_L47P_0	E14	UC_SPI1	{SCK0}
IO_L47N_0	F15	UC_SPI2	{SSEL0}
IO_L48P_0	F14	UC_SPI3	{MISO0}
IO_L48N_0	H14	UC_SPI4	{MOSI0}
IO_L49P_0	D14	LEFT_CONN_A24	{LA12P}
IO_L49N_0	C14	LEFT_CONN_A23	{LA12N}
IO_L50P_0	B14	LEFT_CONN_A26	{LA13P}
IO_L50N_0	A14	LEFT_CONN_A25	{LA13N}
IO_L51P_0	C15	LEFT_CONN_A28	{LA14P}
IO_L51N_0	A15	LEFT_CONN_A27	{LA14N}
IO_L62P_0	D15	LEFT_CONN_A30	{LA15P}
IO_L62N_VREF_0	C16	LEFT_CONN_A29	{LA15N}
IO_L63P_SCP7_0	B16	LEFT_CONN_A32	{LA16P}
IO_L63N_SCP6_0	A16	LEFT_CONN_A31	{LA16N}
IO_L64P_SCP5_0	C17	LEFT_CONN_A34	{LA17P}
IO_L64N_SCP4_0	A17	LEFT_CONN_A33	{LA17N}
IO_L65P_SCP3_0	B18	LEFT_CONN_A36	{LA18P}
IO_L65N_SCP2_0	A18	LEFT_CONN_A35	{LA18N}
IO_L66P_SCP1_0	E16	LEFT_CONN_B4	{LB2P}
IO_L66N_SCP0_0	D17	LEFT_CONN_B3	{LB2N}

LB19P through UCSPI4 Available only with option -B. LX150

D_+3.3V

C128 470nF;0402
C127 470nF;0402
C43 470nF;0402
C47 470nF;0402
C50 470nF;0402
C130 4.7uF;0603
C132 4.7uF;0603
C113 4.7uF;0603

D_GND

Layout Note:
All labeled (P & N) connector nets are
100ohm Z matched LVDS differential pairs

U3B

LEFT_CONN_B7	{LB3P}	C19	IO_L1P_A25_1
LEFT_CONN_B6	{LB3N}	B20	IO_L1N_A24_VREF_1
LEFT_CONN_B9	{LB4P}	G16	IO_L9P_1
LEFT_CONN_B8	{LB4N}	G17	IO_L9N_1
LEFT_CONN_B11	{LB5P}	F16	IO_L10P_1
LEFT_CONN_B10	{LB5N}	F17	IO_L10N_1
LEFT_CONN_B13	{LB6P}	B21	IO_L19P_1
LEFT_CONN_B12	{LB6N}	B22	IO_L19N_1
LEFT_CONN_B15	{LB7P}	A20	IO_L20P_1
LEFT_CONN_B14	{LB7N}	A21	IO_L20N_1
LEFT_CONN_B17	{LB8P}	K16	IO_L21P_1
LEFT_CONN_B16	{LB8N}	J16	IO_L21N_1
LEFT_CONN_B19	{LB9P}	H16	IO_L28P_1
LEFT_CONN_B18	{LB9N}	H17	IO_L28N_VREF_1
LEFT_CONN_B24	{LB11P}	D19	IO_L29P_A23_M1A13_1
LEFT_CONN_B23	{LB11N}	D20	IO_L29N_A22_M1A14_1
LEFT_CONN_B26	{LB12P}	F18	IO_L30P_A21_M1RESET_1
LEFT_CONN_B25	{LB12N}	F19	IO_L30N_A20_M1A11_1
LEFT_CONN_B28	{LB13P}	D21	IO_L31P_A19_M1CKE_1
LEFT_CONN_B27	{LB13N}	D22	IO_L31N_A18_M1A12_1
LEFT_CONN_B30	{LB14P}	C20	IO_L32P_A17_M1A8_1
LEFT_CONN_B29	{LB14N}	C22	IO_L32N_A16_M1A9_1
LEFT_CONN_B33	{LB15P}	G19	IO_L33P_A15_M1A10_1
LEFT_CONN_B32	{LB15N}	F20	IO_L33N_A14_M1A4_1
LEFT_CONN_B35	{LB16P}	H19	IO_L34P_A13_M1WE_1
LEFT_CONN_B34	{LB16N}	H18	IO_L34N_A12_M1BA2_1
LEFT_CONN_B37	{LB17P}	E20	IO_L35P_A11_M1A7_1
LEFT_CONN_B36	{LB17N}	E22	IO_L35N_A10_M1A2_1
LEFT_CONN_B39	{LB18P}	J17	IO_L36P_A9_M1BA0_1
LEFT_CONN_B38	{LB18N}	K17	IO_L36N_A8_M1BA1_1
RIGHT_CONN_A4	{RA2P}	F21	IO_L37P_A7_M1A0_1
RIGHT_CONN_A3	{RA2N}	F22	IO_L37N_A6_M1A1_1
RIGHT_CONN_A6	{RA3P}	H20	IO_L38P_A5_M1CLK_1
RIGHT_CONN_A5	{RA3N}	J19	IO_L38N_A4_M1CLKN_1
RIGHT_CONN_A8	{RA4P}	G20	IO_L39P_M1A3_1
RIGHT_CONN_A7	{RA4N}	G22	IO_L39N_M1ODT_1
LEFT_CONN_B22	{LB10P}	K20	IO_L40P_GCLK11_M1A5_1
LEFT_CONN_B21	{LB10N}	K19	IO_L40N_GCLK10_M1A6_1
RIGHT_CONN_A2	{RA1P}	H21	IO_L41P_GCLK9_IRDY1_M1RASN_1
RIGHT_CONN_A1	{RA1N}	H22	IO_L41N_GCLK8_M1CASN_1
RIGHT_CONN_A20	{RA10P}	M20	IO_L42P_GCLK7_M1UDM_1
RIGHT_CONN_A19	{RA10N}	L19	IO_L42N_GCLK6_TRDY1_M1LDM_1
RIGHT_CONN_A38	{RA19P}	J20	IO_L43P_GCLK5_M1DQ4_1
RIGHT_CONN_A37	{RA19N}	J22	IO_L43N_GCLK4_M1DQ5_1
			IO_L44P_A3_M1DQ6_1
			IO_L44N_A2_M1DQ7_1
			IO_L45P_A1_M1LDQS_1
			IO_L45N_A0_M1LDQSN_1
			IO_L46P_FCS_B_M1DQ2_1
			IO_L46N_FOE_B_M1DQ3_1
			IO_L47P_FWE_B_M1DQ0_1
			IO_L47N_LDC_M1DQ1_1
			IO_L48P_HDC_M1DQ8_1
			IO_L48N_M1DQ9_1
			IO_L49P_M1DQ10_1
			IO_L49N_M1DQ11_1
			IO_L50P_M1UDQS_1
			IO_L50N_M1UDQSN_1
			IO_L51P_M1DQ12_1
			IO_L51N_M1DQ13_1
			IO_L52P_M1DQ14_1
			IO_L52N_M1DQ15_1
			IO_L53P_1
			IO_L53N_VREF_1
			IO_L58P_1
			IO_L58N_1
			IO_L59P_1
			IO_L59N_1
			IO_L60P_1
			IO_L60N_1
			IO_L61P_1
			IO_L61N_1
			IO_L70P_1
			IO_L70N_1
			IO_L71P_1
			IO_L71N_1
			IO_L72P_1
			IO_L72N_1
			IO_L73P_1
			IO_L73N_1
			IO_L74P_AWAKE_1
			IO_L74N_DOUT_BUSY_1

Global Clocks

Supply

VCCO_1_01	C21	
VCCO_1_02	E19	
VCCO_1_03	G21	
VCCO_1_04	J18	
VCCO_1_05	L16	
VCCO_1_06	L21	
VCCO_1_07	N18	
VCCO_1_08	R21	
VCCO_1_09	U18	
VCCO_1_10	W21	

FPGA Bank 1

XC6SLX150-2FGG484C

K21	RIGHT_CONN_A10	{RA5P}	
K22	RIGHT_CONN_A9	{RA5N}	
L20	RIGHT_CONN_A12	{RA6P}	
L22	RIGHT_CONN_A11	{RA6N}	
M21	RIGHT_CONN_A14	{RA7P}	
M22	RIGHT_CONN_A13	{RA7N}	
N20	RIGHT_CONN_A16	{RA8P}	
N22	RIGHT_CONN_A15	{RA8N}	
P21	RIGHT_CONN_A18	{RA9P}	
P22	RIGHT_CONN_A17	{RA9N}	
R20	RIGHT_CONN_A22	{RA11P}	
R22	RIGHT_CONN_A21	{RA11N}	
T21	RIGHT_CONN_A24	{RA12P}	
T22	RIGHT_CONN_A23	{RA12N}	
U20	RIGHT_CONN_A26	{RA13P}	
U22	RIGHT_CONN_A25	{RA13N}	
V21	RIGHT_CONN_A28	{RA14P}	
V22	RIGHT_CONN_A27	{RA14N}	
M19	RIGHT_CONN_A30	{RA15P}	
N19	RIGHT_CONN_A29	{RA15N}	
M16	RIGHT_CONN_A32	{RA16P}	
L15	RIGHT_CONN_A31	{RA16N}	
P19	RIGHT_CONN_A34	{RA17P}	
P20	RIGHT_CONN_A33	{RA17N}	
W20	RIGHT_CONN_A36	{RA18P}	
W22	RIGHT_CONN_A35	{RA18N}	
L17	RIGHT_CONN_A40	{RA20P}	
K18	RIGHT_CONN_A39	{RA20N}	
U19	RIGHT_CONN_A42	{RA21P}	
V20	RIGHT_CONN_A41	{RA21N}	
M17	RIGHT_CONN_A44	{RA22P}	
M18	RIGHT_CONN_A43	{RA22N}	
P17	RIGHT_CONN_A46	{RA23P}	
N16	RIGHT_CONN_A45	{RA23N}	
P18	RIGHT_CONN_A48	{RA24P}	
R19	RIGHT_CONN_A47	{RA24N}	
T19	AUX_DAC_S1	{SDIN}	
T20	AUX_DAC_S2	{SCLK}	

Sensitive Input Clock Traces

LEFT_CONN_A1	{LA1N}	C129	C-OPEN;0402 — D_GND
LEFT_CONN_A19	{LA10N}	C119	C-OPEN;0402 — D_GND
LEFT_CONN_B1	{LB1N}	C131	C-OPEN;0402 — D_GND
LEFT_CONN_B21	{LB10N}	C148	C-OPEN;0402 — D_GND
RIGHT_CONN_A1	{RA1N}	C52	C-OPEN;0402 — D_GND
RIGHT_CONN_A19	{RA10N}	C152	C-OPEN;0402 — D_GND

Layout Note:
Place all capacitors for the Sensitive Input
Clock Traces close to FPGA pins in such a way
as to minimize the impact on the layout of
labeled differential traces

D_+3.3V

C141 470nF;0402
C56 470nF;0402
C157 470nF;0402
C154 470nF;0402
C60 470nF;0402
C65 470nF;0402
C53 4.7uF;0603
C57 4.7uF;0603
C54 4.7uF;0603

D_GND

AK / AZ

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USA

Title: COM-1500 / FPGA BANKS 0/1

Size: B | Document Number: Y10008 | Rev: 1

Date: Friday, February 25, 2011 | Sheet 6 of 10

Shared µC Interface

UC_CTRL[1-2]
UC_CTRL1 {ALE_CCLK}
UC_CTRL2 {REB_RDWRB}
UC_DATA[0-7]

FPGA Programming

FPGA_PROG[1-5]
FPGA_PROG1 {PROGB}
FPGA_PROG2 {DONE}
FPGA_PROG3 {INITB}
FPGA_PROG4 {SUSPEND}
FPGA_PROG5 {CSIB}
FPGA_HSWAPEN
FPGA_HSWAPEN

Miscellaneous Digital I/O

M&C_[1-4]
M&C_1 {LEFT_RX}
M&C_2 {LEFT_TX}
M&C_3 {RIGHT_RX}
M&C_4 {RIGHT_TX}

Power Good Indicators

PGOOD1
PGOOD1 {ARM_+3.3V}
PGOOD[3-4]
PGOOD3 {D_+1.8V}
PGOOD4 {D_+1.2V}

PWR_CTRL[2-4]
PWR_CTRL2 {D_+3.3V}
PWR_CTRL3 {D_+1.8V}
PWR_CTRL4 {D_+1.2V}

AUX_OSC_EN
AUX_OSC_EN

DDR2 SDRAM presence detect

3 SDRAM_MISC[0-3]

High-speed SPI to FPGA

UC_SPI[1-4]

ARM_+3.3V
C108 10nF;0402
C32 10nF;0402
C33 470nF;0402
C27 470nF;0402
C14 470nF;0402
C19 470nF;0402
C16 4.7uF;0603
C98 4.7uF;0603
D_GND

ARM_+3.3V
R57 10R;0402
R59 10R;0402
D_GND
C104 470nF;0402
C103 4.7uF;0603
D_GND

JP1 - Flash Drive Access Mode Select Jumper

JP1 Jumper Position = Flash Drive Access Mode:
1-2 = USB Flash Drive
2-3 or NC = Standard Comblock Monitoring & Control
(NC = Jumper Not Connected in either position)

UC_FLASH_MODE
JP1
ARM_+3.3V
D_GND
TSW-103-07-F-S

Layout Note:
Add Power Source description on Silkscreen

J2: Developer's USB Port

- Microcontroller programming
- USB Flash Drive Device mode for FPGA Flash Programming (set JP1)
- Standard Comblock Monitoring and Control (using Comblock driver)
- May be connected simutaneously with Primary USB Port

ARM_+3.3V
R136 1.5K;0402
USB_CONNECTB
Q5
FDN306P
R4 1.5K;0402
D_GND
C9 4.7uF;0603
J2

Layout Note:
Place 4.7uF cap close to USB connector

USB_+5.0V
UC_USB_DM R6 33R;0402;1%
UC_USB_DP R5 33R;0402;1%
Layout Note:
Z match D+ & D- to 90 ohm diff

FR2
BLM18KG121TN1
C1 470nF;0402
C6 470nF;0402
C2 470nF;0402
C5 470nF;0402
D_GND
USB_MINI_AB_RECEPTACLE
VBUS
D-
D+
ID
GND
SHIELD1
SHIELD2
SHIELD3
SHIELD4

Layout Note:
USB connector should be in the same location as the COM1600 USB

U2 — ARM Cortex-M3 µC

VDD_1 21, VDD_2 42, VDD_3 56, VDD_4 77, VBAT 16, VDDREG_1 34, VDDREG_2 67, VDDA 8, VREFP 10, VREFN 12
VSS_1 24, VSS_2 33, VSS_3 43, VSS_4 57, VSS_5 66, VSS_6 78, VSSA 9

P0[0]/RD1/TXD3/SDA1
P0[1]/TD1/RXD3/SCL1
P0[2]/TXD0/AD0[7]
P0[3]/RXD0/AD0[6]
P0[6]/I2SRX_SDA/SSEL1/MAT2[0]
P0[7]/I2STX_CLK/SCK1/MAT2[1]
P0[8]/I2STX_WS/MISO1/MAT2[2]
P0[9]/I2STX_SDA/MOSI1/MAT2[3]
P0[10]/TXD2/SDA2/MAT3[0]
P0[11]/RXD2/SCL2/MAT3[1]
P0[15]/TXD1/SCK0/SCK
P0[16]/RXD1/SSEL0/SSEL
P0[17]/CTS1/MISO0/MISO
P0[18]/DCD1/MOSI0/MOSI
P0[22]/RTS1/TD1
P0[25]/AD0[2]/I2SRX_SDA/TXD3
P0[26]/AD0[3]/AOUT/RXD3

P1[30]/VBUS/AD0[4] 18
P0[30]/USB_D- 23
P0[29]/USB_D+ 22

P2[0]/PWM1[1]/TXD1
P2[1]/PWM1[2]/RXD1
P2[2]/PWM1[3]/CTS1/TRACEDATA[3]
P2[3]/PWM1[4]/DCD1/TRACEDATA[2]
P2[4]/PWM1[5]/DSR1/TRACEDATA[1]
P2[5]/PWM1[6]/DTR1/TRACEDATA[0]
P2[6]/PCAP1[0]/RI1/TRACECLK
P2[7]/RD2/RTS1
P2[8]/TD2/TXD2
P2[9]/USB_CONNECT/RXD2
P2[10]/EINT0/NMI

60 UC_DATA0
59 UC_DATA1
58 UC_DATA2
55 UC_DATA3
54 UC_DATA4
53 UC_DATA5
52 UC_DATA6
51 UC_DATA7
50 UC_CTRL1 {ALE_CCLK}
49 UC_CTRL2 {REB_RDWRB}
41 FPGA_PROG5 {CSIB} R8 10K;0402;1% ARM_+3.3V

FPGA_PROG1 {PROGB} 37
FPGA_PROG4 {SUSPEND} 38
M&C_2 {LEFT_TX} 79
M&C_1 {LEFT_RX} 80
FPGA_PROG2 {DONE} 64
FPGA_PROG3 {INITB} 63
PGOOD1 {ARM_+3.3V} 62
61
PGOOD3 {D_+1.8V} 39
PGOOD4 {D_+1.2V} 40
UC_SPI1 {SCK0} 47
UC_SPI2 {SSEL0} 48
UC_SPI3 {MISO0} 46
UC_SPI4 {MOSI0} 45
FPGA_HSWAPEN 44
UC_ADC1 7
UC_ANALOG 6

PWR_CTRL2 {D_+3.3V} 76
PWR_CTRL3 {D_+1.8V} 75
PWR_CTRL4 {D_+1.2V} 74

SDRAM_MISC0 {SCL} R15 49.9R;0402;1% 73
SDRAM_MISC1 {SDA} R14 49.9R;0402;1% 72
SDRAM_MISC2 {SA0} R13 49.9R;0402;1% 71
SDRAM_MISC3 {SA1} R12 49.9R;0402;1% 70
UC_CTRL3 {NAND_WEB} 69
USB_CONNECTB 25
AUX_OSC_EN 26
UC_PWM_u 27
UC_FLASH_MODE 28
NAND_R/BB2 29
NAND_R/BB 30
NAND_CEB2 31
NAND_WPB 32
NAND_CLE 35
NAND_CEB 36
UC_ADC2 17

P1[0]
P1[1]
P1[4]
P1[8]
P1[9]
P1[10]
P1[14]
P1[15]
P1[18]/USB_UP_LED/PWM1[1]/CAP1[0]
P1[19]/MC0A/USB_PPWR/CAP1[1]
P1[20]/MCI0/PWM1[2]/SCK0
P1[22]/MCOB0/USB_PWRD/MAT1[0]
P1[23]/MCI1/PWM1[4]/MISO0
P1[24]/MCI2/PWM1[5]/MOSI0
P1[25]/MCOA1/MAT1[1]
P1[26]/MCOB1/PWM1[6]/CAP0[0]
P1[28]/MCOA2/PCAP1[0]/MAT0[0]
P1[29]/MCOB2/PCAP1[1]/MAT0[1]
P1[31]/SCK1/AD0[5]

P4[28]/RX_MCLK/MAT2[0]/TXD3
P4[29]/TX_MCLK/MAT2[1]/RXD3

65 M&C_4 {RIGHT_TX}
68 M&C_3 {RIGHT_RX}

TRST 4 ARM_JTAG_TRSTB
TDI 2 ARM_JTAG_TDI
TMS/SWDIO 3 ARM_JTAG_TMS
TCK/SWDCLK 5 ARM_JTAG_TCK
TDO/SWO 1 ARM_JTAG_TDO
RESET 14 UC_RESET
RSTOUT 11

XTAL1 19 C20 100pF;0402 UC_XTAL_IN
XTAL2 20 C22 100pF;0402 D_GND
RTCX1 13 C28 12pF;0402 D_GND
RTCX2 15
RTCX circuit
Y2 AB26TRB-32.768KHZ
C29 33pF;0402 D_GND

LPC1759FBD80

System Reset Button

ARM_+3.3V
R45 10K;0402;1%
SW1
R44 510R;0402;1%
SW TACT-SPST-2/SM
C95 470nF;0402
D_GND

Note: System Reset Button
Pressing will reset the microcontroller and subsequently the FPGA and load Personality #1, as seen in Personalities window of Comblock Control Center

128MByte NAND

U8
D_+3.3V
D_GND
C97 470nF;0402
C112 470nF;0402
R52 10K;0402;1%

NC1 1, NC2 2, NC3 3, NC4 4, NC5 5, NC11 11, NC14 14, NC15 15, NC23 23, NC24 24, NC25 25, NC26 26, NC27 27, NC28 28, NC33 33, NC34 34, NC35 35, NC39 39, NC40 40, NC45 45, NC46 46, NC47 47, NC48 48, DNU1 20, DNU2 21, DNU3 22
VCC1 12, VCC2 37, VSS1 13, VSS2 36, VSS3 38

R/B 7 NAND_R/BB
RFU1 6 NAND_R/BB2
RE 8 UC_CTRL2 {REB_RDWRB}
CE 9 NAND_CEB
RFU2 10 NAND_CEB2
CLE 16 NAND_CLE
ALE 17 UC_CTRL1 {ALE_CCLK}
WE 18 UC_CTRL3 {NAND_WEB}
WP 19 NAND_WPB

I/O0 29 UC_DATA0
I/O1 30 UC_DATA1
I/O2 31 UC_DATA2
I/O3 32 UC_DATA3
I/O4 41 UC_DATA4
I/O5 42 UC_DATA5
I/O6 43 UC_DATA6
I/O7 44 UC_DATA7

x8 bit NAND Flash Memory
48-pin TSOP
MT29F1G08AACWP

Note:
NAND_CEB2 & NAND_R/BB2 nets are connected for future use with a potential 8Gb NAND part or larger.

ARM_+3.3V
C171 470nF;0402
D_GND

J10 — CARD EDGE CONNECTOR

MEC1-108-01-S-D-RA1-SL

M&C_1 {LEFT_RX} 3
JTAG7 {DE_B} 5
FPGA_PROG5 {CSIB} 9
ARM_JTAG_TRSTB 11
ARM_JTAG_TDI 13

R125 10K;0402;1%
R127 10K;0402;1%
R128 10K;0402;1%

M&C_2 {LEFT_TX} 4
UC_RESET {RSTB} 6 R38 R-OPEN;0402 ARM_JTAG_TRSTB
ARM_JTAG_TDO 8 R36 10K;0402;1% D_GND
ARM_JTAG_RTCK 10 R126 R-OPEN;0402 ARM_+3.3V
ARM_JTAG_TCK 12 R42 10K;0402;1% D_GND
ARM_JTAG_TMS 14 R129 10K;0402;1% ARM_+3.3V
R37 10K;0402;1% ARM_+3.3V

User Defined Analog/Digital µC I/O

Optional LPF for µC's PWM output

UC_PWM_u R7 0R;0402;1%
C13 C-OPEN;0402
D_GND

Layout Note:
LPF placement should be near micro

Layout Note:
Add SST Label for 3.3V and GND

J4
UC_ANALOG 1
UC_PWM 2
UC_ADC1 3
UC_ADC2 4
D_GND 5
UC_SPI1 {SCK0} 6
UC_SPI2 {SSEL0} 7
UC_SPI3 {MISO0} 8
UC_SPI4 {MOSI0} 9
ARM_+3.3V 10
D_GND 11
12
13
14
TMMH-107-01-F-DV
2mm Header

Note:
All user I/O pins of J4 can be configured as general purpose digital signals, interrupts or specialized signals as indicated by their respective net names. UC_ANALOG can be configured as an ADC input or DAC ouput. UC_TP[1-4] may be configured for a high speed SSP interface.

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Size: B
Document Number: Y10008
Rev: 1
Date: Monday, March 14, 2011
Sheet 7 of 10

+5V Supply 3A max

Green Terminal Block

OPERATIONAL RANGE: 4.75 - 5.5V

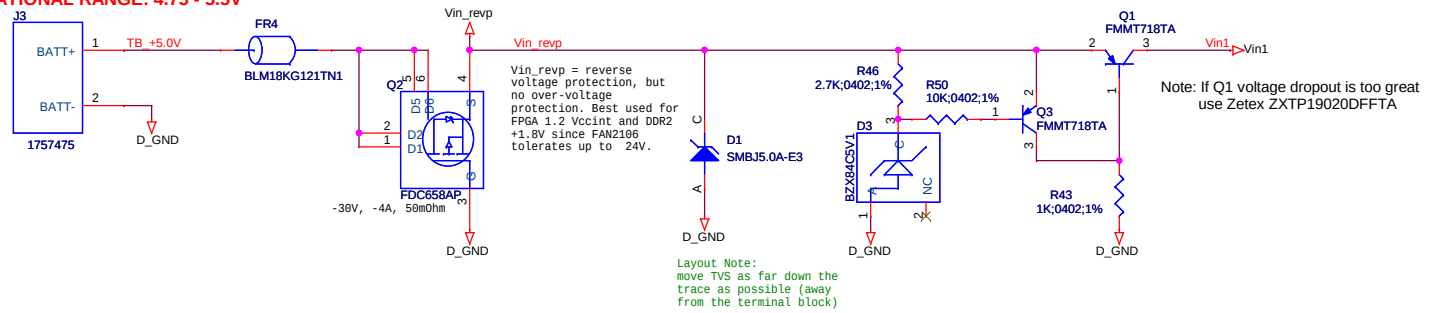
Filter

Reverse Voltage Protection

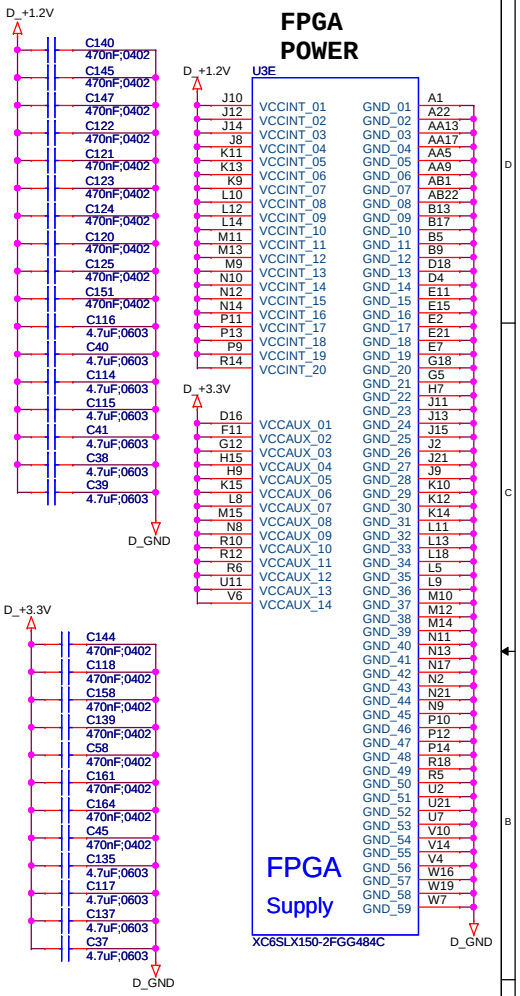
Transient Voltage Suppression

Over Voltage Protection (5.85V, 1.5A)

Layout Note:
FR4, Q1, Q2 & Q4 must be placed and routed for a high current throughput.



FPGA POWER



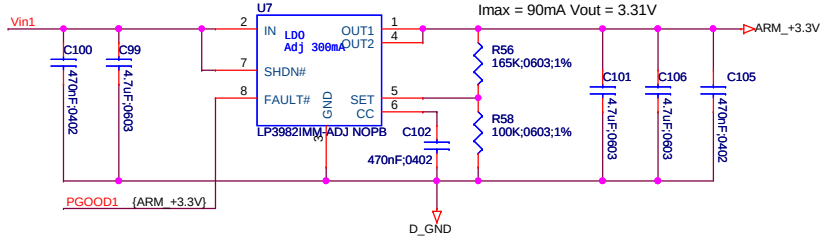
Main Power Supply Enable

PWR_CTRL2 — PWR_CTRL2 {D_+3.3V}

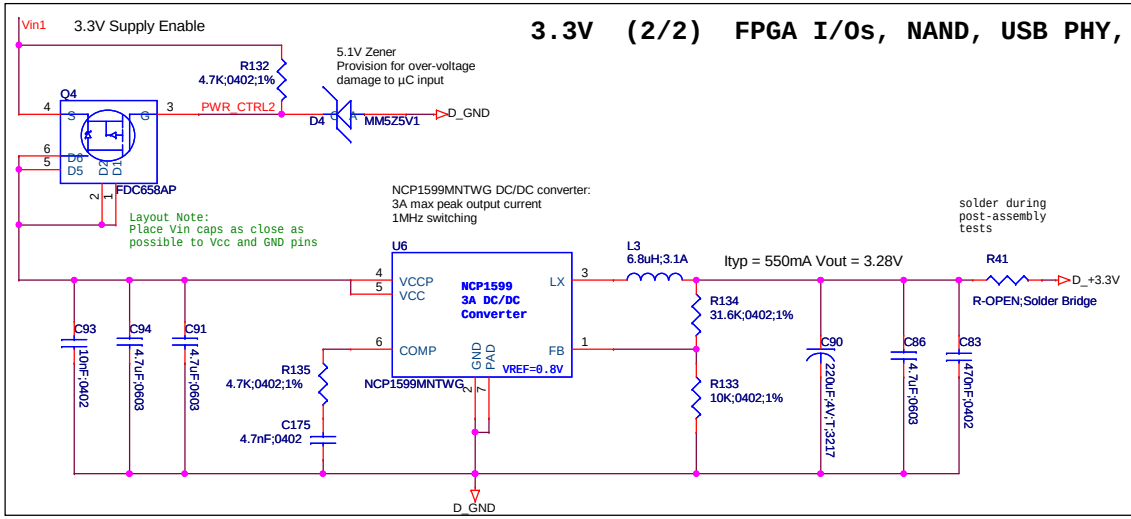
Power Good Indicator

PGOOD1 — PGOOD1 {ARM_+3.3V}

3.3V (1/2) Always ON



3.3V (2/2) FPGA I/Os, NAND, USB PHY, DAC



PCB Mounting Holes

H1 H2 H3 H4

Power Requirements

COMP	V	mA
FPGA	+3.3	300
MICRO	+3.3	90
NAND	+3.3	50
USB	+3.3	50
DAC	+3.3	60
DDDR2	+1.8	2835 (300 MHz)
FPGA	+1.2	5000 max

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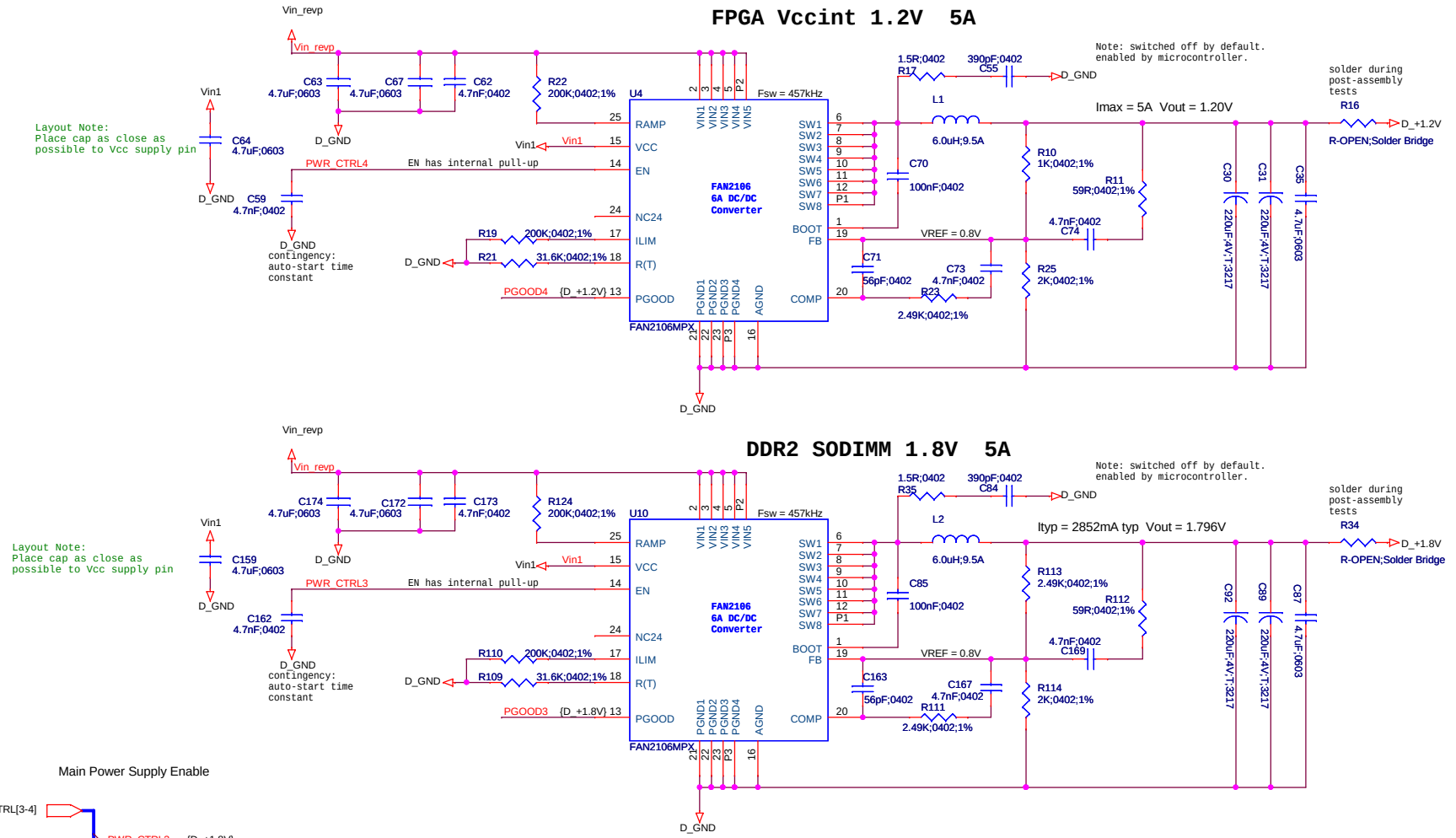
Size: B | Document Number: Y10008 | Rev: 1

Date: Wednesday, March 09, 2011 | Sheet 8 of 10



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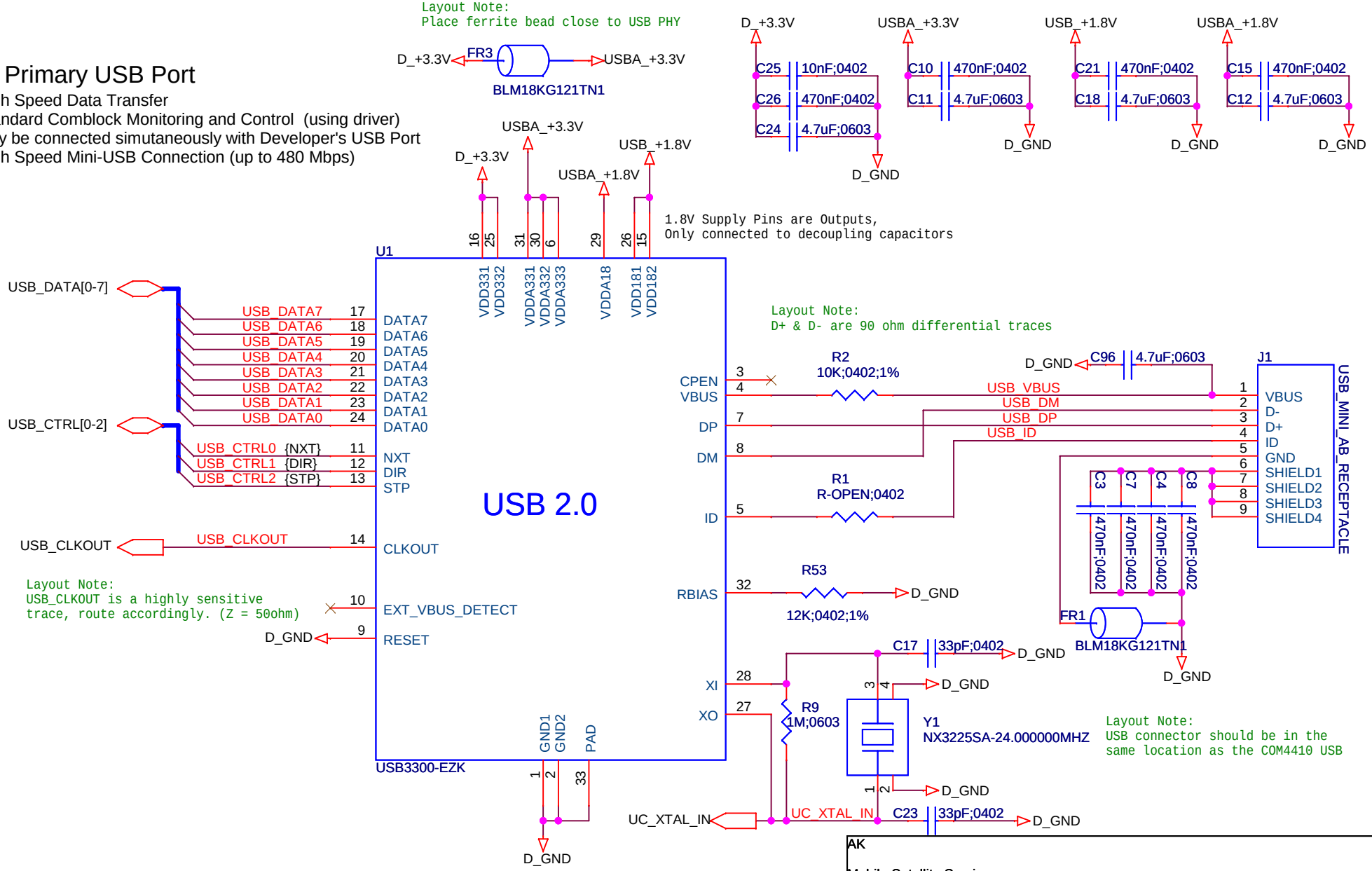
B	Y10008	1

Date: Friday, February 25, 2011 Sheet 9 of 10

J1: Primary USB Port

- High Speed Data Transfer
- Standard Comblock Monitoring and Control (using driver)
- May be connected simutaneously with Developer's USB Port
- High Speed Mini-USB Connection (up to 480 Mbps)



Note:
OTG and Host capabilites are disabled.
All USB connectivity on the COM-1500 is
limited to USB device only.

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Title	COM-1500 / USB	
Size A	Document Number Y10008	Rev 1
Date: Friday, February 25, 2011	Sheet 10 of 10	