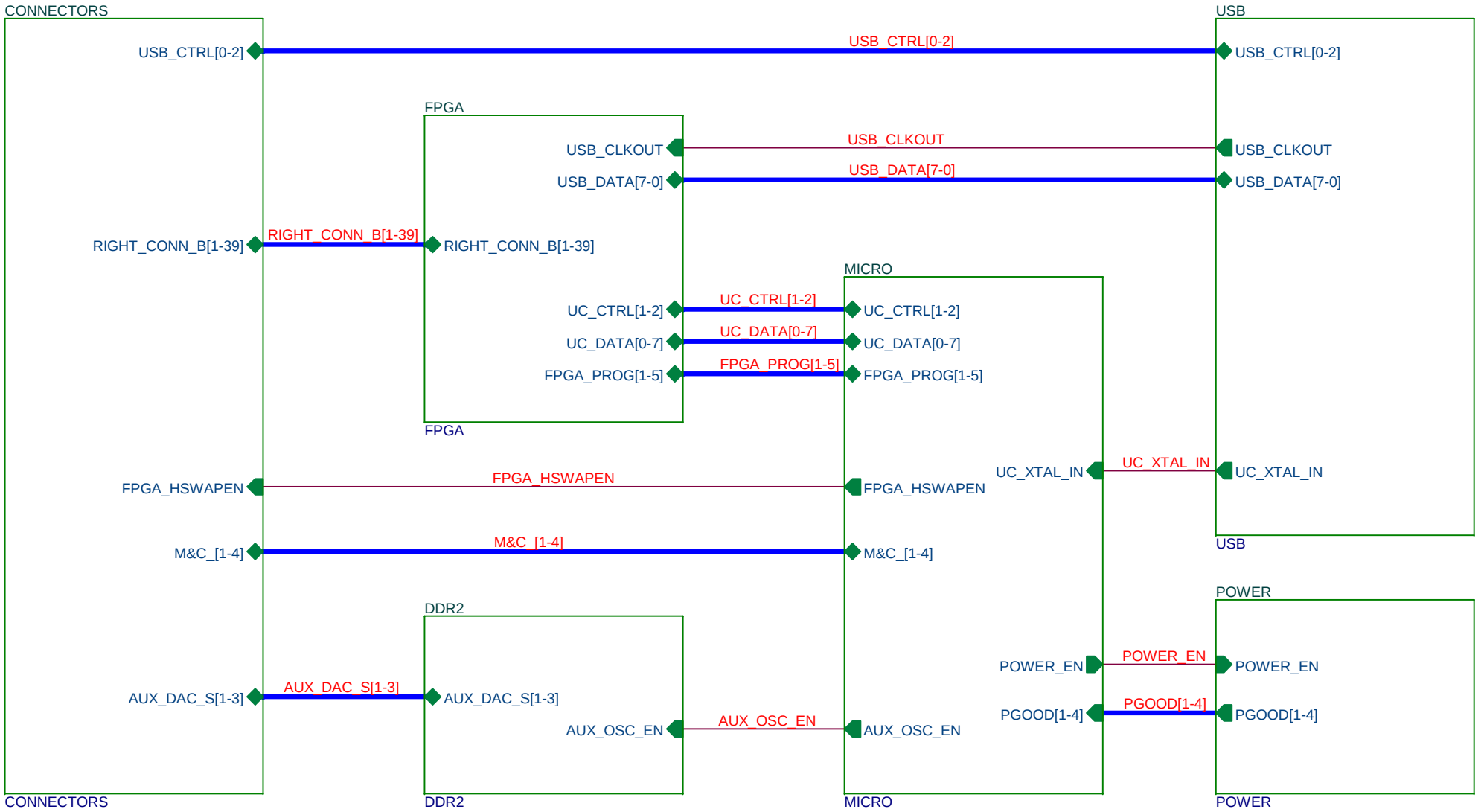

TABLE OF CONTENTS

General Layout Notes:
- use c0603 for all 0603
- use RC0402 for all 0402
- Label all TPs' names on SST

AK

Mobile Satellite Services
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Gaithersburg, MD 20879
USA

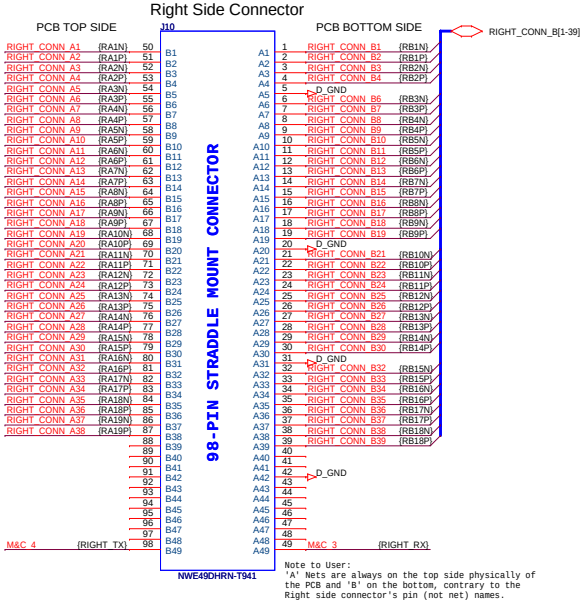
Title: COM-1600 / MAIN

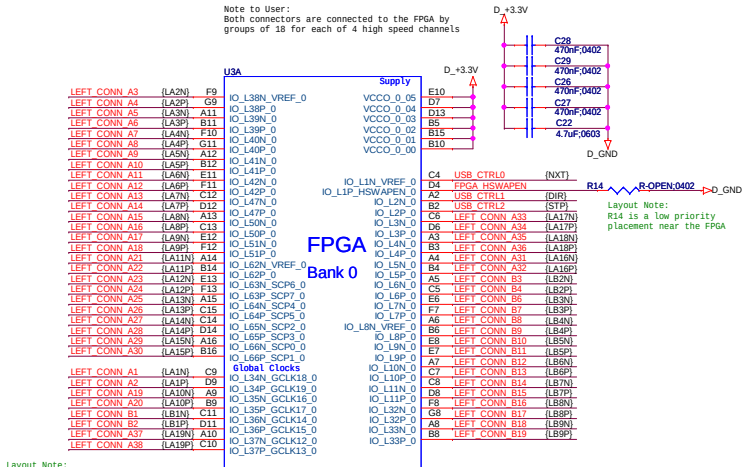
Size	Document Number	Rev
A	Y10001	2

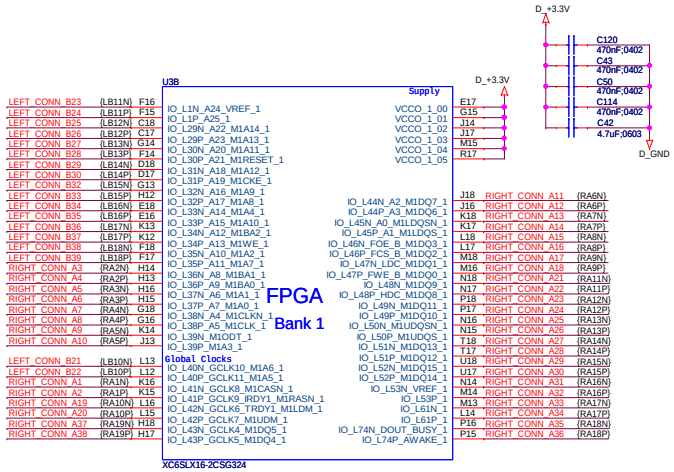
Date: Monday, June 13, 2011 Sheet 1 of 7

Left Side Connector

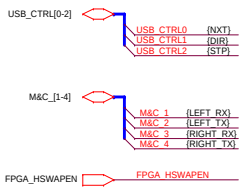
Right Side Connector



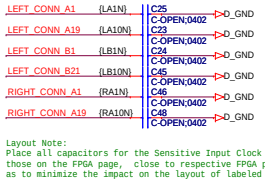




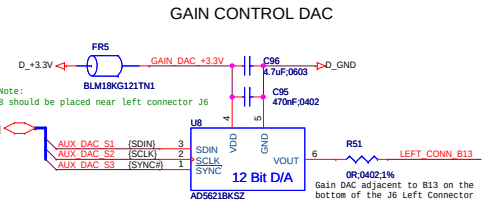
Miscellaneous Digital I/O



Sensitive Input Clock Traces



GAIN CONTROL DAC



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Title: COM-1600 / CONNECTORS

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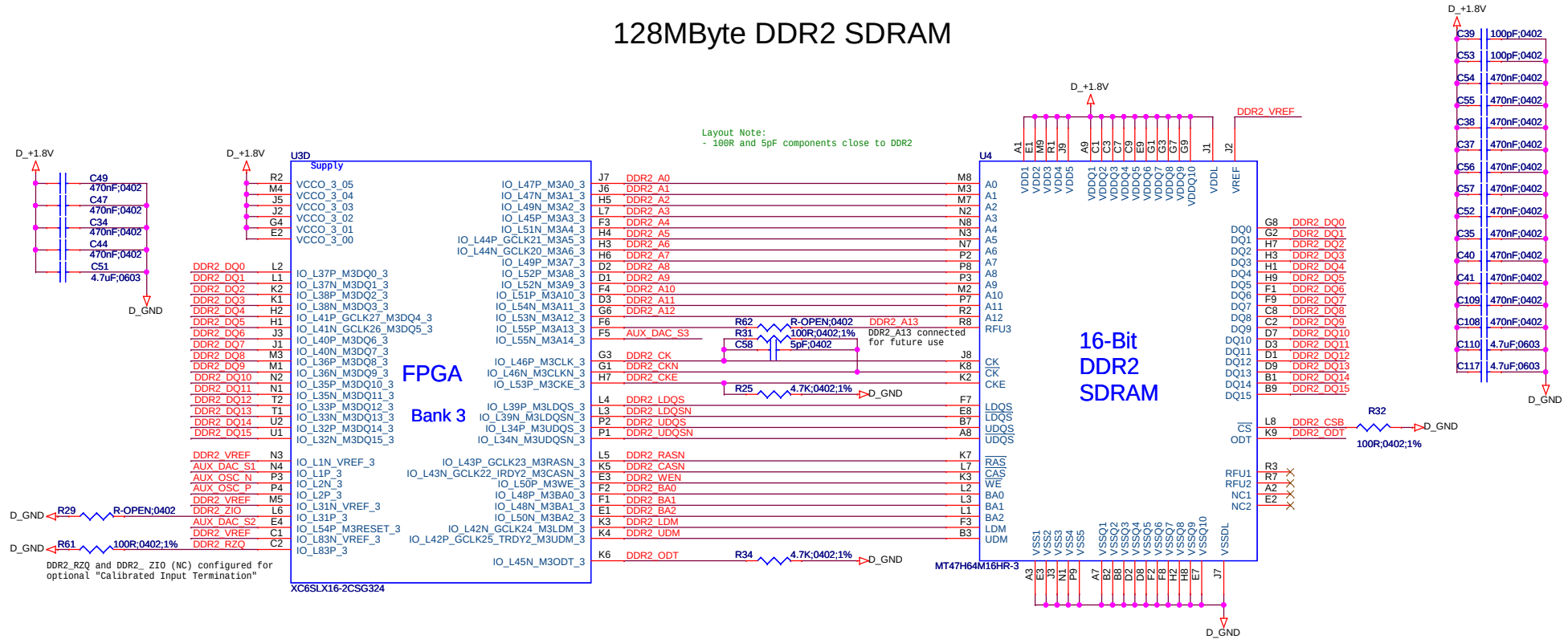
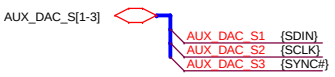
Date: Tuesday, September 28, 2010 Sheet 2 of 7

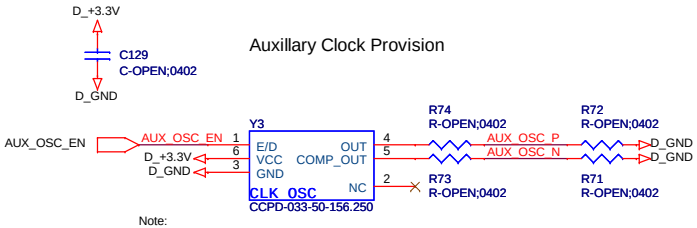
128MByte DDR2 SDRAM



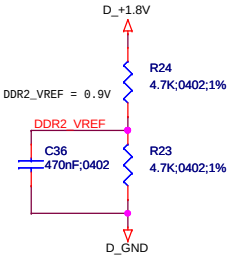
Auxillary DAC Control (SPI)



Auxillary Clock Provision



Note:
Y3 Auxillary Clock Oscillator is only a provision for a high speed clock reference to the FPGA, and is Not Populated.



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Title: COM-1600 / DDR2		
Size: B	Document Number: Y10001	Rev: 2
Date: Friday, October 08, 2010	Sheet 3 of 7	

Shared µC Interface

UC_DATA[0-7] — UC_DATA0, UC_DATA1, UC_DATA2, UC_DATA3, UC_DATA4, UC_DATA5, UC_DATA6, UC_DATA7

UC_CTRL[1-2] — UC_CTRL1 {ALE_CCLK}, UC_CTRL2 {REB_RDWRB}

FPGA Programming

FPGA_PROG[1-5] — FPGA_PROG1 {PROGB}, FPGA_PROG2 {DONE}, FPGA_PROG3 {INITB_WEB}, FPGA_PROG4 {SUSPEND}, FPGA_PROG5 {CSIB}

USB INTERFACE

USB_DATA[7-0] — USB_DATA7, USB_DATA6, USB_DATA5, USB_DATA4, USB_DATA3, USB_DATA2, USB_DATA1, USB_DATA0

USB_CLKOUT — USB_CLKOUT

DIGITAL CONNECTOR

RIGHT_CONN_B[1-39]

RIGHT_CONN_B1 {RB1N}, RIGHT_CONN_B2 {RB1P}, RIGHT_CONN_B3 {RB2N}, RIGHT_CONN_B4 {RB2P}, RIGHT_CONN_B6 {RB3N}, RIGHT_CONN_B7 {RB3P}, RIGHT_CONN_B8 {RB4N}, RIGHT_CONN_B9 {RB4P}, RIGHT_CONN_B10 {RB5N}, RIGHT_CONN_B11 {RB5P}, RIGHT_CONN_B12 {RB6N}, RIGHT_CONN_B13 {RB6P}, RIGHT_CONN_B14 {RB7N}, RIGHT_CONN_B15 {RB7P}, RIGHT_CONN_B16 {RB8N}, RIGHT_CONN_B17 {RB8P}, RIGHT_CONN_B18 {RB9N}, RIGHT_CONN_B19 {RB9P}, RIGHT_CONN_B21 {RB10N}, RIGHT_CONN_B22 {RB10P}, RIGHT_CONN_B23 {RB11N}, RIGHT_CONN_B24 {RB11P}, RIGHT_CONN_B25 {RB12N}, RIGHT_CONN_B26 {RB12P}, RIGHT_CONN_B27 {RB13N}, RIGHT_CONN_B28 {RB13P}, RIGHT_CONN_B29 {RB14N}, RIGHT_CONN_B30 {RB14P}, RIGHT_CONN_B32 {RB15N}, RIGHT_CONN_B33 {RB15P}, RIGHT_CONN_B34 {RB16N}, RIGHT_CONN_B35 {RB16P}, RIGHT_CONN_B36 {RB17N}, RIGHT_CONN_B37 {RB17P}, RIGHT_CONN_B38 {RB18N}, RIGHT_CONN_B39 {RB18P}

FPGA CONFIGURATION

D_+3.3V — C63 470nF;0402, C64 470nF;0402, C104 470nF;0402, C121 470nF;0402, C122 4.7uF;0603 — D_GND

D_+3.3V — R35 4.7K;0402;1% FPGA_PROG1 {PROGB}; D_+3.3V — R33 R-OPEN;0402 UC_CTRL1 {ALE_CCLK}; D_GND — R30 R-OPEN;0402

D_+3.3V — R37 330R;0402 FPGA_PROG2 {DONE}; D_+3.3V — R36 4.7K;0402;1% FPGA_PROG3 {INITB_WEB}

TP1 DONE

Layout Note:
- Route UC_CTRL1 as 50ohm trace
- place termination 100Rs closest to FPGA

J7 (87831-1420)

1	GND1 Vref	2	D_+3.3V
3	GND2 TMS	4	FPGA_JTAG_TMS
5	GND3 TCK	6	FPGA_JTAG_TCK
7	GND4 TDO	8	FPGA_JTAG_TDO
9	GND5 TDI	10	FPGA_JTAG_TDI
11	GND6 NC1	12	
13	GND7 NC2	14	

D_GND

FPGA JTAG header compatible with Xilinx Parallel Cable IV Model DLC7 only populated on COM-1600 development platform

Layout Note:
Orient with notch facing in towards middle of PCB

D_+3.3V — R15 10K;0402;1% — FPGA_JTAG_TCK

Layout note:
10MHZ_REF and USB_CLKOUT traces should be routed away from noise sources.

Slave SelectMAP Programming Configuration: D_GND T15, D_+3.3V N12

U3C — FPGA Bank 2 — XC6SLX16-2CSG324

Supply: VCCO_2_00 P9, VCCO_2_01 R12, VCCO_2_02 R6, VCCO_2_03 U14, VCCO_2_04 U4, VCCO_2_05 U9

D_+3.3V — P13

PROGRAM_B_2		IO_L2N_CMPMOSI_2	V16 RIGHT_CONN_B3 {RB2N}
IO_L1P_CCLK_2		IO_L2P_CMPCLK_2	U16 RIGHT_CONN_B4 {RB2P}
IO_L3N_MOSI_CSI_B_MISO0_2		IO_L5N_2	V15 RIGHT_CONN_B6 {RB3N}
IO_L48N_RDWR_B_VREF_2		IO_L5P_2	U15 RIGHT_CONN_B7 {RB3P}
DONE_2		IO_L14N_D12_2	V13 RIGHT_CONN_B8 {RB4N}
IO_L65P_INIT_B_2		IO_L14P_D11_2	U13 RIGHT_CONN_B9 {RB4P}
SUSPEND		IO_L15N_2	N11 RIGHT_CONN_B10 {RB5N}
CMPCS_B_2		IO_L15P_2	M11 RIGHT_CONN_B11 {RB5P}
		IO_L16N_VREF_2	T11 RIGHT_CONN_B12 {RB6N}
IO_L3P_D0_DIN_MISO_MISO1_2		IO_L16P_2	R11 RIGHT_CONN_B13 {RB6P}
IO_L12P_D1_MISO2_2		IO_L19N_2	V12 RIGHT_CONN_B14 {RB7N}
IO_L12N_D2_MISO3_2		IO_L19P_2	T12 RIGHT_CONN_B15 {RB7P}
IO_L49P_D3_2		IO_L20N_2	P11 RIGHT_CONN_B16 {RB8N}
IO_L49N_D4_2		IO_L20P_2	N10 RIGHT_CONN_B17 {RB8P}
IO_L62P_D5_2		IO_L22N_2	N9 RIGHT_CONN_B18 {RB9N}
IO_L62N_D6_2		IO_L22P_2	M10 RIGHT_CONN_B19 {RB9P}
IO_L48P_D7_2		IO_L23N_2	V11 RIGHT_CONN_B23 {RB11N}
		IO_L23P_2	U11 RIGHT_CONN_B24 {RB11P}
IO_L1N_M0_CMPMISO_2		IO_L40N_2	N8 RIGHT_CONN_B25 {RB12N}
IO_L13P_M1_2		IO_L40P_2	M8 RIGHT_CONN_B26 {RB12P}
		IO_L41N_VREF_2	V8 RIGHT_CONN_B27 {RB13N}
TCK		IO_L41P_2	U8 RIGHT_CONN_B28 {RB13P}
TDI JTAG		IO_L43N_2	V7 RIGHT_CONN_B29 {RB14N}
TDO		IO_L43P_2	U7 RIGHT_CONN_B30 {RB14P}
TMS		IO_L44N_2	P8 RIGHT_CONN_B32 {RB15N}
Global Clocks		IO_L44P_2	N7 RIGHT_CONN_B33 {RB15P}
IO_L29N_GCLK2_2		IO_L45N_2	V6 RIGHT_CONN_B34 {RB16N}
IO_L29P_GCLK3_2		IO_L45P_2	T6 RIGHT_CONN_B35 {RB16P}
IO_L30N_GCLK0_USERCCLK_2		IO_L47N_2	P7 RIGHT_CONN_B36 {RB17N}
IO_L30P_GCLK1_D13_2		IO_L47P_2	N6 RIGHT_CONN_B37 {RB17P}
IO_L31N_GCLK30_D15_2		IO_L46N_2	T7 USB_DATA0
IO_L31P_GCLK31_D14_2		IO_L46P_2	R7 USB_DATA1
IO_L32N_GCLK28_2		IO_L63N_2	V4 USB_DATA2
IO_L32P_GCLK29_2		IO_L63P_2	T4 USB_DATA3
		IO_L64N_D9_2	P6 USB_DATA4
		IO_L64P_D8_2	N5 USB_DATA5
	Not with Differential Pair		
		IO_L65N_CSO_B_2	V3 USB_DATA6
		IO_L13N_D10_2	P12 USB_DATA7

FPGA_PROG1 {PROGB}	V2
UC_CTRL1 {ALE_CCLK}	R15
FPGA_PROG5 {CSIB}	T13
UC_CTRL2 {REB_RDWRB}	T5
FPGA_PROG2 {DONE}	V17
FPGA_PROG3 {INITB_WEB}	U3
FPGA_PROG4 {SUSPEND}	R16
UC_DATA0	R13
UC_DATA1	T14
UC_DATA2	V14
UC_DATA3	U5
UC_DATA4	V5
UC_DATA5	R3
UC_DATA6	T3
UC_DATA7	R5
FPGA_JTAG_TCK	A17
FPGA_JTAG_TDI	D15
FPGA_JTAG_TDO	D16
FPGA_JTAG_TMS	B18
RIGHT_CONN_B1 {RB1N}	T10
RIGHT_CONN_B2 {RB1P}	R10
RIGHT_CONN_B21 {RB10N}	V10
RIGHT_CONN_B22 {RB10P}	U10
RIGHT_CONN_B38 {RB18N}	T8
RIGHT_CONN_B39 {RB18P}	R8
10MHZ_REF	V9
USB_CLKOUT	T9

Note:
Other FPGA banks can be found on their respective functions' primary schematic page

10MHz EXTERNAL FREQUENCY REFERENCE

RIGHT_CONN_B[1-39]

D_+3.3V — R40 10K;0402;1%

D_+3.3V — D_GND — C71 470nF;0402 — D_GND

J9 SMA_EDGE_FEMALE (GND1–GND4) — C72 470nF;0402 — R41 12.4K;0402;1% — D_GND

U6 NC7SZ04P5X (NC, A, Y, VCC, GND) — 10MHZ_REF

Layout note:
Noise sources should be routed away from reference clock circuitry.

D2 TZM5227B

3.6V Zener: Prevent over/under-voltage damage to NC7SZ04 at analog inputs.

Layout Note:
SMA edge location should be the same with COM2802

Sensitive Input Clock Traces

UC_CTRL1	{ALE_CCLK}	C65 C-OPEN;0402	D_GND
USB_CLKOUT		C61 C-OPEN;0402	D_GND
RIGHT_CONN_B1	{RB1N}	C60 C-OPEN;0402	D_GND
RIGHT_CONN_B21	{RB10N}	C62 C-OPEN;0402	D_GND
FPGA_JTAG_TCK		C30 C-OPEN;0402	D_GND

Layout Note:
Place clock capacitors close to the FPGA

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USA

Title: COM-1600 / FPGA

Size: B | Document Number: Y10001 | Rev: 2

Date: Thursday, October 07, 2010 | Sheet 4 of 7

Shared µC Interface

UC_CTRL[1-2]
- UC_CTRL1 {ALE_CCLK}
- UC_CTRL2 {REB_RDWRB}

UC_DATA[0-7]
- UC_DATA0
- UC_DATA1
- UC_DATA2
- UC_DATA3
- UC_DATA4
- UC_DATA5
- UC_DATA6
- UC_DATA7

FPGA Programming

FPGA_PROG[1-5]
- FPGA_PROG1 {PROGB}
- FPGA_PROG2 {DONE}
- FPGA_PROG3 {INITB_WEB}
- FPGA_PROG4 {SUSPEND}
- FPGA_PROG5 {CSIB}

FPGA_HSWAPEN
- FPGA_HSWAPEN

Miscellaneous Digital I/O

M&C_[1-4]
- M&C_1 {LEFT_RX}
- M&C_2 {LEFT_TX}
- M&C_3 {RIGHT_RX}
- M&C_4 {RIGHT_TX}

Power Good Indicators

PGOOD[1-4]
- PGOOD1 {ARM_+3.3V}
- PGOOD2 {D_+3.3V}
- PGOOD3 {D_+1.8V}
- PGOOD4 {D_+1.2V}

POWER_EN
- POWER_EN

AUX_OSC_EN
- AUX_OSC_EN

ARM_+3.3V
- C8 10nF;0402
- C9 10nF;0402
- C12 470nF;0402
- C19 470nF;0402
- C20 470nF;0402
- C18 470nF;0402
- C14 4.7uF;0603
- C21 4.7uF;0603

D_GND

JP1 - Flash Drive Access Mode Select Jumper

JP1 Jumper Position = Flash Drive Access Mode:
1-2 = USB Flash Drive
2-3 or NC = Standard Comblock Monitoring & Control
(NC = Jumper Not Connected in either position)

JP1
- UC_FLASH_MODE
- ARM_+3.3V
- D_GND

TSW-103-07-F-S

Layout Note:
Add Power Source description on Silkscreen near JP1

J1: Developer's USB Port

- Microcontroller programming
- Alternate +5V Power Source (enabled by JP2, Jumper)
- USB Flash Drive Device mode for FPGA Flash Programming (set JP1)
- Standard Comblock Monitoring and Control (using Comblock driver)
- May be connected simutaneously with Primary USB Port

ARM_+3.3V
- R12 10R;0402
- R13 10R;0402
- C17 470nF;0402
- C16 4.7uF;0603

D_GND

USB_CONNECTB
- R78 1.5K;0402
- Q5 FDN306P
- R2 1.5K;0402

USB_+5.0V
- C6 4.7uF;0603

Layout Note:
Place C6 close to J1

J1
- VBUS
- D-
- D+
- ID
- GND
- SHIELD1
- SHIELD2
- SHIELD3
- SHIELD4

USB_MINI_AB_RECEPTACLE

Layout Note:
USB connector should be in the same location as the COM4410 USB

FR2
BLM18KG121TN1

C75 470nF;0402
C4 470nF;0402
C78 470nF;0402
C76 470nF;0402

U2 — ARM Cortex-M3 µC

VDD_1 21, VDD_2 42, VDD_3 56, VDD_4 77, VBAT 16, VDDREG_1 34, VDDREG_2 67, VDDA 8, VREFP 10, VREFN 12
VSS_1 24, VSS_2 33, VSS_3 43, VSS_4 57, VSS_5 66, VSS_6 78, VSSA 9

P0[0]/RD1/TXD3/SDA1
P0[1]/TD1/RXD3/SCL1
P0[2]/TXD0/AD0[7]
P0[3]/RXD0/AD0[6]
P0[6]/I2SRX_SDA/SSEL1/MAT2[0]
P0[7]/I2STX_CLK/SCK1/MAT2[1]
P0[8]/I2STX_WS/MISO1/MAT2[2]
P0[9]/I2STX_SDA/MOSI1/MAT2[3]
P0[10]/TXD2/SDA2/MAT3[0]
P0[11]/RXD2/SCL2/MAT3[1]
P0[15]/TXD1/SCK0/SCK
P0[16]/RXD1/SSEL0/SSEL
P0[17]/CTS1/MISO0/MISO
P0[18]/DCD1/MOSI0/MOSI
P0[22]/RTS1/TD1
P0[25]/AD0[2]/I2SRX_SDA/TXD3
P0[26]/AD0[3]/AOUT/RXD3

P1[30]/VBUS/AD0[4]
P0[30]/USB_D-
P0[29]/USB_D+

P2[0]/PWM1[1]/TXD1
P2[1]/PWM1[2]/RXD1
P2[2]/PWM1[3]/CTS1/TRACEDATA[3]
P2[3]/PWM1[4]/DCD1/TRACEDATA[2]
P2[4]/PWM1[5]/DSR1/TRACEDATA[1]
P2[5]/PWM1[6]/DTR1/TRACEDATA[0]
P2[6]/PCAP1[0]/RI1/TRACECLK
P2[7]/RD2/RTS1
P2[8]/TD2/TXD2
P2[9]/USB_CONNECT/RXD2
P2[10]/EINT0/NMI

P4[28]/RX_MCLK/MAT2[0]/TXD3
P4[29]/TX_MCLK/MAT2[1]/RXD3

P1[0]
P1[1]
P1[4]
P1[8]
P1[9]
P1[10]
P1[14]
P1[15]
P1[18]/USB_UP_LED/PWM1[1]/CAP1[0]
P1[19]/MC0A/USB_PPWR/CAP1[1]
P1[20]/MCI0/PWM1[2]/SCK0
P1[22]/MCOB0/USB_PWRD/MAT1[0]
P1[23]/MCI1/PWM1[4]/MISO0
P1[24]/MCI2/PWM1[5]/MOSI0
P1[25]/MCOA1/MAT1[1]
P1[26]/MCOB1/PWM1[6]/CAP0[0]
P1[28]/MCOA2/PCAP1[0]/MAT0[0]
P1[29]/MCOB2/PCAP1[1]/MAT0[1]
P1[31]/SCK1/AD0[5]

TRST
TDI
TMS/SWDIO
TCK/SWDCLK
TDO/SWO
RESET
RSTOUT

XTAL1
XTAL2
RTCX1
RTCX2

LPC1759FBD80

FPGA_PROG1	{PROGB}	37	
FPGA_PROG4	{SUSPEND}	38	
M&C_2	{LEFT_TX}	79	
M&C_1	{LEFT_RX}	80	
FPGA_PROG2	{DONE}	64	
FPGA_PROG3	{INITB_WEB}	63	
PGOOD1	{ARM_+3.3V}	62	
PGOOD2	{D_+3.3V}	61	
PGOOD3	{D_+1.8V}	39	
PGOOD4	{D_+1.2V}	40	
UC_TP1	{SCK0}	47	
UC_TP2	{SSEL0}	48	
UC_TP3	{MISO0}	46	
UC_TP4	{MOSI0}	45	
FPGA_HSWAPEN		44	
UC_ADC1		7	
UC_ANALOG		6	
POWER_EN		76	
TEST_EDGE1		75	
		74	
		73	
		72	
		71	
		70	
UC_CTRL3	{NAND_WEB}	69	
USB_CONNECTB		25	
AUX_OSC_EN		26	
UC_PWM_u		27	
UC_FLASH_MODE		28	
NAND_R/BB2		29	
NAND_R/BB		30	
NAND_CEB2		31	
NAND_WPB		32	
NAND_CLE		35	
NAND_CEB		36	
UC_ADC2		17	

18	Layout Note:	USB_+5.0V	
23	Z match D+ & D- to	UC_USB_DM	R7 33R;0402;1%
22	90 ohm diff	UC_USB_DP	R8 33R;0402;1%
60	UC_DATA0		
59	UC_DATA1		
58	UC_DATA2		
55	UC_DATA3		
54	UC_DATA4		
53	UC_DATA5		
52	UC_DATA6		
51	UC_DATA7		
50	UC_CTRL1	{ALE_CCLK}	
49	UC_CTRL2	{REB_RDWRB}	
41	FPGA_PROG5	{CSIB}	R11 10K;0402;1%
65	M&C_4	{RIGHT_TX}	
68	M&C_3	{RIGHT_RX}	
4	ARM_JTAG_TRSTB		
2	ARM_JTAG_TDI		
3	ARM_JTAG_TMS		
5	ARM_JTAG_TCK		
1	ARM_JTAG_RTCK		
14	ARM_JTAG_TDO		
11	UC_RESET		
19	UC_XTAL_IN		C91 100pF;0402
20			C92 100pF;0402
13			C13 12pF;0402
15			C11 33pF;0402

Y2
AB26TRB-32.768KHZ

R49 10K;0402;1%
R52 10K;0402;1%
R55 10K;0402;1%
R57 10K;0402;1%
R59 10K;0402;1%

J5
TSW-110-07-F-D

ARM_JTAG_DE_B
R50 510R;0402;1%
C94 470nF;0402
R54 10K;0402;1%
R53 10K;0402;1%
R48 10K;0402;1%
R47 10K;0402;1%

ARM JTAG standard 20 pin programming header only populated on COM-1600 development platform

128MByte NAND

U9
MT29F1G08AACWP
x8 bit NAND Flash Memory
48-pin TSOP

NC1			
NC2			
NC3			
NC4		R/B	
NC5		RFU1	
NC11		RE	
NC14		CE	
NC15		RFU2	
NC23			
NC24		CLE	
NC25		ALE	
NC26			
NC27		WE	
NC28		WP	
NC33			
NC34			
NC35			
NC39		I/O0	
NC40		I/O1	
NC45		I/O2	
NC46		I/O3	
NC47		I/O4	
NC48		I/O5	
DNU1		I/O6	
DNU2		I/O7	
DNU3			

7	NAND_R/BB	R77	10K;0402;1%
6	NAND_R/BB2		
8	UC_CTRL2	{REB_RDWRB}	
9	NAND_CEB		
10	NAND_CEB2		
16	NAND_CLE		
17	UC_CTRL1	{ALE_CCLK}	
18	UC_CTRL3	{NAND_WEB}	
19	NAND_WPB		
29	UC_DATA0		
30	UC_DATA1		
31	UC_DATA2		
32	UC_DATA3		
41	UC_DATA4		
42	UC_DATA5		
43	UC_DATA6		
44	UC_DATA7		

D_+3.3V
D_GND
C84 470nF;0402
C98 470nF;0402

Note:
NAND_CEB2 & NAND_R/BB2 nets are connected for future use with a potential 8Gb NAND part or larger.

C70 470nF;0402

Microcontroller Programming Interface

J8
CARD EDGE CONNECTOR
MEC1-108-01-S-D-RA1-SL

M&C_1	{LEFT_RX}	M&C_2	{LEFT_TX}
TEST_EDGE1			
FPGA_PROG5	{CSIB}		

Please note:
Serial link is TTL NOT RS232.

Optional LPF for µC's PWM output

C7 C-OPEN;0603
UC_PWM
R9 0R;0402;1%
UC_PWM_u

Layout Note:
LPF placement should be near micro

User Defined Analog/Digital µC I/O

J4
TMMH-106-01-L-D

UC_ANALOG			
UC_PWM			
UC_ADC1			
UC_ADC2			
UC_TP1	{SCK0}		
UC_TP2	{SSEL0}		
UC_TP3	{MISO0}		
UC_TP4	{MOSI0}		

2mm Header
NOT POPULATED

Note:
All user I/O pins can be configured as general purpose digital signals, interrupts or specialized signals as indicated by their respective net names. UC_ANALOG can be configured as an ADC input or DAC ouput. UC_TP[1-4] may be configured for a high speed SSP interface.

System Reset Button

SW1
SW TACT-SPST-2/SM

Note: System Reset Button (TBC)
Pressing will reset the microcontroller and subsequently the FPGA and load Personality #1, as seen in Personalities window of Comblock Control Center

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+5V Supply

JP2 - Power Source Jumper

Green Terminal Block
OPERATIONAL RANGE: 4.75 - 5.5V

J3 — 1757475

USB_+5.0V

JP2 — TSW-103-07-F-S

Power Sources by Jumper Position:
1-2 = J5*, Developer's USB Connector (where TBD)
2-3 = J8*, Green Terminal Block

Layout Note:
Add Power Source description
on Silkscreen near JP1*

FR3 — BLM18KG121TN1

Layout Note:
Q2, Q3 & Q4 must be placed and routed for a high current throughput.

Reverse Voltage Protection — Q4 FDN306P

Over Voltage Protection (5.85V) — D4 BZX84C5V1

Note: If Q2 voltage dropout is too great use Zetex ZXTP19020DFFTA

Q2 FMMT718TA, Q1 FMMT718TA

U7 — LP3982IMM-ADJ NOPB (LDO Adj 300mA)

Imax = 90mA Vout = 3.31V

ARM_+3.3V

U3E — XC6SLX16-2CSG324

FPGA Supply

D_+1.2V, D_+3.3V

Note to User:
JP2 Power Source Jumper must be connected.

Main Power Supply Enable — Q3 FDN306P, R1 3.3K;0402;1%, D1 TZM5231B

FAN2013B DC/DC converters:
2A max peak output current
1.2MHz switching

Vin

Layout Note: FAN2013 (x3)
Place Vin caps as close as possible to Vin and PGND pins

U10 — FAN2013BMPX — L1 6.8uH;3.1A — Ityp = ~300mA Vout = 3.28V — D_+3.3V

U5 — FAN2013BMPX — L2 6.8uH;3.1A — Ityp = ~400mA Vout = 1.82V — D_+1.8V

U11 — FAN2013BMPX — L3 6.8uH;3.1A — Ityp = ~1.5A Vout = 1.21V — D_+1.2V

D3 SMBJ5.0A-E3

Layout Note:
TVS component placed near DC/DC Converter in ground return path to terminal block

Main Power Supply Enable

POWER_EN

Power Good Indicators

PGOOD[1-4]

PGOOD1 {ARM_+3.3V}
PGOOD2 {D_+3.3V}
PGOOD3 {D_+1.8V}
PGOOD4 {D_+1.2V}

PCB Mounting Holes

H3, H4, H1, H2

Power Requirements (*TBC)

COMP	V	mA
FPGA	+3.3	200*
MICRO	+3.3	50*
NAND	+3.3	50*
USB	+3.3	50
DDDR2	+1.8	580*
FPGA	+1.2	1500

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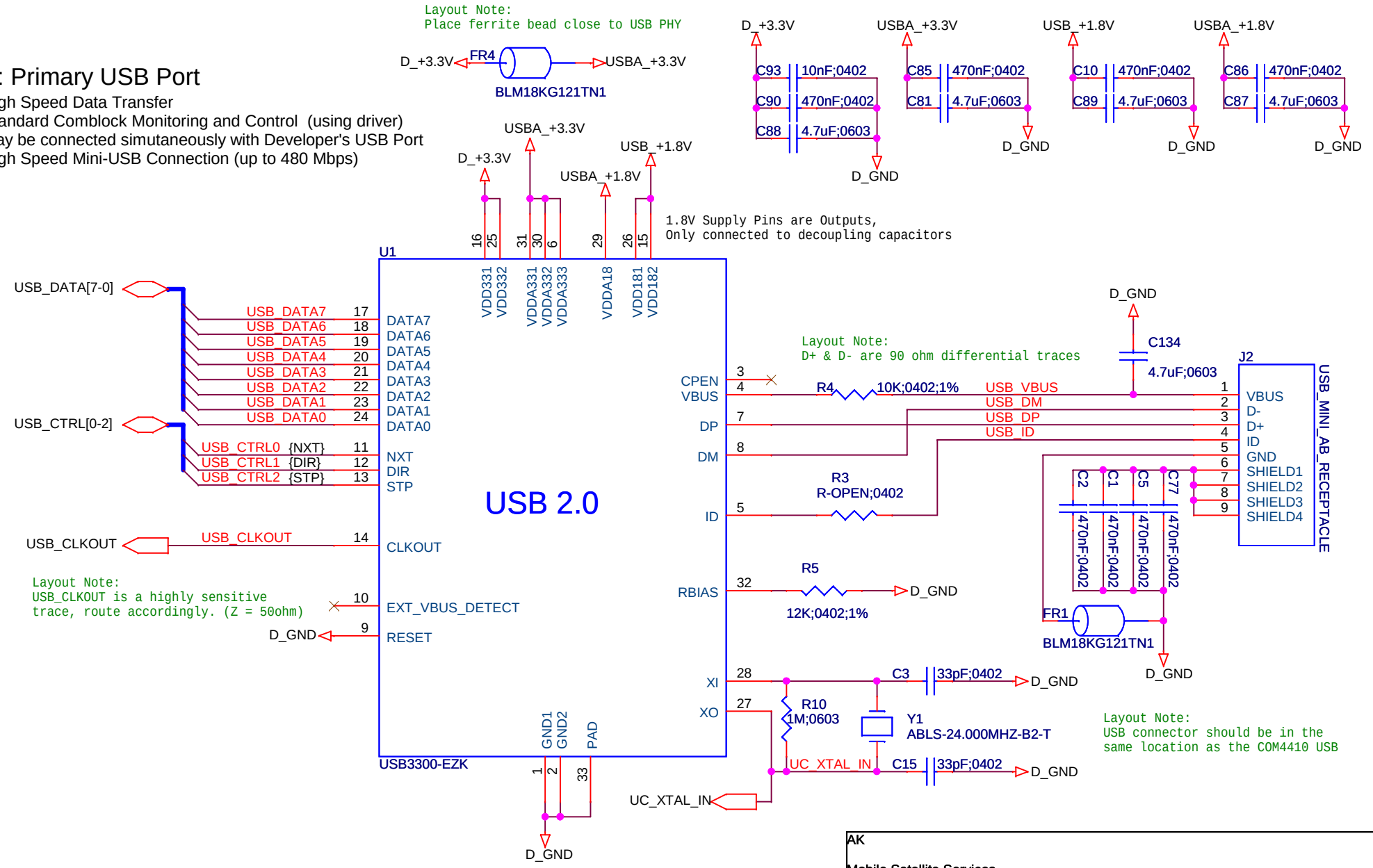
J2: Primary USB Port

- High Speed Data Transfer
- Standard Comblock Monitoring and Control (using driver)
- May be connected simutaneously with Developer's USB Port
- High Speed Mini-USB Connection (up to 480 Mbps)



Note:
OTG and Host capabilites are disabled.
All USB connectivity on the COM-1600 is
limited to USB device only.

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