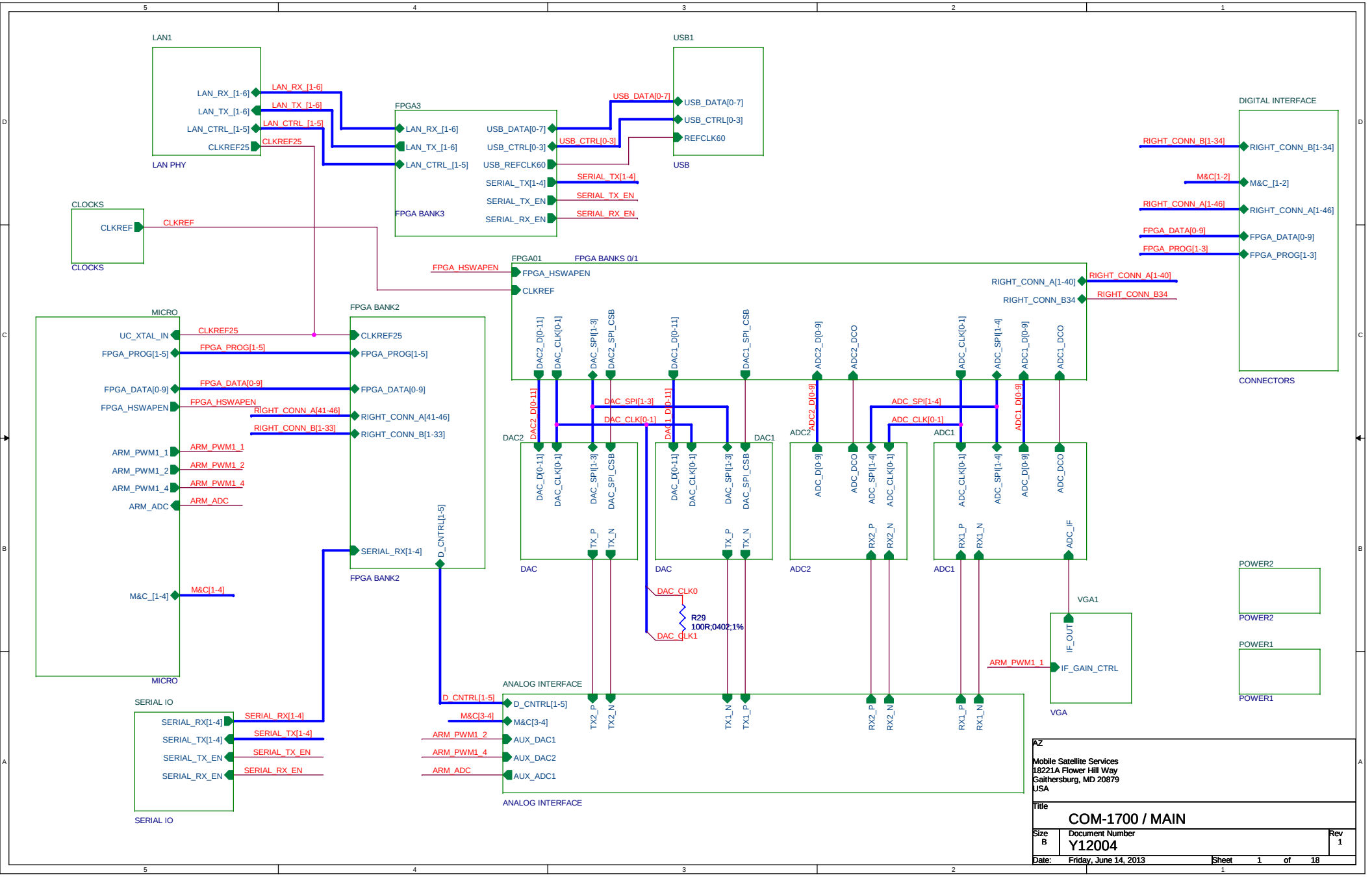

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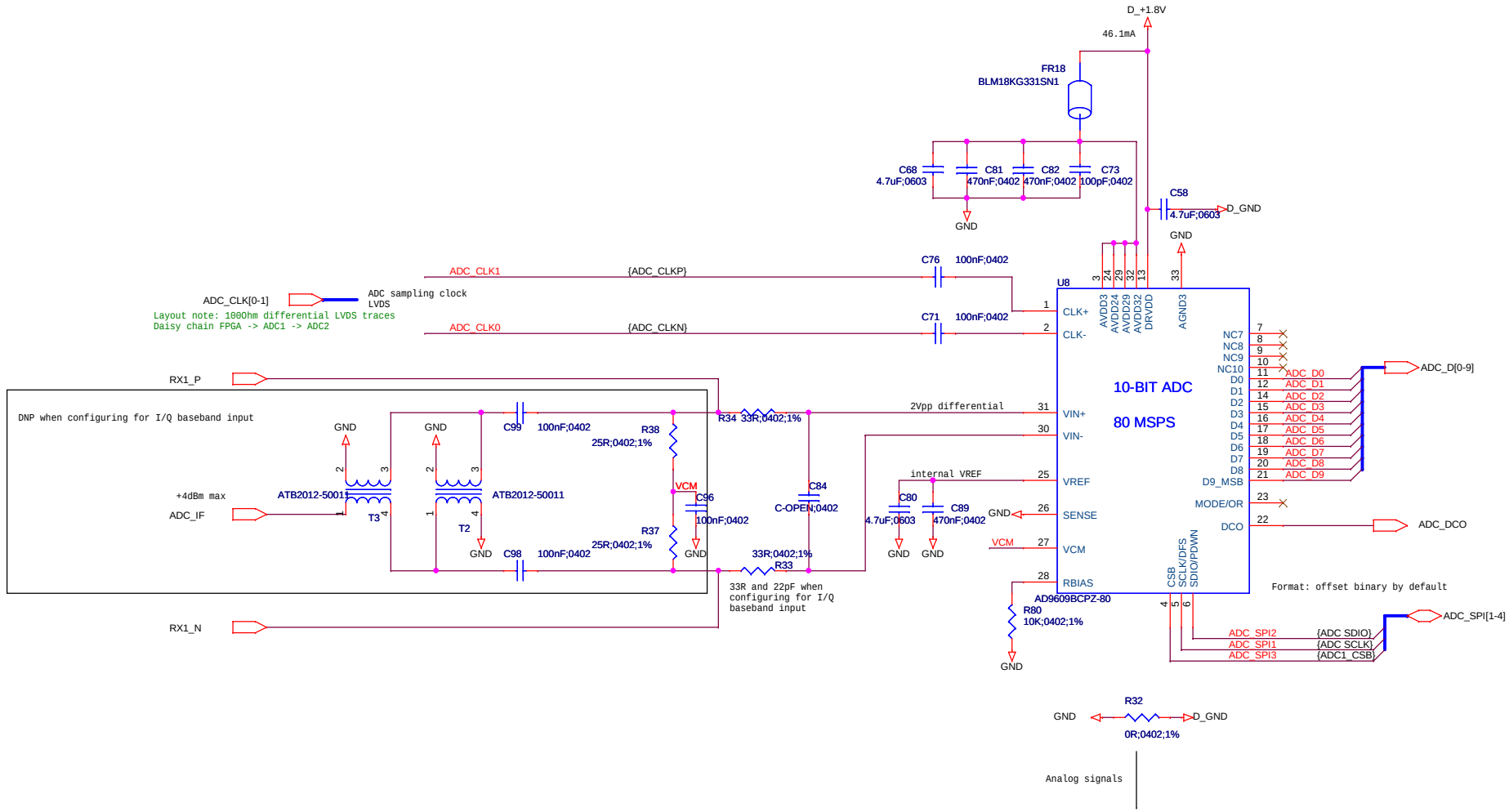
USA

Title: COM-1700 / MAIN

Size	Document Number	Rev
B	Y12004	1

Date: Friday, June 14, 2013 Sheet 1 of 18

ADC1 (IF or baseband I)



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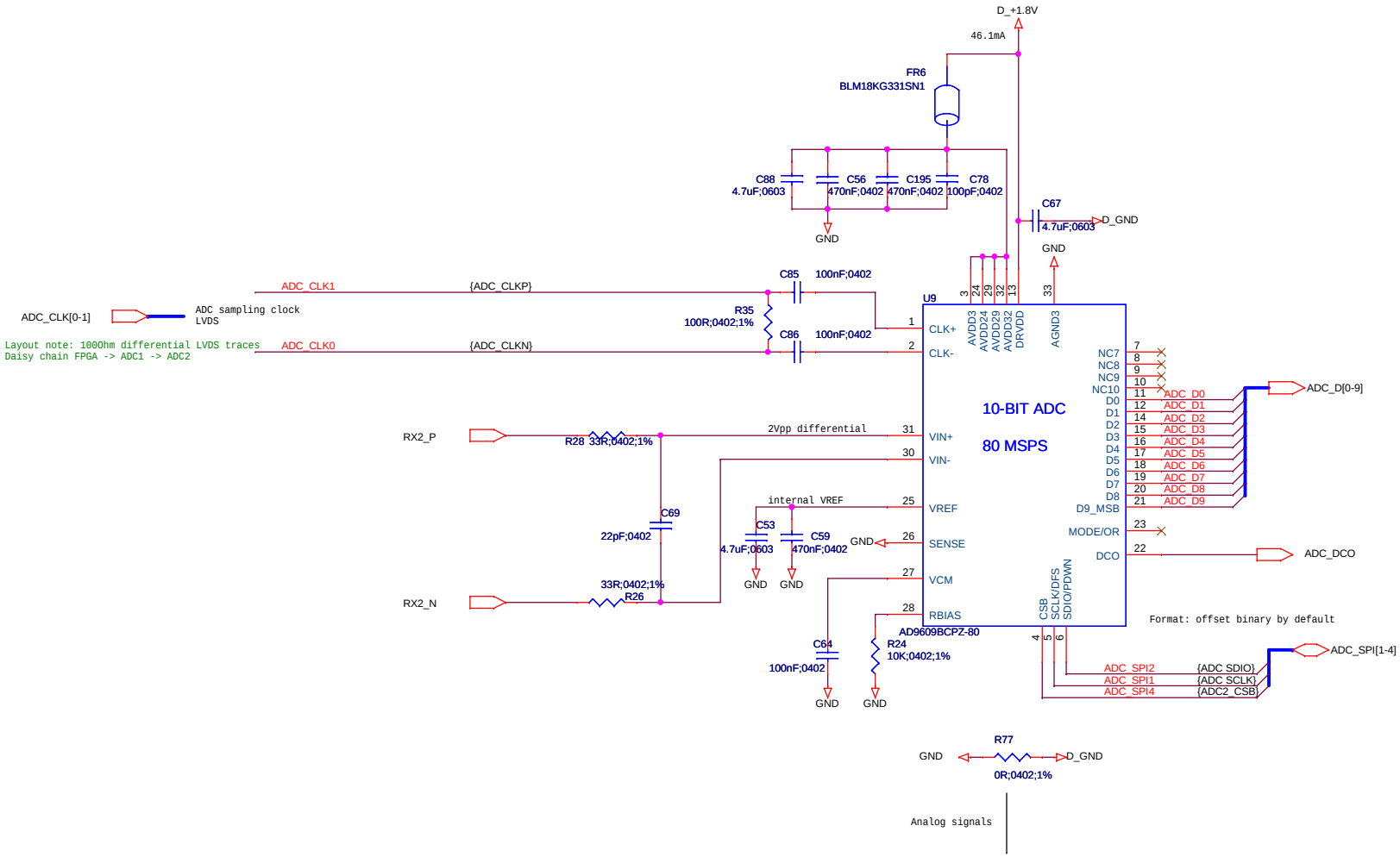
Title	COM-1700 / ADC1	
Size B	Document Number Y12004	Rev 1
Date: Wednesday, June 12, 2013	Sheet 2 of 18	

ADC2 (baseband Q)



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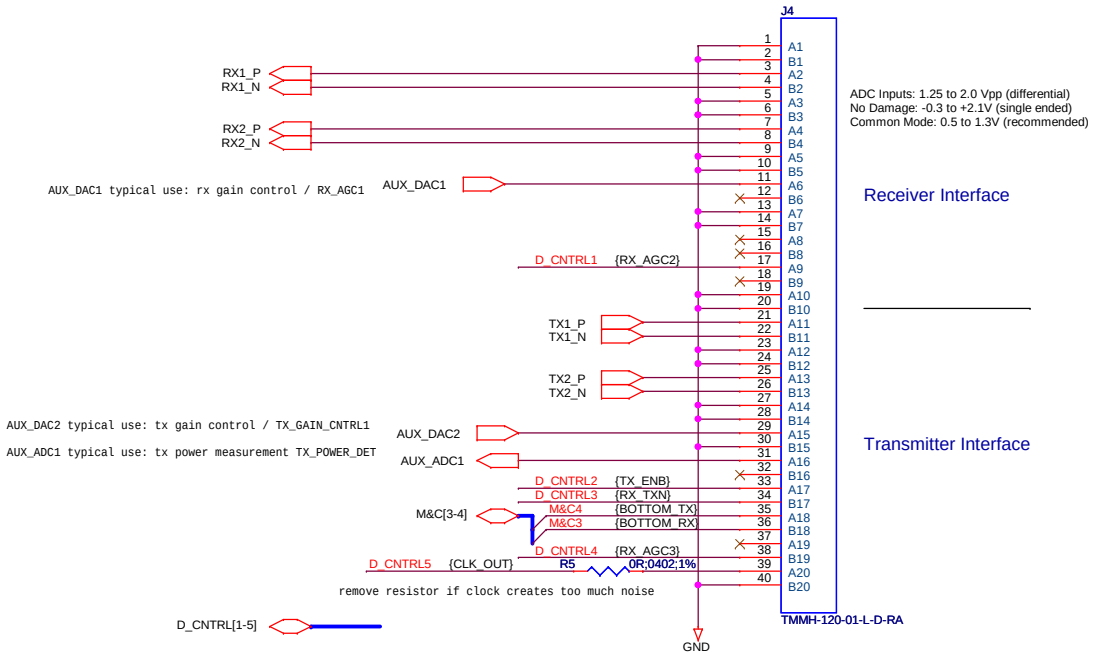
Title: COM-1700 / ADC2		
Size: B	Document Number: Y12004	Rev: 1
Date: Wednesday, June 12, 2013	Sheet 3 of 18	

TRANSCEIVER INTERFACE

Differential analog I/O
Right-angle 2 row x 20 positions (40 pin) 2mm Connector



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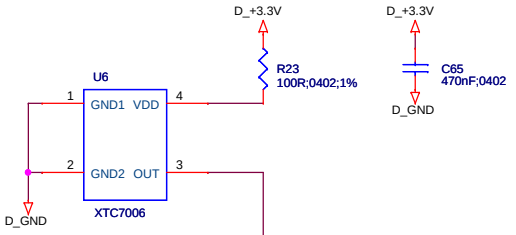
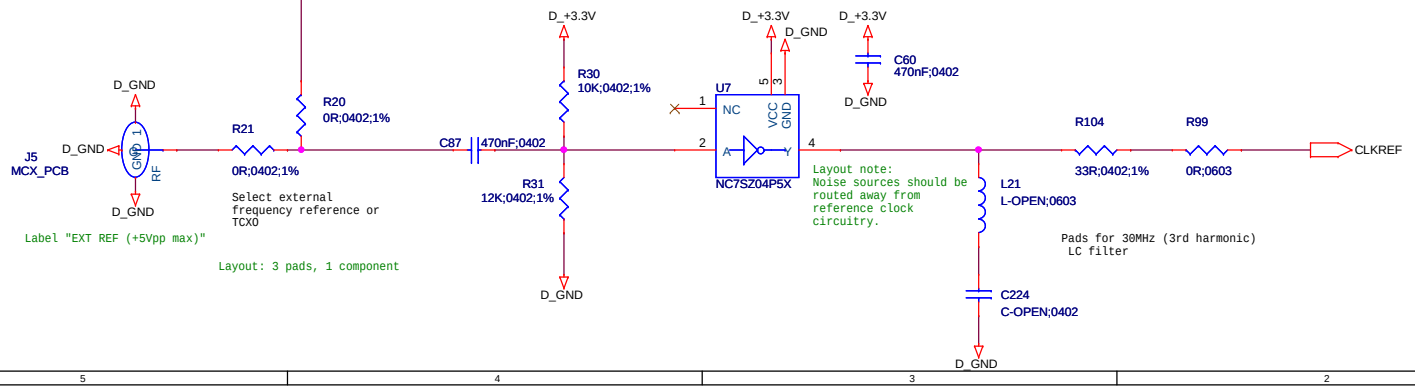
Title	COM-1700 / ANALOG INTERFACE	
Size B	Document Number Y12004	Rev 2
Date: Wednesday, June 12, 2013	Sheet 4 of 18	

(26MHz) TCXO

2ppm tolerance, 0.5ppm over -30/+85C, 1ppm/year aging



(10MHz) EXTERNAL FREQUENCY REFERENCE



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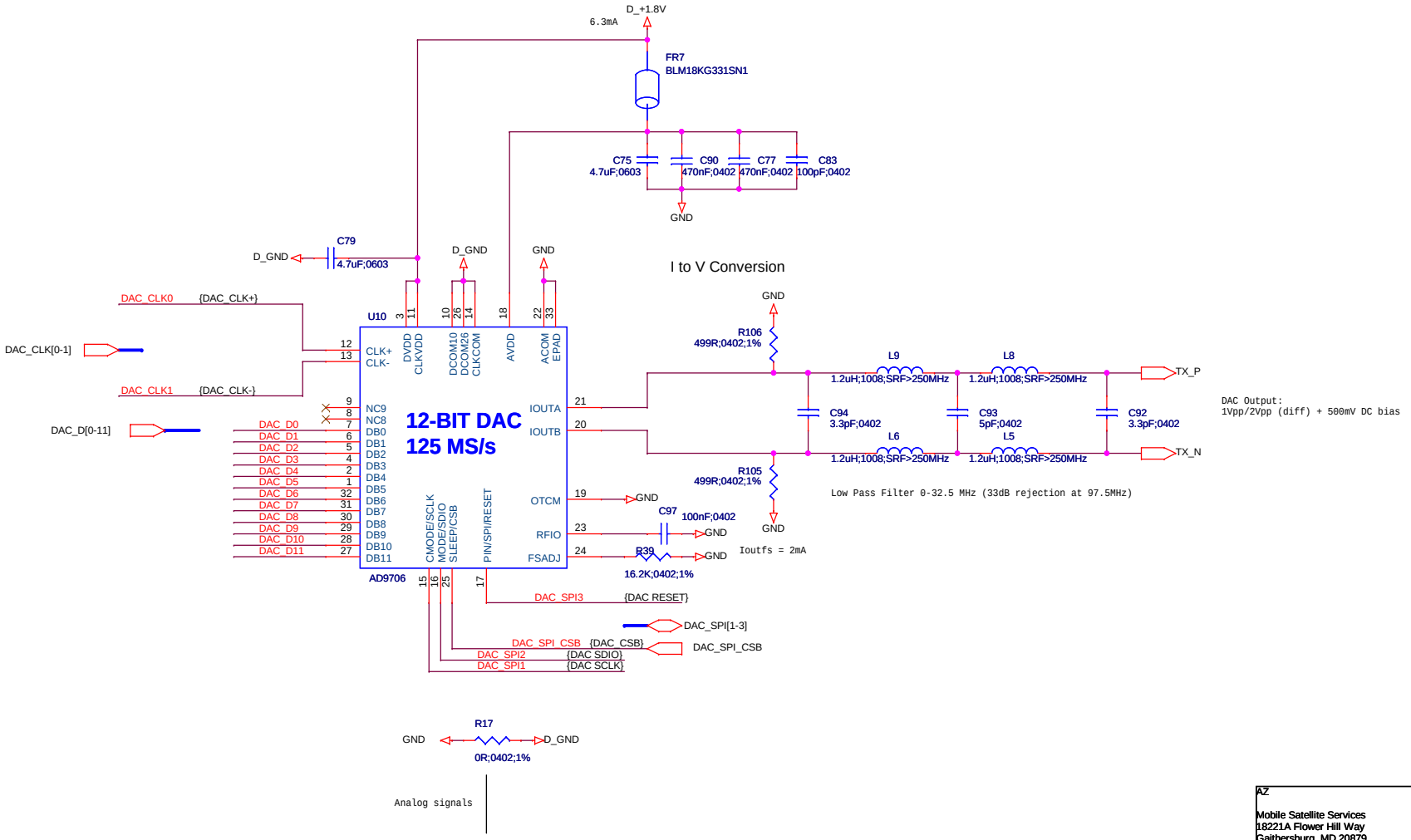
Title: COM-1700 / CLOCKS

Size	Document Number	Rev
B	Y12004	2

Date: Friday, June 14, 2013 Sheet 5 of 18

DAC (1 baseband channel)



AZ		
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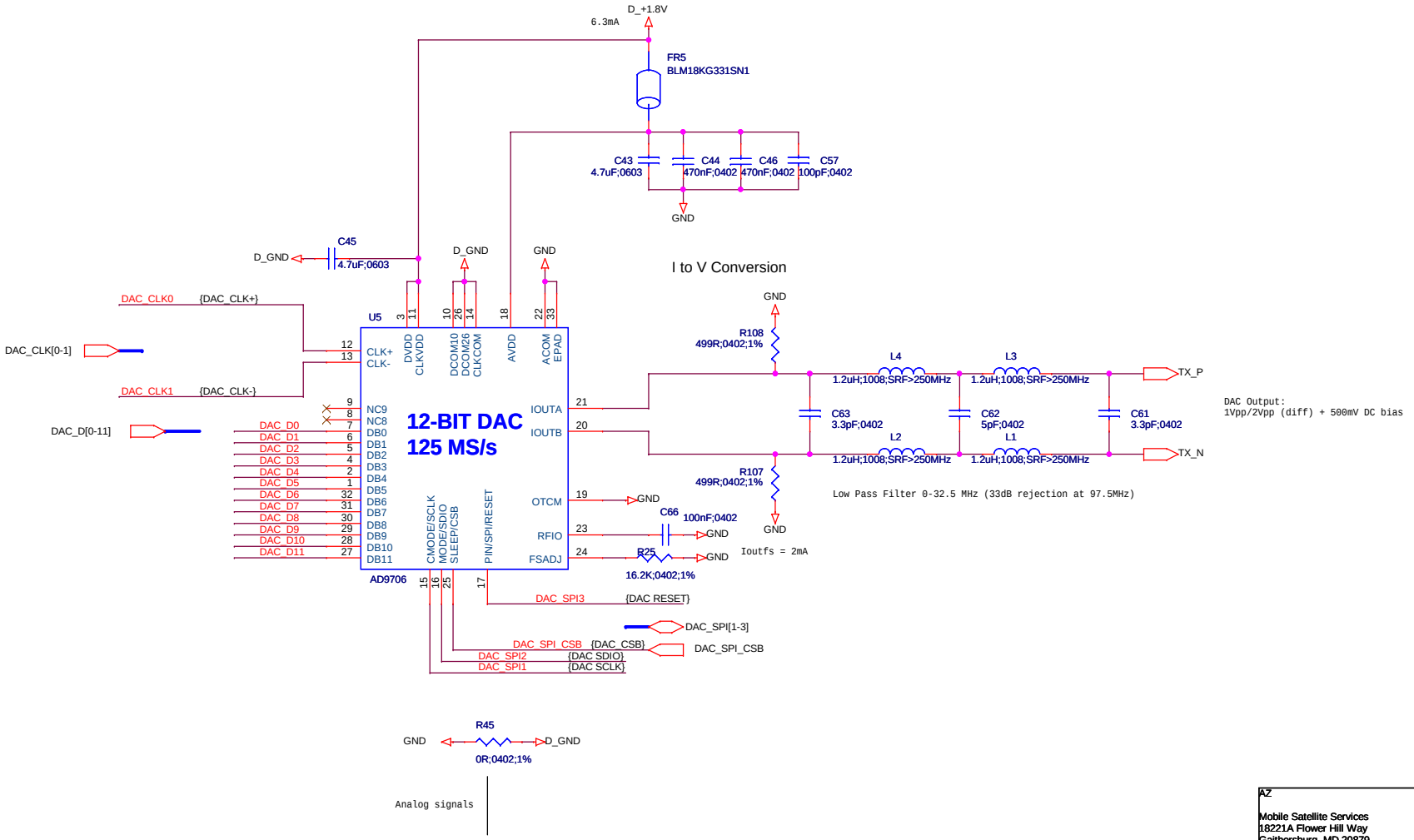
Title: COM-1700 / DAC		
Size: B	Document Number: Y12004	Rev: 2
Date: Wednesday, June 12, 2013	Sheet 6 of 18	

DAC (1 baseband channel)



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Title	COM-1700 / DAC	
Size B	Document Number Y12004	Rev 2
Date: Wednesday, June 12, 2013	Sheet 7 of 18	

CARD-EDGE RIGHT SIDE

FPGA (RE)CONFIGURATION

FPGA_DATA[0-9]

FPGA_PROG[1-3]

HIGH-SPEED LVDS I/Os

RIGHT_CONN_A[1-46]

RIGHT_CONN_B[1-34]

MONITORING & CONTROL

M&C_[1-2]

M&C_1 {RIGHT_RX}

M&C_2 {RIGHT_TX}

AK + AZ

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Title: COM-1700 / CONNECTORS

Size	Document Number	Rev
B	Y12004	1

Date: Wednesday, June 12, 2013 Sheet 8 of 18

FPGA (RE)CONFIGURATION & COMMS

FPGA LEFT SIDE, 3.3V I/O

FPGA_DATA[0-9]
- FPGA_DATA0 {D0}
- FPGA_DATA1 {D1}
- FPGA_DATA2 {D2}
- FPGA_DATA3 {D3}
- FPGA_DATA4 {D4}
- FPGA_DATA5 {D5}
- FPGA_DATA6 {D6}
- FPGA_DATA7 {D7}
- FPGA_DATA8 {CCLK/ALE}
- FPGA_DATA9 {RDWR_B/REB}

FPGA Programming

FPGA_PROG[1-5]
- FPGA_PROG1 {PROG_B}
- FPGA_PROG2 {CSI_B}
- FPGA_PROG3 {DONE}
- FPGA_PROG4 {INITB/WEB}
- FPGA_PROG5 {SUSPEND}

FPGA CONFIGURATION

D_+3.3V
- C26 470nF;0402
- C30 470nF;0402
- C177 470nF;0402
- C24 470nF;0402
- C22 4.7uF;0603

D_GND

D_+3.3V
- R6 4.7K;0402;1% FPGA_PROG1 {PROG_B}
- R18 330R;0402 FPGA_PROG3 {DONE}
- R9 4.7K;0402;1% FPGA_PROG4 {INITB/WEB}

Layout Note:
- Route UC_CTRL1 as 50ohm trace
- place termination 100Rs closest to FPGA

TP1 DONE

J8 — 87831-1420

1	GND1	Vref	2	D_+3.3V	
3	GND2	TMS	4	FPGA_JTAG_TMS	
5	GND3	TCK	6	FPGA_JTAG_TCK	
7	GND4	TDO	8	FPGA_JTAG_TDO	
9	GND5	TDI	10	FPGA_JTAG_TDI	
11	GND6	NC1	12		
13	GND7	NC2	14		

D_GND

FPGA JTAG header compatible with Xilinx 2x7 2mm connector

D_+3.3V — R19 10K;0402;1% — FPGA_JTAG_TCK

Slave SelectMAP Programming Configuration: D_GND, D_+3.3V

U4C

Supply
- VCCO_2_00 P9
- VCCO_2_01 R12
- VCCO_2_02 R6
- VCCO_2_03 U14
- VCCO_2_04 U4
- VCCO_2_05 U9

D_+3.3V

FPGA_PROG1	{PROG_B}	V2
FPGA_DATA8	{CCLK/ALE}	R15
FPGA_PROG2	{CSI_B}	T13
FPGA_DATA9	{RDWR_B/REB}	R8
FPGA_PROG3	{DONE}	V17
FPGA_PROG4	{INITB/WEB}	U3
FPGA_PROG5	{SUSPEND}	R16
		P13

D_+3.3V

FPGA_DATA0	{D0}	R13
FPGA_DATA1	{D1}	T14
FPGA_DATA2	{D2}	V14
FPGA_DATA3	{D3}	U5
FPGA_DATA4	{D4}	V5
FPGA_DATA5	{D5}	R3
FPGA_DATA6	{D6}	T3
FPGA_DATA7	{D7}	R5
	D_GND	T15
	D_+3.3V	N12

FPGA_JTAG_TCK		A17
FPGA_JTAG_TDI		D15
FPGA_JTAG_TDO		D16
FPGA_JTAG_TMS		B18

RIGHT_CONN_B27	{RB13N}	T10
RIGHT_CONN_B28	{RB13P}	R10
RIGHT_CONN_B25	{RB12N}	V10
RIGHT_CONN_B26	{RB12P}	U10
RIGHT_CONN_B16	{RB8N}	T8
RIGHT_CONN_B17	{RB8P}	R8
CLKREF25		V9
SERIAL_RX4		T9

FPGA Bank 2

TCK, TDI, TDO, TMS — JTAG

Global Clocks
- IO_L29N_GCLK2_2
- IO_L29P_GCLK3_2
- IO_L30N_GCLK0_USERCCLK_2
- IO_L30P_GCLK1_D13_2
- IO_L31N_GCLK30_D15_2
- IO_L31P_GCLK31_D14_2
- IO_L32N_GCLK28_2
- IO_L32P_GCLK29_2

Not with Differential Pair
- IO_L65N_CSO_B_2
- IO_L13N_D10_2

V3	SERIAL_RX1	
P12	D_CNTRL2	

XC6SLX45-L1CSG324

V16	D_CNTRL5	
U16	D_CNTRL4	
V15	SERIAL_RX3	
U15	D_CNTRL3	
V13	RIGHT_CONN_A45	{RA23N}
U13	RIGHT_CONN_A46	{RA23P}
N11	SERIAL_RX2	
M11	D_CNTRL1	
T11	RIGHT_CONN_B32	{RB15N}
R11	RIGHT_CONN_B33	{RB15P}
V12	RIGHT_CONN_A43	{RA22N}
T12	RIGHT_CONN_A44	{RA22P}
P11	RIGHT_CONN_A41	{RA21N}
N10	RIGHT_CONN_A42	{RA21P}
N9	RIGHT_CONN_B23	{RB11N}
M10	RIGHT_CONN_B24	{RB11P}
V11	RIGHT_CONN_B29	{RB14N}
U11	RIGHT_CONN_B30	{RB14P}
N8	RIGHT_CONN_B21	{RB10N}
M8	RIGHT_CONN_B22	{RB10P}
V8	RIGHT_CONN_B14	{RB7N}
U8	RIGHT_CONN_B15	{RB7P}
V7	RIGHT_CONN_B8	{RB4N}
U7	RIGHT_CONN_B9	{RB4P}
P8	RIGHT_CONN_B18	{RB9N}
N7	RIGHT_CONN_B19	{RB9P}
V6	RIGHT_CONN_B3	{RB2N}
T6	RIGHT_CONN_B4	{RB2P}
T7	RIGHT_CONN_B10	{RB5N}
R7	RIGHT_CONN_B11	{RB5P}
P7	RIGHT_CONN_B12	{RB6N}
N6	RIGHT_CONN_B13	{RB6P}
V4	RIGHT_CONN_B1	{RB1N}
T4	RIGHT_CONN_B2	{RB1P}
P6	RIGHT_CONN_B6	{RB3N}
N5	RIGHT_CONN_B7	{RB3P}

CLKREF25 — Internal frequency reference (from LAN PHY crystal)

D_CNTRL[1-5] — Digital controls for an external transceiver

HIGH-SPEED LVDS I/Os

RIGHT_CONN_B[1-33]

RIGHT_CONN_A[41-46]

RS422 RX

SERIAL_RX[1-4]

Sensitive Input Clock Traces

- FPGA_DATA8 {CCLK/ALE} — C41 C-OPEN;0402 — D_GND
- FPGA_JTAG_TCK — C42 C-OPEN;0402 — D_GND

Layout Note:
Place clock capacitors close to the FPGA

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Title: COM-1700 / FPGA BANK2

Size: B | Document Number: Y12004 | Rev: 1

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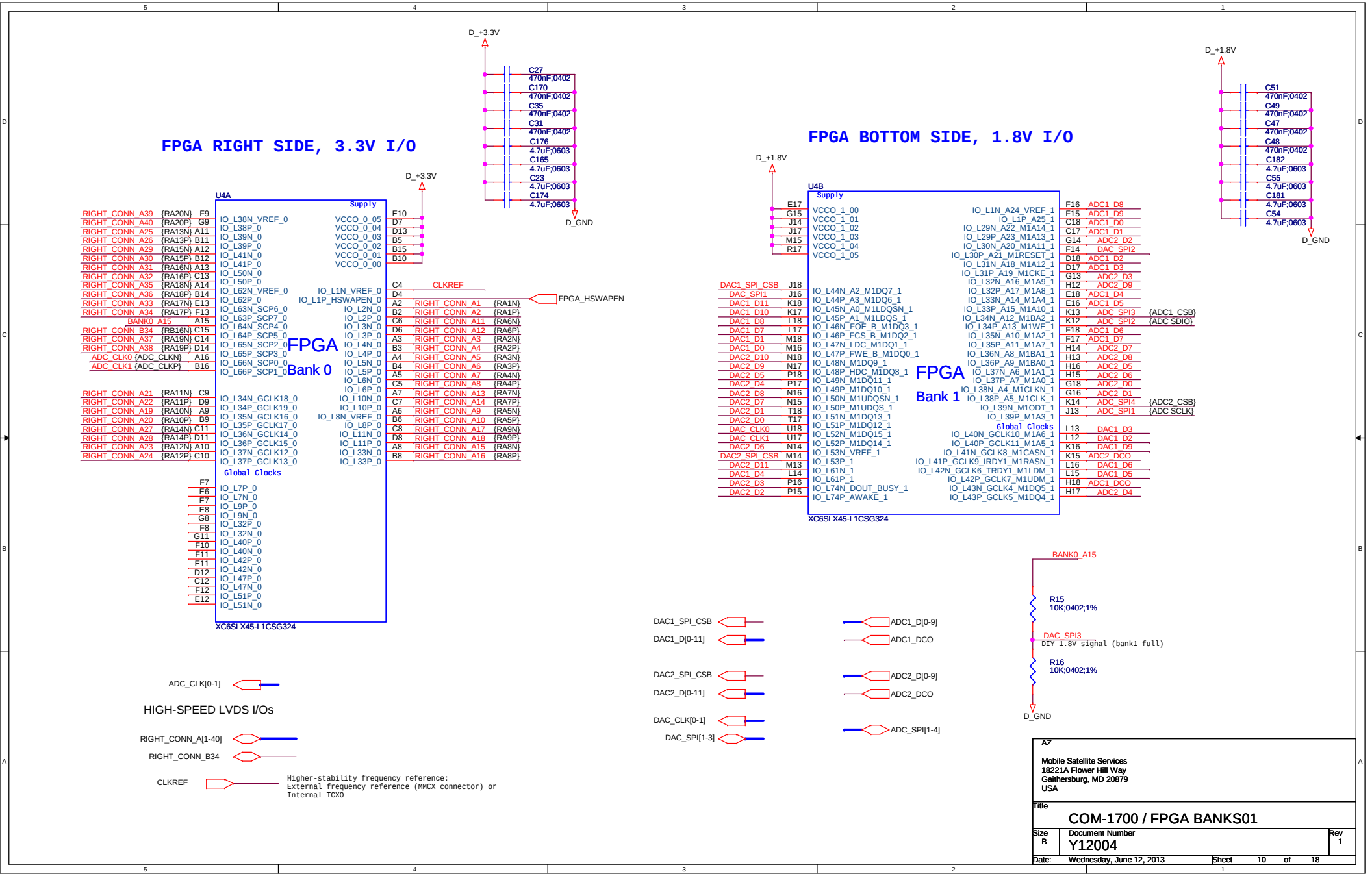
FPGA RIGHT SIDE, 3.3V I/O
FPGA BOTTOM SIDE, 1.8V I/O
U4A
U4B
FPGA
Bank 0
FPGA
Bank 1
XC6SLX45-L1CSG324
XC6SLX45-L1CSG324
D_+3.3V
D_+1.8V
D_GND
C27 470nF;0402
C170 470nF;0402
C35 470nF;0402
C31 470nF;0402
C176 4.7uF;0603
C165 4.7uF;0603
C23 4.7uF;0603
C174 4.7uF;0603
C51 470nF;0402
C49 470nF;0402
C47 470nF;0402
C48 470nF;0402
C182 4.7uF;0603
C55 4.7uF;0603
C181 4.7uF;0603
C54 4.7uF;0603
FPGA_HSWAPEN
CLKREF
BANK0_A15
R15 10K;0402;1%
R16 10K;0402;1%
DAC_SPI3
DIY 1.8V signal (bank1 full)
ADC_CLK[0-1]
HIGH-SPEED LVDS I/Os
RIGHT_CONN_A[1-40]
RIGHT_CONN_B34
CLKREF
Higher-stability frequency reference:
External frequency reference (MMCX connector) or
Internal TCXO
DAC1_SPI_CSB
DAC1_D[0-11]
DAC2_SPI_CSB
DAC2_D[0-11]
DAC_CLK[0-1]
DAC_SPI[1-3]
ADC1_D[0-9]
ADC1_DCO
ADC2_D[0-9]
ADC2_DCO
ADC_SPI[1-4]
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Title
COM-1700 / FPGA BANKS01
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FPGA TOP SIDE, 2.5V I/O

LAN_CTRL_[1-5]
LAN_TX_[1-6]
LAN_RX_[1-6]
USB_DATA[0-7]
USB_CTRL[0-3]
USB_REFCLK60

D_+2.5V
C15 470nF;0402
C152 470nF;0402
C16 470nF;0402
C151 470nF;0402
C14 470nF;0402
C150 470nF;0402
C13 4.7uF;0603
C149 4.7uF;0603
C9 4.7uF;0603
C148 4.7uF;0603
D_GND

U4D

	J7	IO_L47P_M3A0_3	Supply	R2	
	J6	IO_L47N_M3A1_3	VCCO_3_05	M4	
	H5	IO_L49N_M3A2_3	VCCO_3_04	J5	
SERIAL_TX4	L7	IO_L45P_M3A3_3	VCCO_3_03	J2	
Layout: sensitive trace USB_REFCLK60	F3	IO_L51N_M3A4_3	VCCO_3_02	G4	
	H4	IO_L44P_GCLK21_M3A5_3	VCCO_3_01	E2	
	H3	IO_L44N_GCLK20_M3A6_3	VCCO_3_00		
	H6	IO_L49P_M3A7_3			
USB_DATA7	D2	IO_L52P_M3A8_3	IO_L37P_M3DQ0_3	L2	SERIAL_TX_EN
USB_DATA3	D1	IO_L52N_M3A9_3	IO_L37N_M3DQ1_3	L1	SERIAL_RX_EN
USB_CTRL0 {NXT}	F4	IO_L51P_M3A10_3	IO_L38P_M3DQ2_3	K2	
USB_DATA4	D3	IO_L54N_M3A11_3	IO_L38N_M3DQ3_3	K1	
	G6	IO_L53N_M3A12_3	IO_L41P_GCLK27_M3DQ4_3	H2	
USB_CTRL1 {DIR}	F6	IO_L55P_M3A13_3	IO_L41N_GCLK26_M3DQ5_3	H1	
USB_CTRL2 {STP}	F5	IO_L55N_M3A14_3	IO_L40P_M3DQ6_3	J3	
			IO_L40N_M3DQ7_3	J1	
	G3	IO_L46P_M3CLK_3	IO_L36P_M3DQ8_3	M3	LAN_CTRL_2 {INT_N}
	G1	IO_L46N_M3CLKN_3	IO_L36N_M3DQ9_3	M1	LAN_CTRL_5 {MDIO}
	H7	IO_L53P_M3CKE_3	IO_L35P_M3DQ10_3	N2	LAN_TX_5 {TXD2}
SERIAL_TX2	L4		IO_L35N_M3DQ11_3	N1	LAN_TX_6 {TXD3}
SERIAL_TX1	L3	IO_L39P_M3LDQS_3	IO_L33P_M3DQ12_3	T2	LAN_RX_4 {RXD1}
LAN_RX_2 {RX_DV}	P2	IO_L39N_M3LDQSN_3	IO_L33N_M3DQ13_3	T1	LAN_RX_5 {RXD2}
LAN_RX_3 {RXD0}	P1	IO_L34P_M3UDQS_3	IO_L32P_M3DQ14_3	U2	LAN_RX_6 {RXD3}
		IO_L34N_M3UDQSN_3	IO_L32N_M3DQ15_3	U1	LAN_TX_2 {TX_EN}
LAN_CTRL_1 {CLK125_NDO}	L5			N3	LAN_TX_3 {TXD0}
	K5	IO_L43P_GCLK23_M3RASN_3	IO_L1N_VREF_3	N4	LAN_CTRL_4 {MDC}
	E3	IO_L43N_GCLK22_IRDY2_M3CASN_3	IO_L1P_3	P3	LAN_TX_1 {GTX_CLK}
USB_DATA1	F2	IO_L50P_M3WE_3	IO_L2N_3	P4	LAN_TX_4 {TXD1}
USB_CTRL3 {RESETB}	F1	IO_L48P_M3BA0_3	IO_L2P_3	M5	LAN_CTRL_3 {RESET_N}
	E1	IO_L48N_M3BA1_3	IO_L31N_VREF_3	L6	SERIAL_TX3
USB_DATA0	K3	IO_L50N_M3BA2_3	IO_L31P_3	E4	USB_DATA2
Layout: sensitive trace LAN_RX_1 {RX_CLK}	K4	IO_L42N_GCLK24_M3LDM_3	IO_L54P_M3RESET_3	C1	USB_DATA5
		IO_L42P_GCLK25_TRDY2_M3UDM_3	IO_L83N_VREF_3	C2	USB_DATA6
	K6		IO_L83P_3		
		IO_L45N_M3ODT_3			

FPGA
Bank 3
XC6SLX45-L1CSG324

D_+2.5V

Layout: sensitive trace +
Place pad near FPGA pin (to filter glitches if any)

LAN_RX_1 {RX_CLK} C17 C-OPEN;0402
D_GND

SERIAL_TX[1-4]

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Title: COM-1700 / FPGA BANK3

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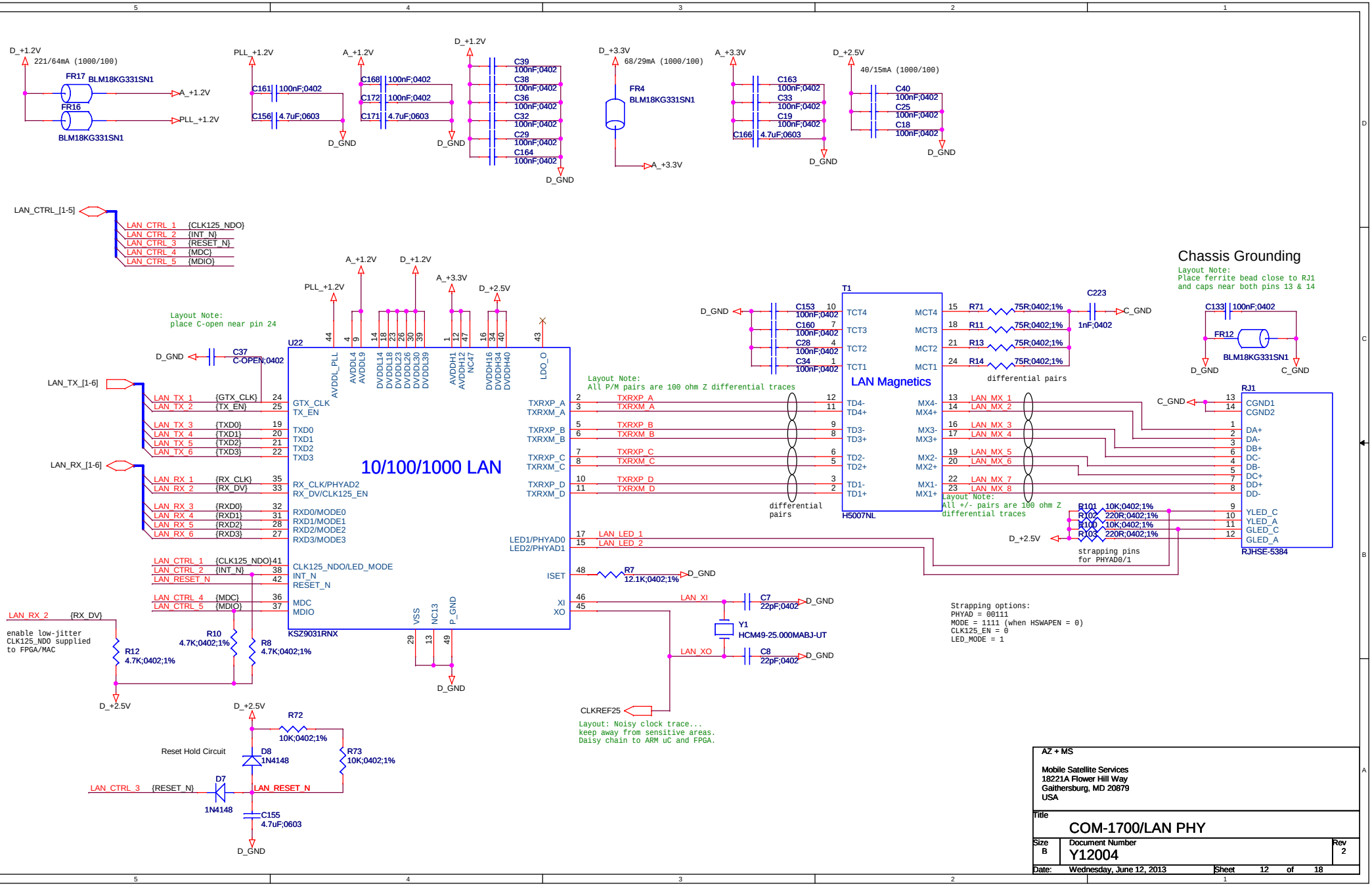

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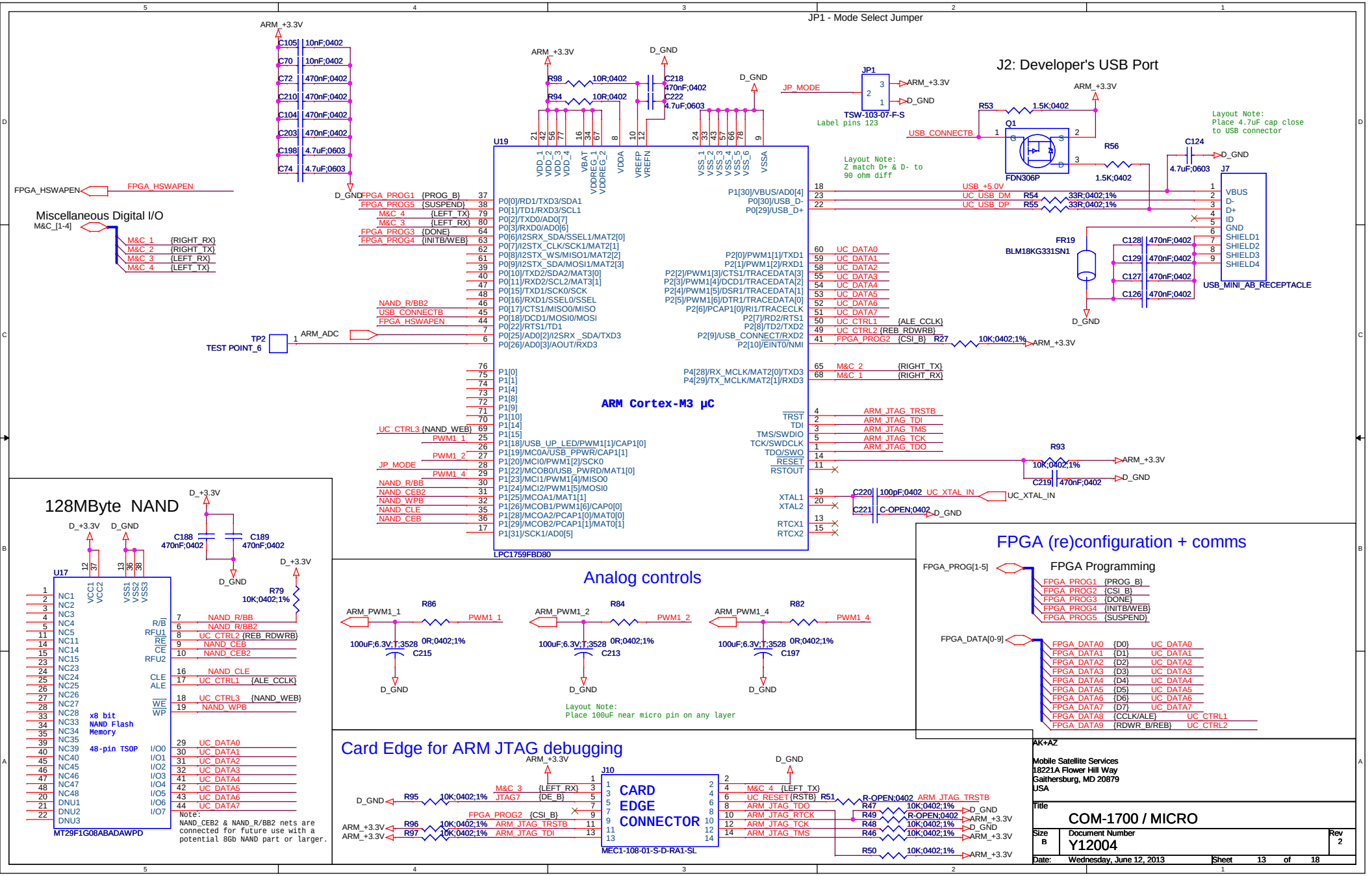
Title
COM-1700/LAN PHY

Size	Document Number	Rev
B	Y12004	2

Date: Wednesday, June 12, 2013 Sheet 12 of 18


JP1 - Mode Select Jumper
J2: Developer's USB Port
Miscellaneous Digital I/O
ARM Cortex-M3 µC
LPC1759FBD80
128MByte NAND
MT29F1G08ABADAWPD
Analog controls
FPGA (re)configuration + comms
FPGA Programming
Card Edge for ARM JTAG debugging
CARD EDGE CONNECTOR
MEC1-108-01-S-D-RA1-SL
TSW-103-07-F-S
FDN306P
BLM18KG331SN1
USB_MINI_AB_RECEPTACLE
TEST POINT_6
Layout Note:
Place 4.7uF cap close to USB connector
Layout Note:
Z match D+ & D- to 90 ohm diff
Layout Note:
Place 100uF near micro pin on any layer
Note:
NAND_CEB2 & NAND_R/BB2 nets are connected for future use with a potential 8Gb NAND part or larger.
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+5V, internal protection

Green Terminal Block

OPERATIONAL RANGE: 4.75 - 5.5V

Filter

Reverse Voltage Protection

Transient Voltage Suppression

Over Voltage Protection (5.85V, 1.5A)

Layout Note:
FR4, Q1, Q2 & Q4 must be placed and routed for a high current throughput.

J3
BATT+
BATT-
P02ECH381RH-E
TB +5.0V
R61
R-OPEN;Solder Bridge
FR15
BLM18KG331SN1
R60
R-OPEN;Solder Bridge
D_GND
Layout Note: 0 Ohm and R-OPEN resistors share 1 pad
D_+3.3V
ARM_+3.3V
Vin_revp
Q2
FDC658AP
-30V, -4A, 50mOhm
Vin_revp = reverse voltage protection, but no over-voltage protection. Best used for FPGA 1.2 Vccint and DDR2 +1.8V since FAN2106 tolerates up to 24V.
D6
SMBJ5.0A-E3
R3
499R;0402;1%
R4
10K;0402;1%
D1
MM5Z5V1
Q4
FMMT718TA
Q3
FMMT718TA
R70
1K;0402;1%
Layout Note:
move TVS as far down the trace as possible (away from the terminal block)

REGULATED 3.3V

NCP1599MNTWG DC/DC converter:
3A max peak output current
1MHz switching
Layout Note:
Place Vin caps as close as possible to Vcc and GND pins
U16
NCP1599
3A DC/DC
Converter
VCCP
VCC
LX
COMP
GND PAD
FB
VREF=0.8V
NCP1599MNTWG
L17
6.8uH;3.1A
Ityp = 1160A Vout = 3.28V
R67
R-OPEN;Solder Bridge
D_+3.3V
solder during post-assembly tests
Layout Note: R67 and R44 resistors share 1 pad (optional)
R75
31.6K;0402;1%
R76
10K;0402;1%
R74
4.7K;0402;1%
C159
4.7nF;0402
C154
10nF;0402
C157
4.7uF;0603
C158
4.7uF;0603
C146
220uF;4V;T;3217
C144
4.7uF;0603
C142
470nF;0402
D_GND

D_+1V
C183 470nF;0402
C167 470nF;0402
C173 470nF;0402
C184 470nF;0402
C180 470nF;0402
C175 470nF;0402
C179 4.7uF;0603
C185 4.7uF;0603
C187 4.7uF;0603
C186 4.7uF;0603
D_GND
D_+2.5V
FR3
BLM18KG331SN1
C50 470nF;0402
C52 470nF;0402
C169 470nF;0402
C162 470nF;0402
C178 470nF;0402
C21 4.7uF;0603
C11 4.7uF;0603
C12 4.7uF;0603
C10 4.7uF;0603
D_GND

FPGA POWER

D_+1V
U4E
VCCINT_10 VCCINT_09 VCCINT_08 VCCINT_07 VCCINT_06 VCCINT_05 VCCINT_04 VCCINT_03 VCCINT_02 VCCINT_01 VCCINT_00
VCCAUX_11 VCCAUX_10 VCCAUX_09 VCCAUX_08 VCCAUX_07 VCCAUX_06 VCCAUX_05 VCCAUX_04 VCCAUX_03 VCCAUX_02 VCCAUX_01 VCCAUX_00
GND_36 GND_35 GND_34 GND_33 GND_32 GND_31 GND_30 GND_29 GND_28 GND_27 GND_26 GND_25 GND_24 GND_23 GND_22 GND_21 GND_20 GND_19 GND_18 GND_17 GND_16 GND_15 GND_14 GND_13 GND_12 GND_11 GND_10 GND_09 GND_08 GND_07 GND_06 GND_05 GND_04 GND_03 GND_02 GND_01 GND_00
FPGA Supply
XC6SLX45-L1CSG324
D_GND

PCB Mounting Holes

H3 H2 H1 H4

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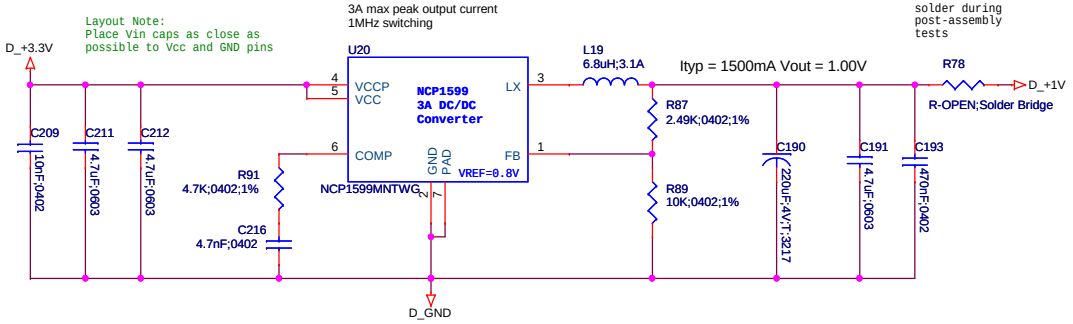
FPGA Vccint 1V 3A



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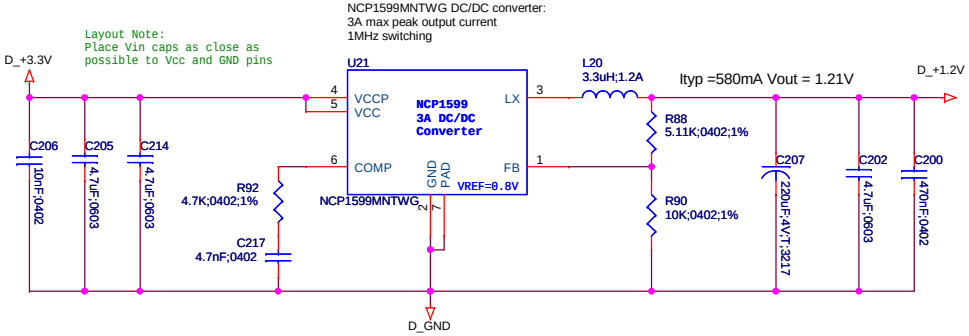

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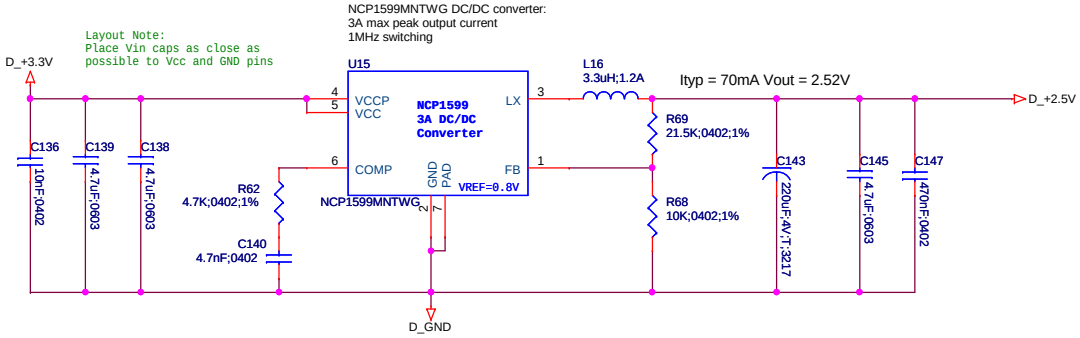
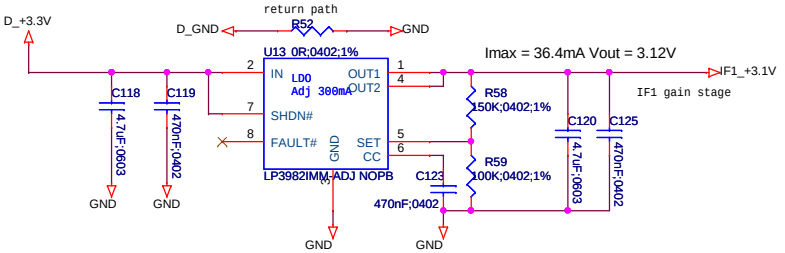
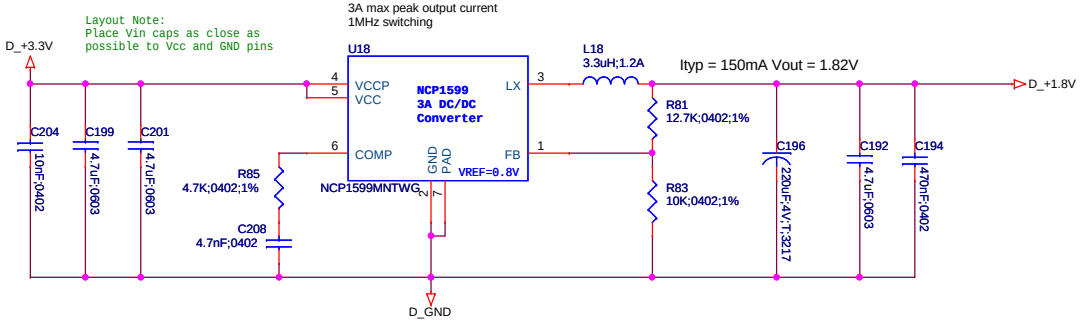




FPGA 1.8V 3A



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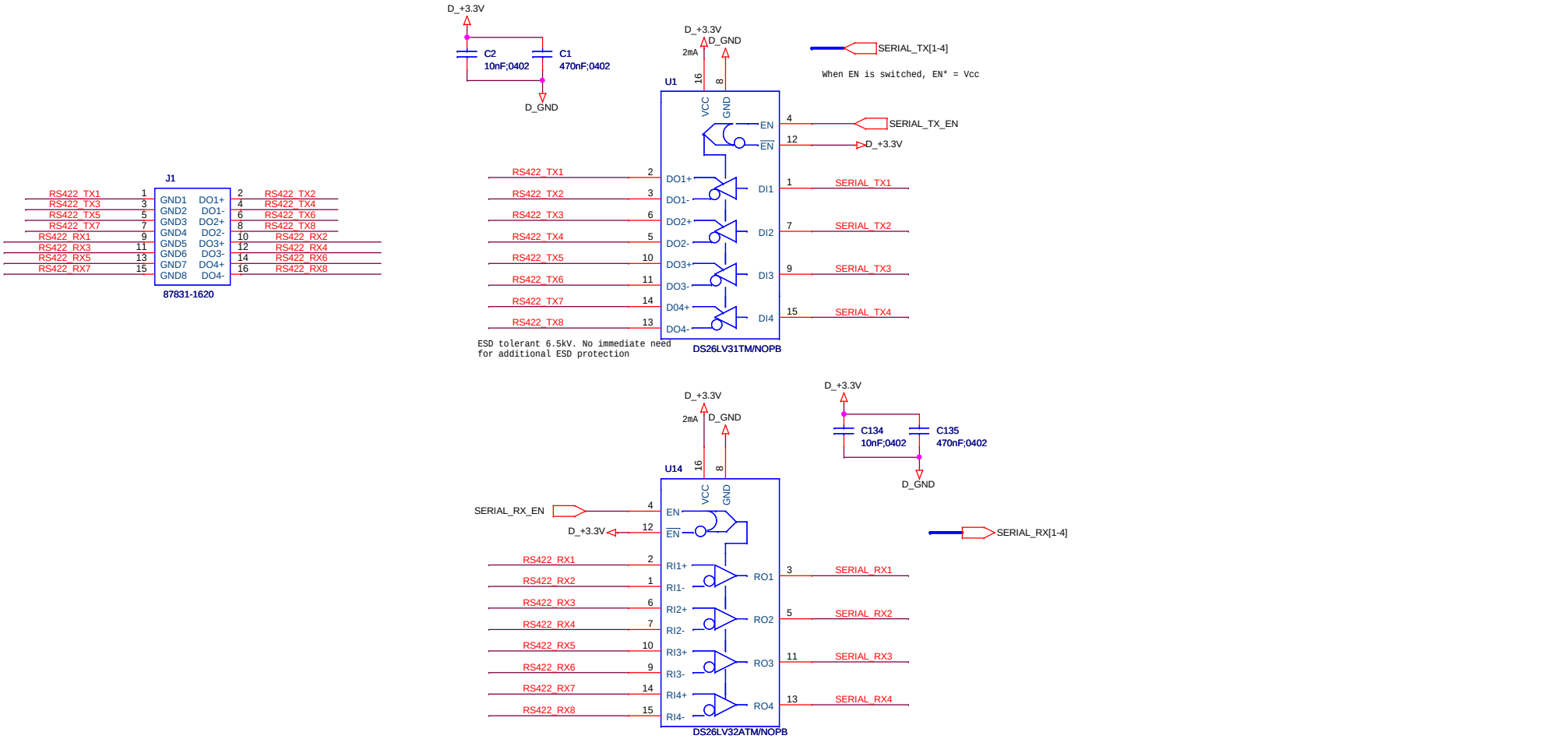
RS-422/RS-485 DRIVERS



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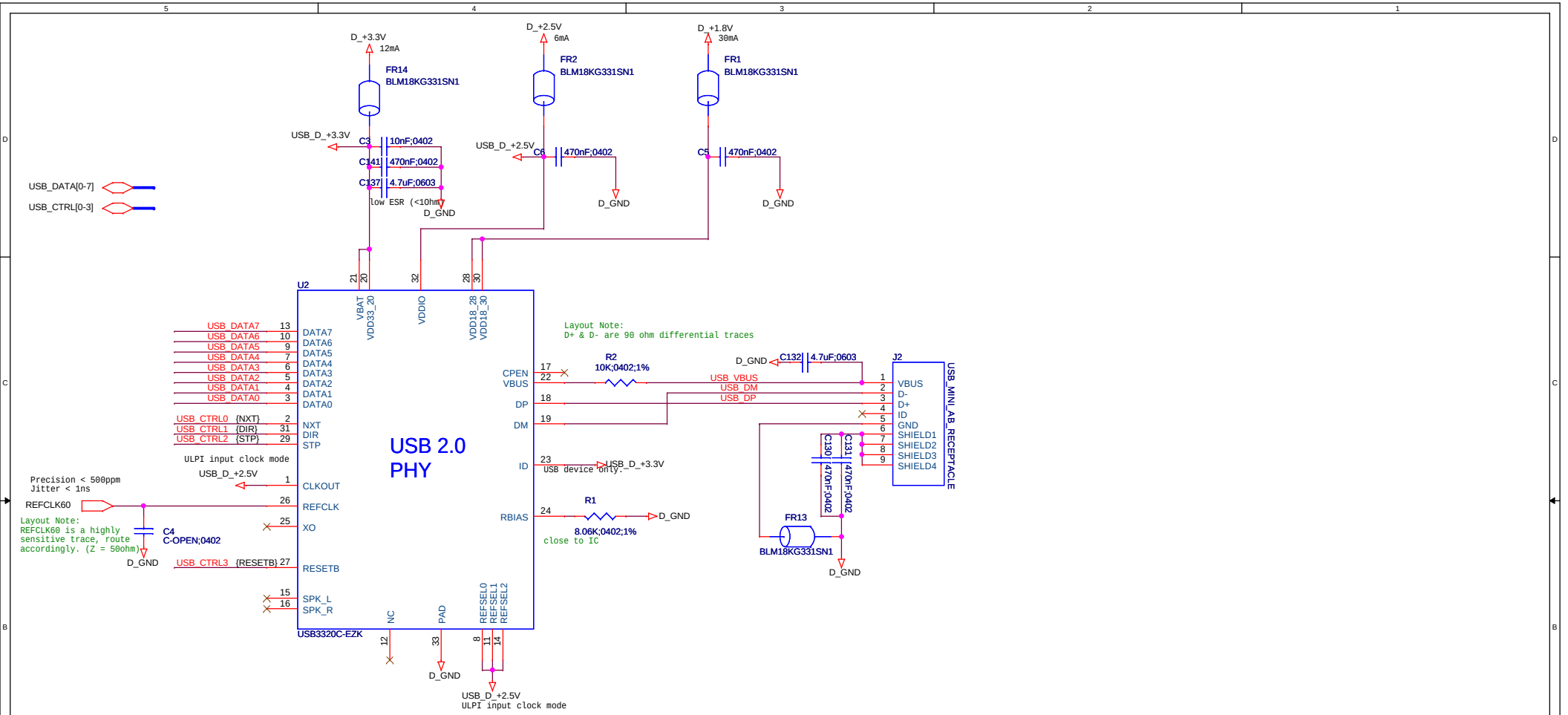

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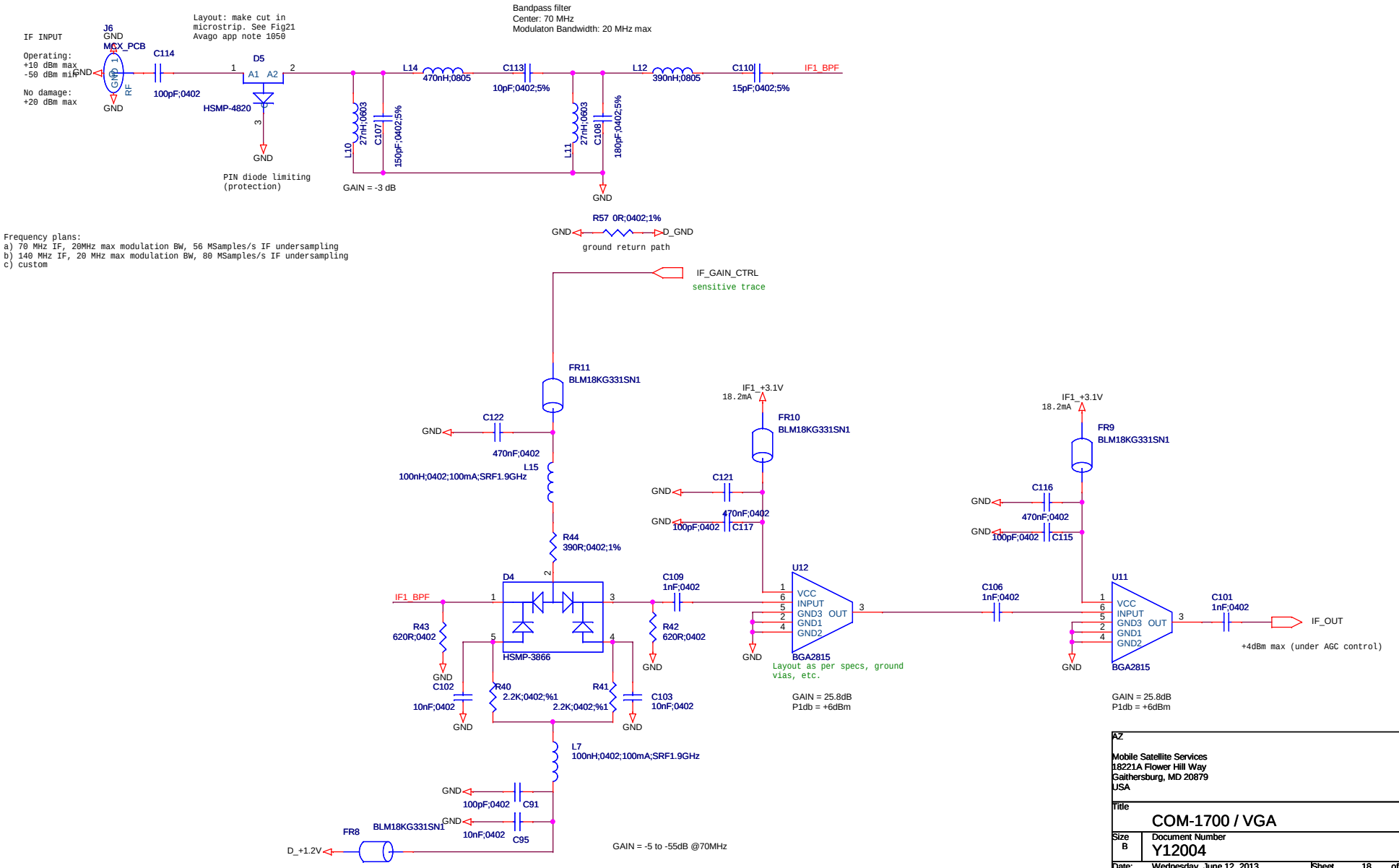
BAND-PASS FILTER



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