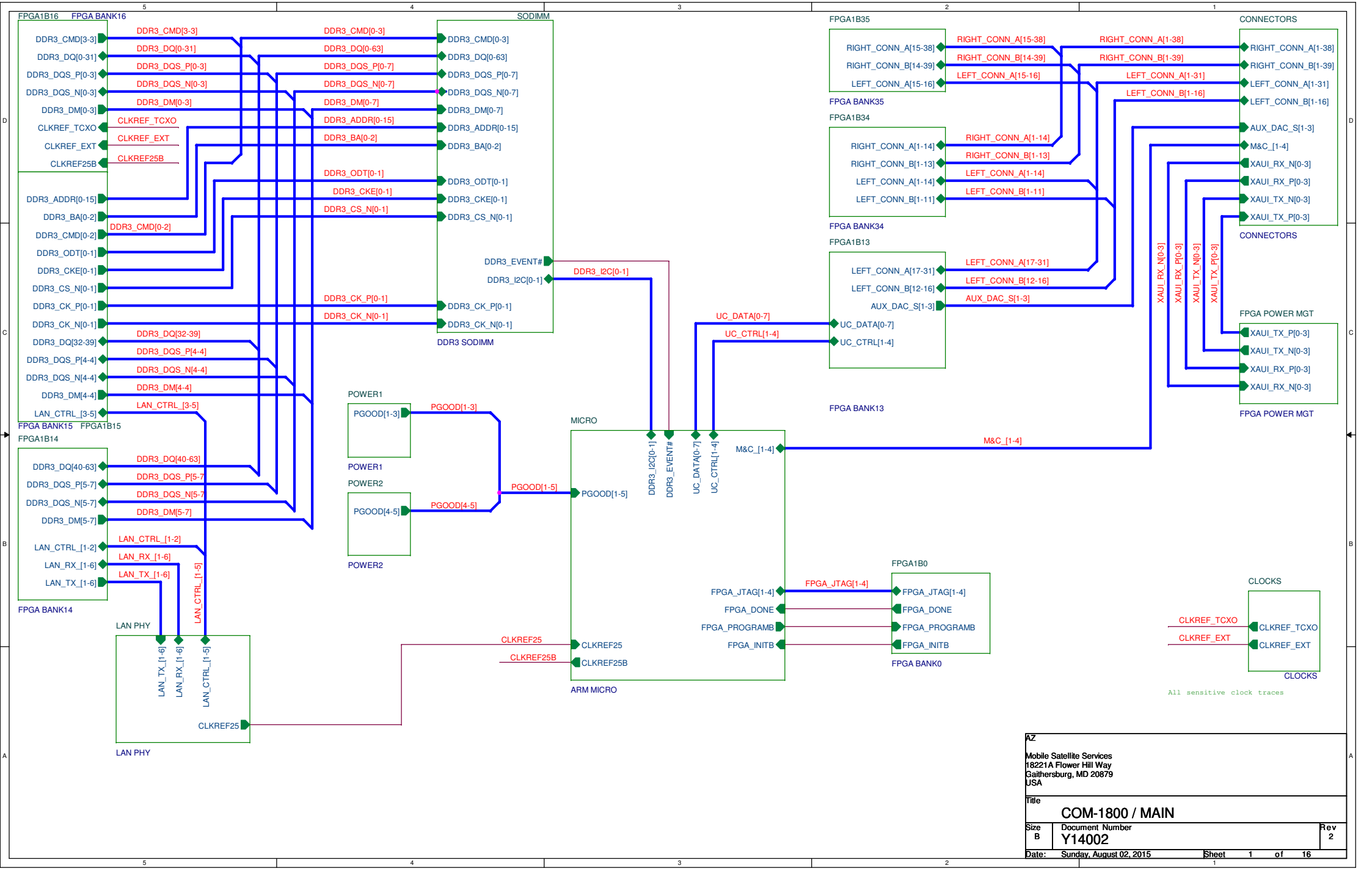

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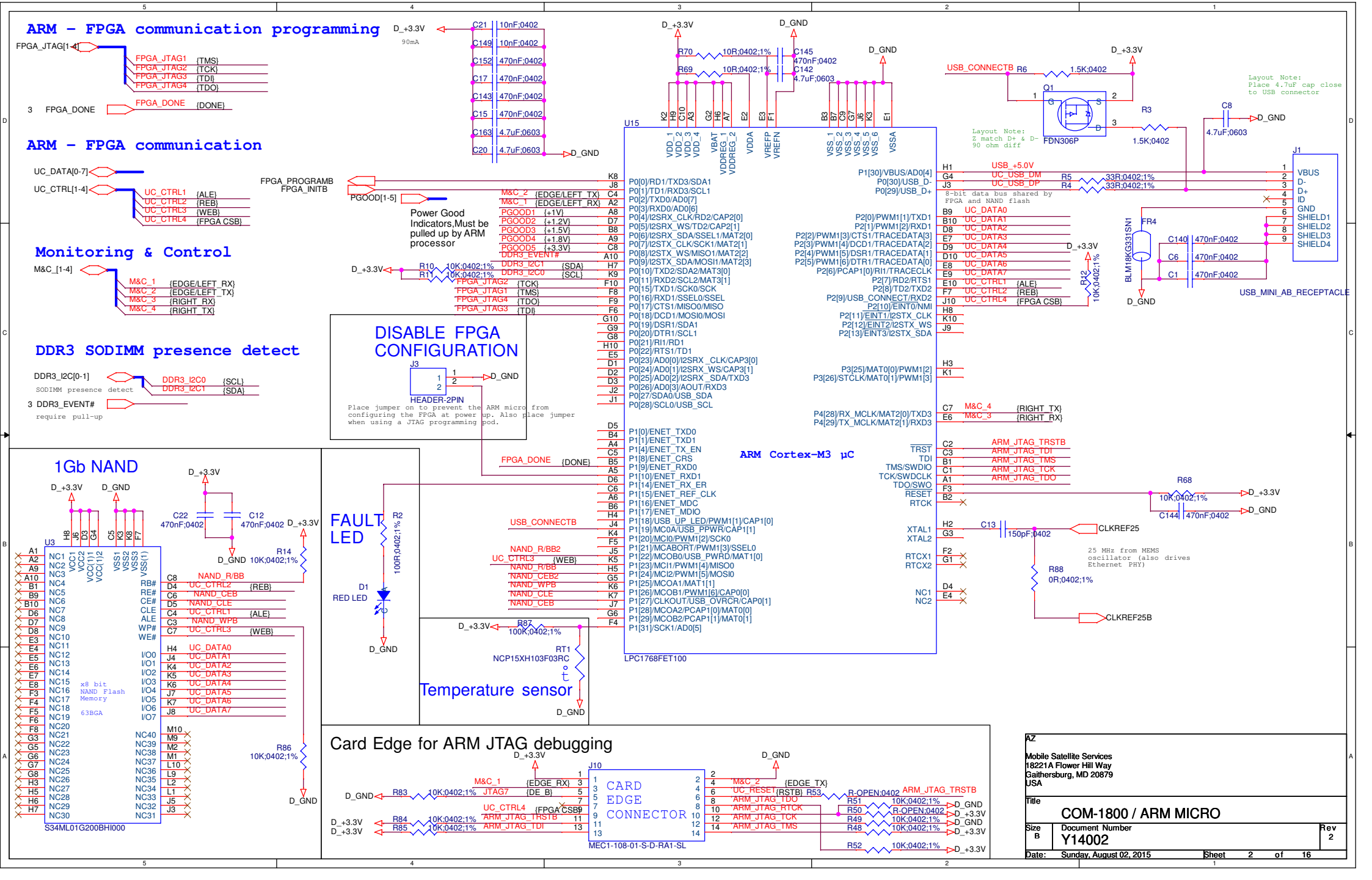
ARM – FPGA communication programming
FPGA_JTAG[1-4]
FPGA_JTAG1 {TMS}
FPGA_JTAG2 {TCK}
FPGA_JTAG3 {TDI}
FPGA_JTAG4 {TDO}
3 FPGA_DONE
FPGA_DONE {DONE}
ARM – FPGA communication
UC_DATA[0-7]
UC_CTRL[1-4]
UC_CTRL1 {ALE}
UC_CTRL2 {REB}
UC_CTRL3 {WEB}
UC_CTRL4 {FPGA CSB}
Monitoring & Control
M&C_[1-4]
M&C_1 {EDGE/LEFT_RX}
M&C_2 {EDGE/LEFT_TX}
M&C_3 {RIGHT_RX}
M&C_4 {RIGHT_TX}
DDR3 SODIMM presence detect
DDR3_I2C[0-1]
SODIMM presence detect
DDR3_I2C0 {SCL}
DDR3_I2C1 {SDA}
3 DDR3_EVENT#
require pull-up
1Gb NAND
S34ML01G200BHI000
x8 bit NAND Flash Memory
63BGA
FAULT LED
RED LED
Temperature sensor
NCP15XH103F03RC
DISABLE FPGA CONFIGURATION
HEADER-2PIN
Place jumper on to prevent the ARM micro from configuring the FPGA at power up. Also place jumper when using a JTAG programming pod.
ARM Cortex-M3 µC
LPC1768FET100
Power Good Indicators,Must be pulled up by ARM processor
FPGA_PROGRAMB
FPGA_INITB
PGOOD[1-5]
USB_CONNECTB
FDN306P
USB_MINI_AB_RECEPTACLE
Layout Note: Place 4.7uF cap close to USB connector
Layout Note: Z match D+ & D- 90 ohm diff
8-bit data bus shared by FPGA and NAND flash
25 MHz from MEMS oscillator (also drives Ethernet PHY)
CLKREF25
CLKREF25B
Card Edge for ARM JTAG debugging
CARD EDGE CONNECTOR
MEC1-108-01-S-D-RA1-SL
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COM-1800 / ARM MICRO
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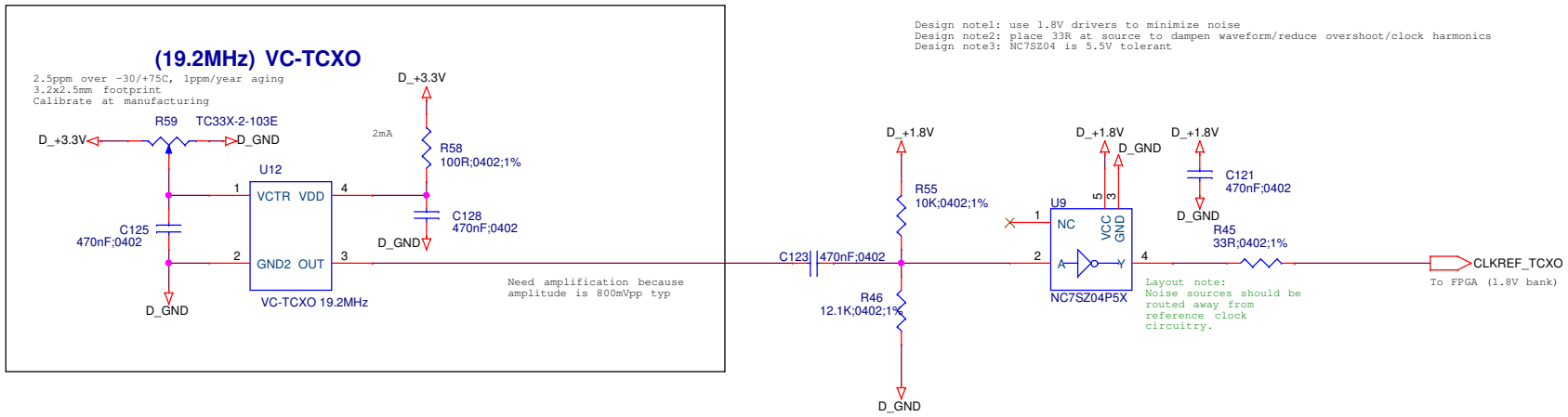
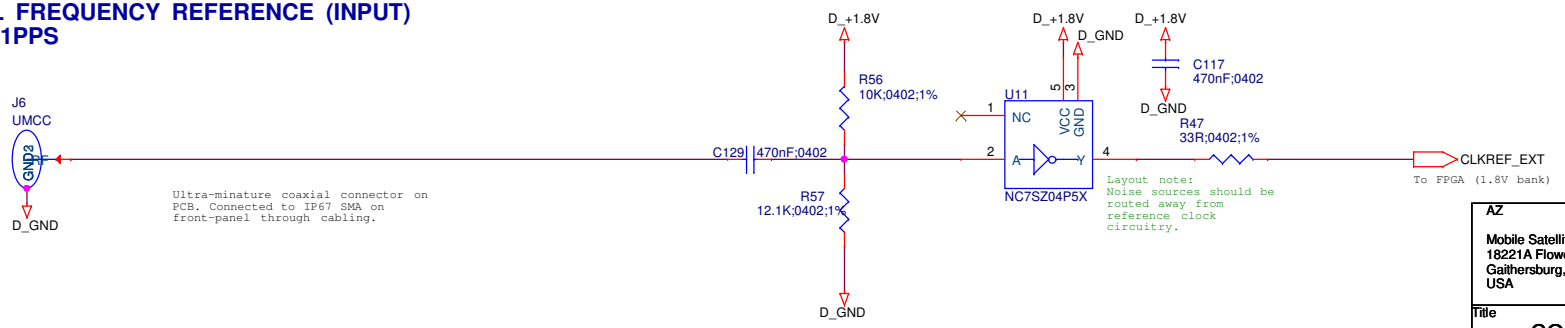


EXTERNAL FREQUENCY REFERENCE (INPUT)
10 MHz or 1PPS



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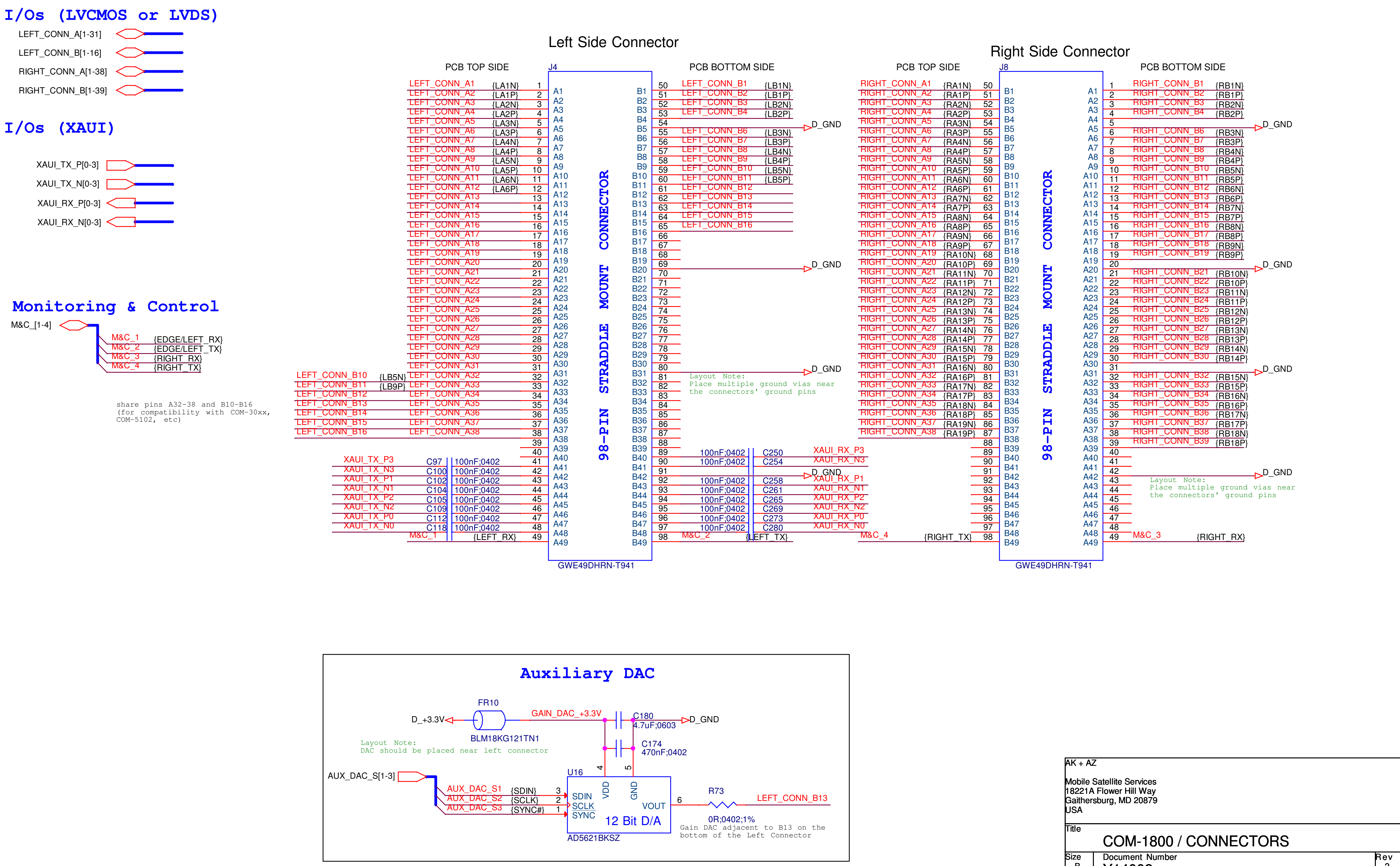
I/Os (LVCMOS or LVDS)
LEFT_CONN_A[1-31]
LEFT_CONN_B[1-16]
RIGHT_CONN_A[1-38]
RIGHT_CONN_B[1-39]
I/Os (XAUI)
XAUI_TX_P[0-3]
XAUI_TX_N[0-3]
XAUI_RX_P[0-3]
XAUI_RX_N[0-3]
Monitoring & Control
M&C_[1-4]
M&C_1 {EDGE/LEFT_RX}
M&C_2 {EDGE/LEFT_TX}
M&C_3 {RIGHT_RX}
M&C_4 {RIGHT_TX}
share pins A32-38 and B10-B16
(for compatibility with COM-30xx,
COM-5102, etc)
Left Side Connector
PCB TOP SIDE
J4
PCB BOTTOM SIDE
98-PIN STRADDLE MOUNT CONNECTOR
GWE49DHRN-T941
LEFT_CONN_B10 {LB5N}
LEFT_CONN_B11 {LB9P}
LEFT_CONN_B12
LEFT_CONN_B13
LEFT_CONN_B14
LEFT_CONN_B15
LEFT_CONN_B16
D_GND
Layout Note:
Place multiple ground vias near
the connectors' ground pins
XAUI_TX_P3 C97 100nF;0402
XAUI_TX_N3 C100 100nF;0402
XAUI_TX_P1 C102 100nF;0402
XAUI_TX_N1 C104 100nF;0402
XAUI_TX_P2 C105 100nF;0402
XAUI_TX_N2 C109 100nF;0402
XAUI_TX_P0 C112 100nF;0402
XAUI_TX_N0 C118 100nF;0402
M&C_1 {LEFT_RX}
100nF;0402 C250 XAUI_RX_P3
100nF;0402 C254 XAUI_RX_N3
100nF;0402 C258 XAUI_RX_P1
100nF;0402 C261 XAUI_RX_N1
100nF;0402 C265 XAUI_RX_P2
100nF;0402 C269 XAUI_RX_N2
100nF;0402 C273 XAUI_RX_P0
100nF;0402 C280 XAUI_RX_N0
M&C_2 {LEFT_TX}
Right Side Connector
PCB TOP SIDE
J8
PCB BOTTOM SIDE
98-PIN STRADDLE MOUNT CONNECTOR
GWE49DHRN-T941
M&C_4 {RIGHT_TX}
M&C_3 {RIGHT_RX}
D_GND
Layout Note:
Place multiple ground vias near
the connectors' ground pins
Auxiliary DAC
FR10
D_+3.3V
BLM18KG121TN1
GAIN_DAC_+3.3V
C180
4.7uF;0603
D_GND
C174
470nF;0402
Layout Note:
DAC should be placed near left connector
AUX_DAC_S[1-3]
U16
AUX_DAC_S1 {SDIN} 3
AUX_DAC_S2 {SCLK} 2
AUX_DAC_S3 {SYNC#} 1
SDIN
SCLK
SYNC
VDD
GND
VOUT
12 Bit D/A
AD5621BKSZ
R73
0R;0402;1%
LEFT_CONN_B13
Gain DAC adjacent to B13 on the
bottom of the Left Connector

AK + AZ

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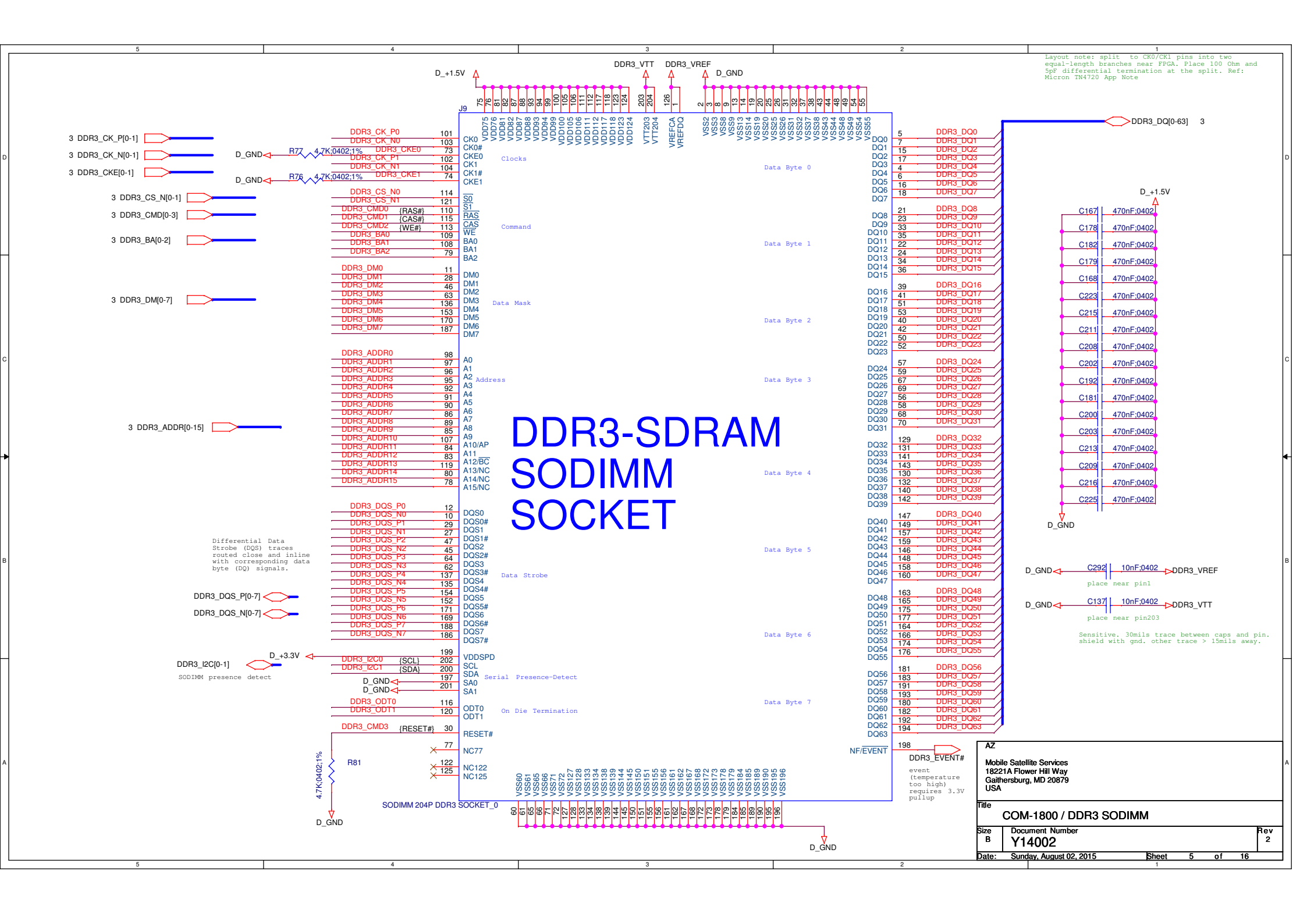
DDR3-SDRAM
SODIMM
SOCKET
J9
SODIMM 204P DDR3 SOCKET_0
Layout note: split to CK0/CK1 pins into two equal-length branches near FPGA. Place 100 Ohm and 5pF differential termination at the split. Ref: Micron TN4720 App Note
D_+1.5V
DDR3_VTT
DDR3_VREF
D_GND
DDR3_DQ[0-63] 3
3 DDR3_CK_P[0-1]
3 DDR3_CK_N[0-1]
3 DDR3_CKE[0-1]
3 DDR3_CS_N[0-1]
3 DDR3_CMD[0-3]
3 DDR3_BA[0-2]
3 DDR3_DM[0-7]
3 DDR3_ADDR[0-15]
DDR3_DQS_P[0-7]
DDR3_DQS_N[0-7]
DDR3_I2C[0-1]
SODIMM presence detect
Differential Data Strobe (DQS) traces routed close and inline with corresponding data byte (DQ) signals.
Clocks
Command
Address
Data Mask
Data Strobe
Serial Presence-Detect
On Die Termination
Data Byte 0
Data Byte 1
Data Byte 2
Data Byte 3
Data Byte 4
Data Byte 5
Data Byte 6
Data Byte 7
R77 4.7K;0402;1%
R76 4.7K;0402;1%
R81 4.7K;0402;1%
DDR3_CKE0
DDR3_CKE1
{RAS#}
{CAS#}
{WE#}
{SCL}
{SDA}
{RESET#}
NC77
NC122
NC125
NF/EVENT
DDR3_EVENT#
event (temperature too high) requires 3.3V pullup
C167 470nF;0402
C178 470nF;0402
C182 470nF;0402
C179 470nF;0402
C168 470nF;0402
C223 470nF;0402
C215 470nF;0402
C211 470nF;0402
C208 470nF;0402
C202 470nF;0402
C192 470nF;0402
C181 470nF;0402
C200 470nF;0402
C203 470nF;0402
C213 470nF;0402
C209 470nF;0402
C216 470nF;0402
C225 470nF;0402
C292 10nF;0402
C137 10nF;0402
place near pin1
place near pin203
Sensitive. 30mils trace between caps and pin. shield with gnd. other trace > 15mils away.
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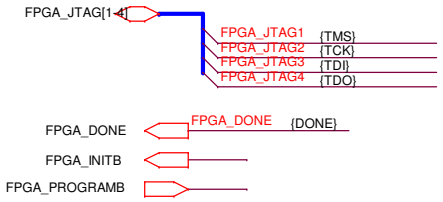
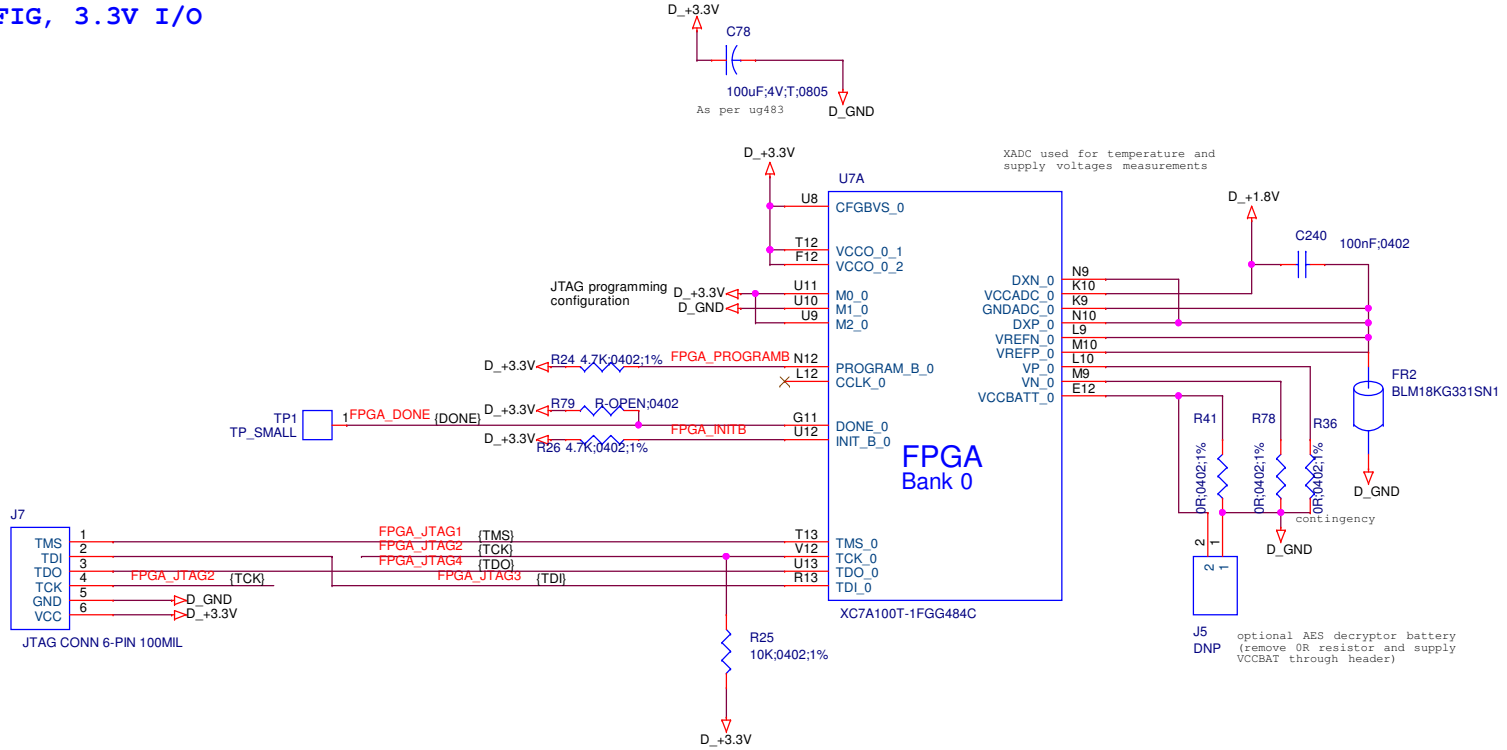
FPGA DEDICATED CONFIG, 3.3V I/O

ARM – FPGA communication programming





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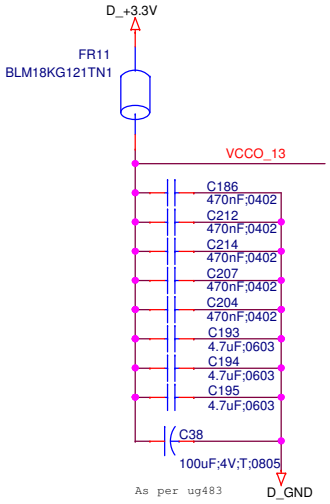
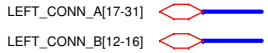
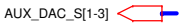
FPGA BANK 13, 3.3 I/O



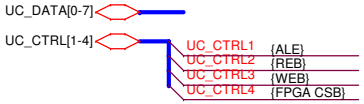
I/Os (LVCMOS33)



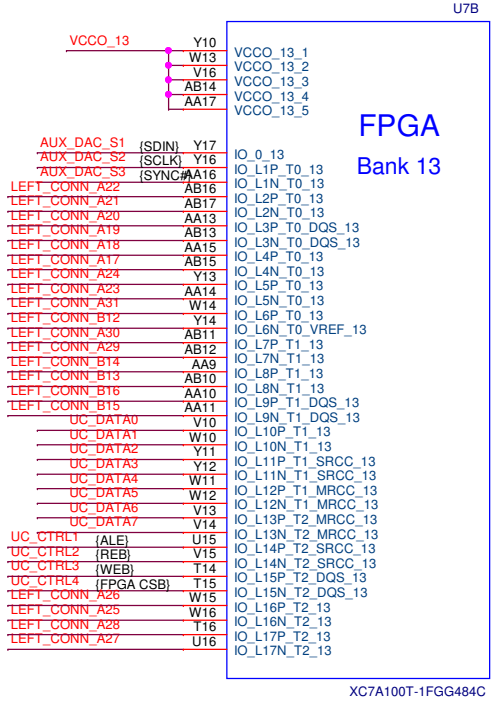
Auxiliary DAC



ARM - FPGA communication



8-bit data bus shared by FPGA and NAND flash



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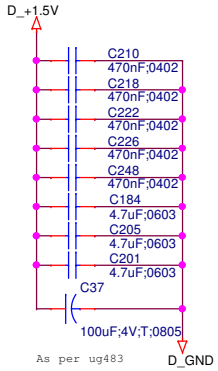
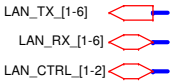
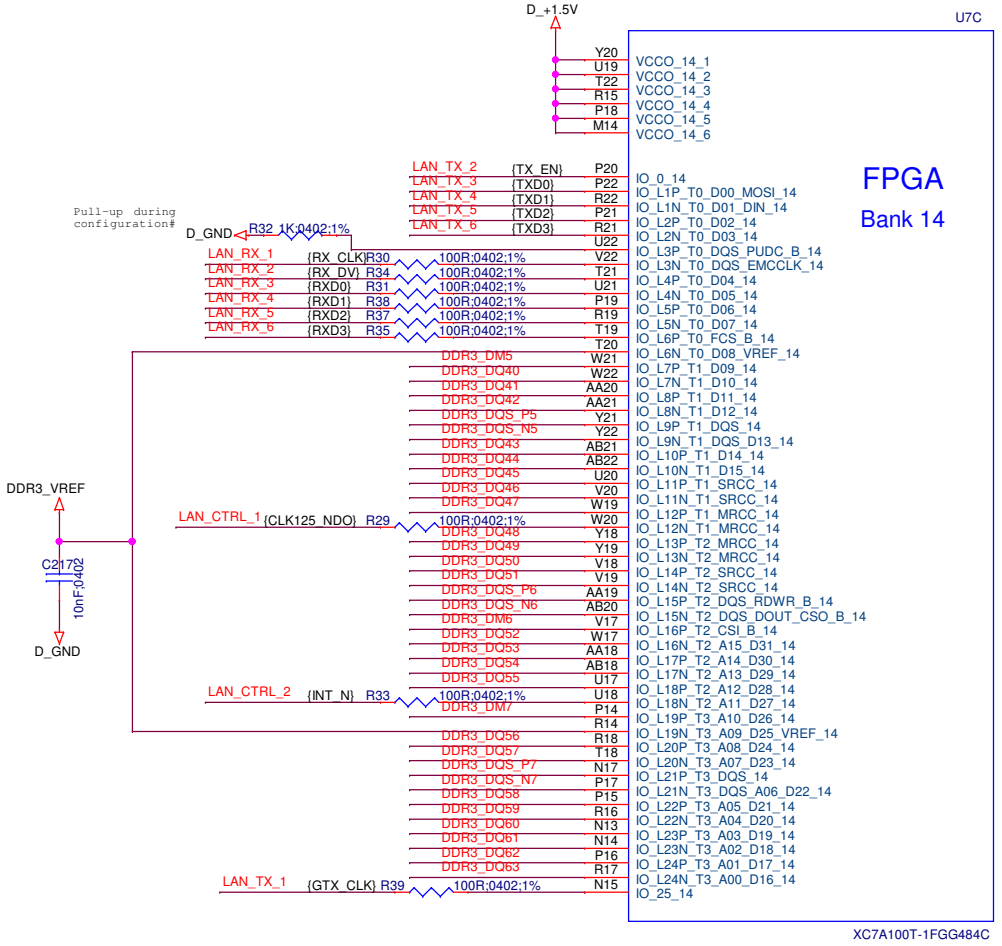
FPGA BANK 14, 1.5V I/O



DDR3 SODIMM

Ethernet LAN PHY





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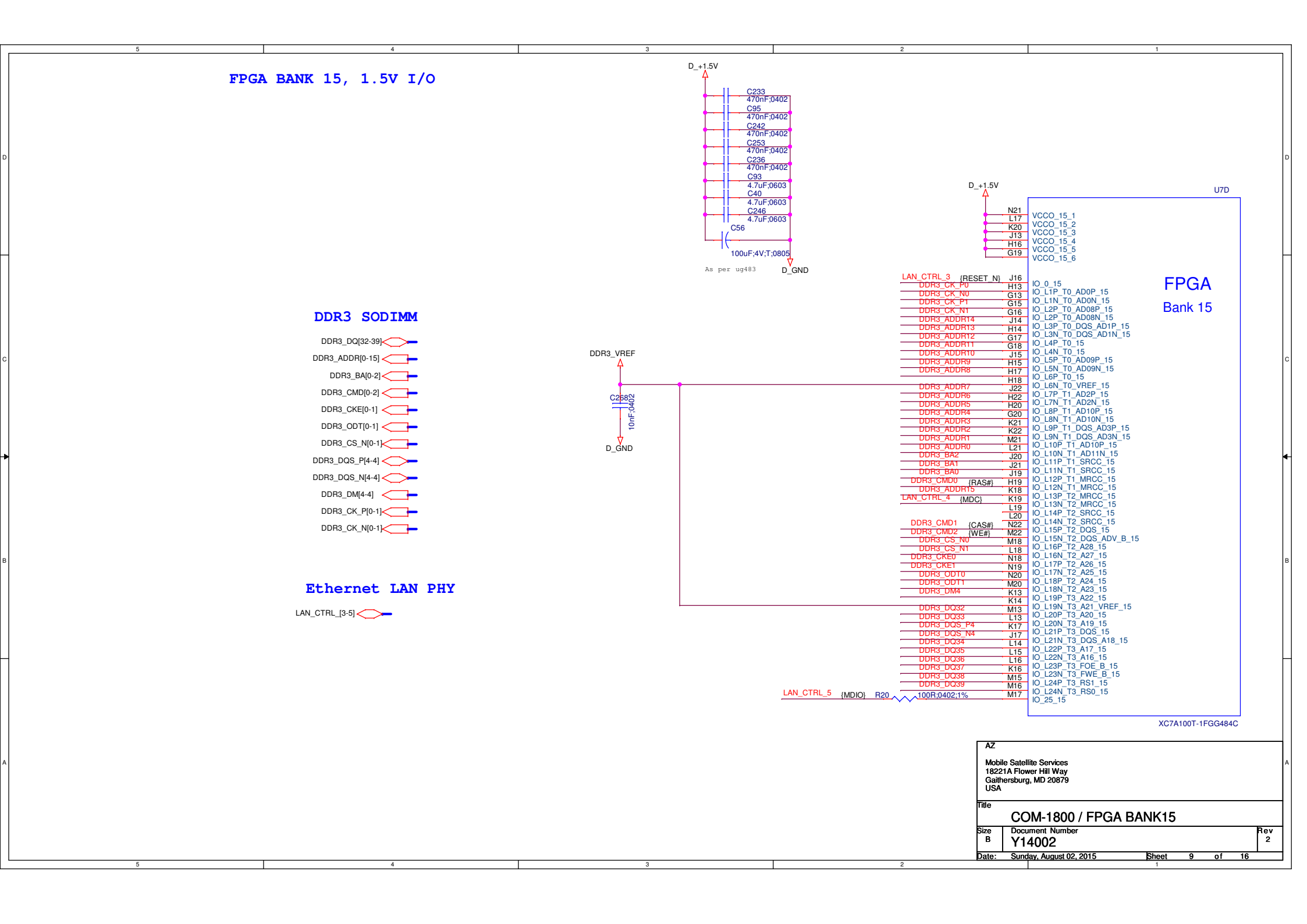
FPGA BANK 15, 1.5V I/O



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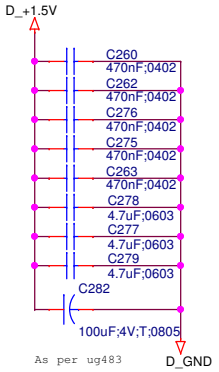
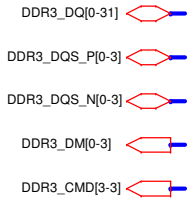
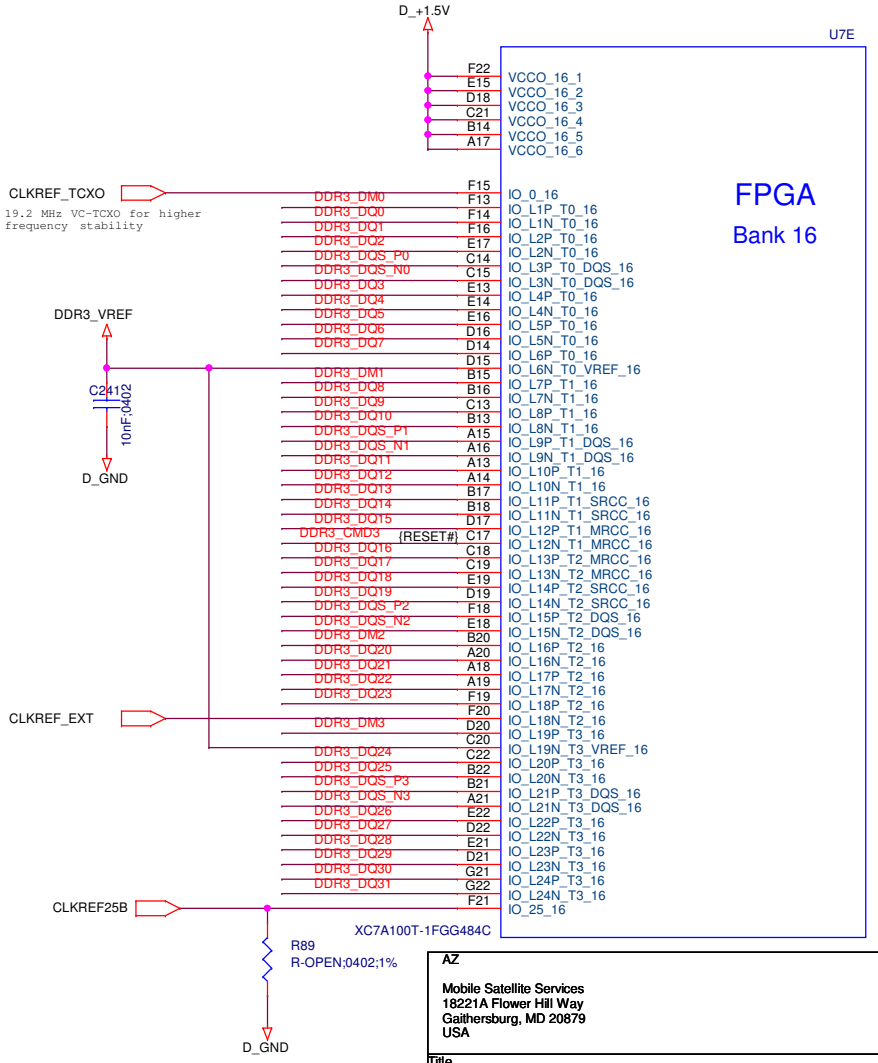
FPGA BANK 16, 1.5V I/O



DDR3 SODIMM





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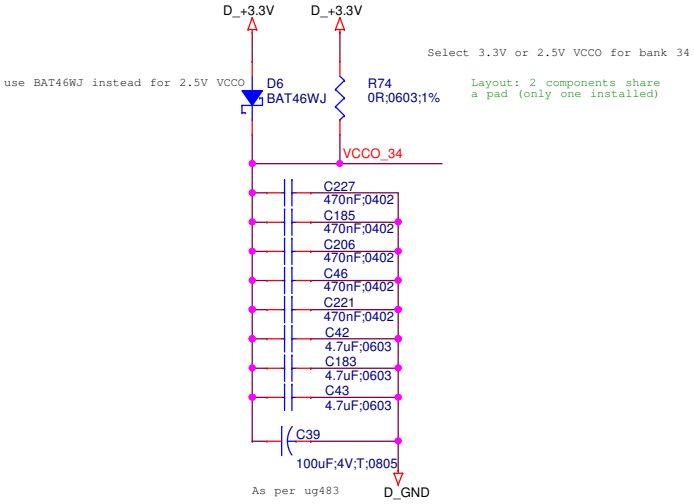
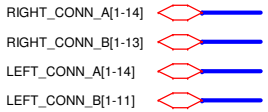
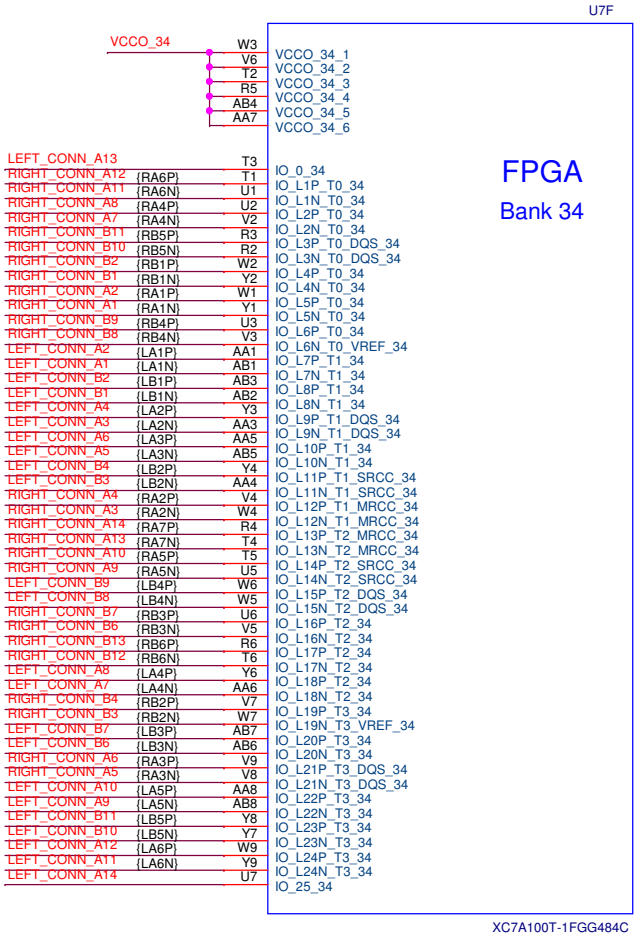
FPGA BANK 34, 2.5V or 3.3 I/O



I/Os (LVCMOS or LVDS)





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Title: COM-1800 / FPGA BANK34

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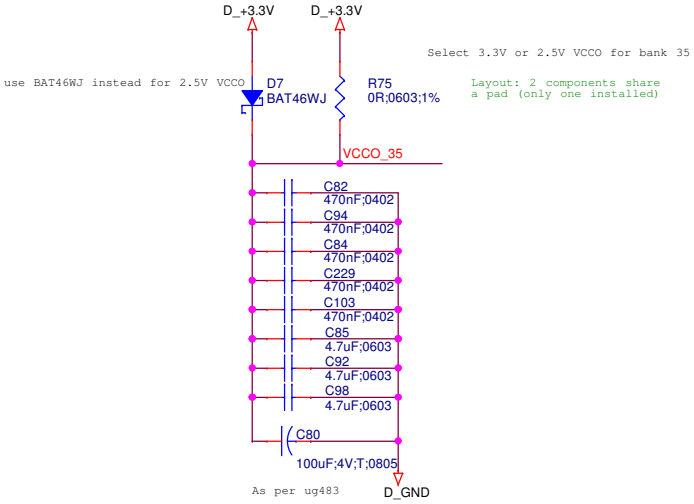
FPGA BANK 35, 2.5V or 3.3 I/O

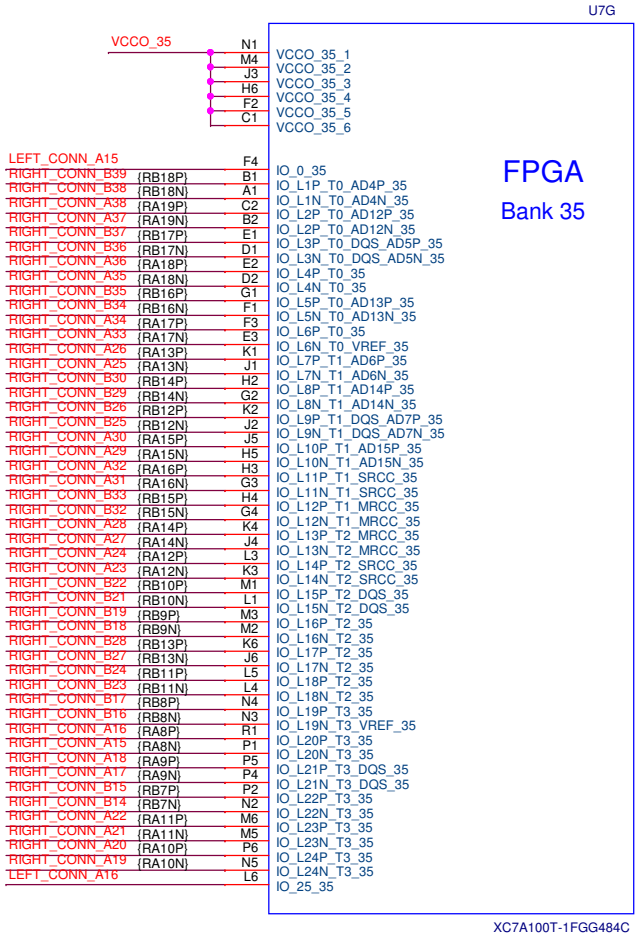


HIGH-SPEED LVCMOS or LVDS I/Os

RIGHT_CONN_A[15-38]

RIGHT_CONN_B[14-39]

LEFT_CONN_A[15-16]



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Title: COM-1800 / FPGA BANK35

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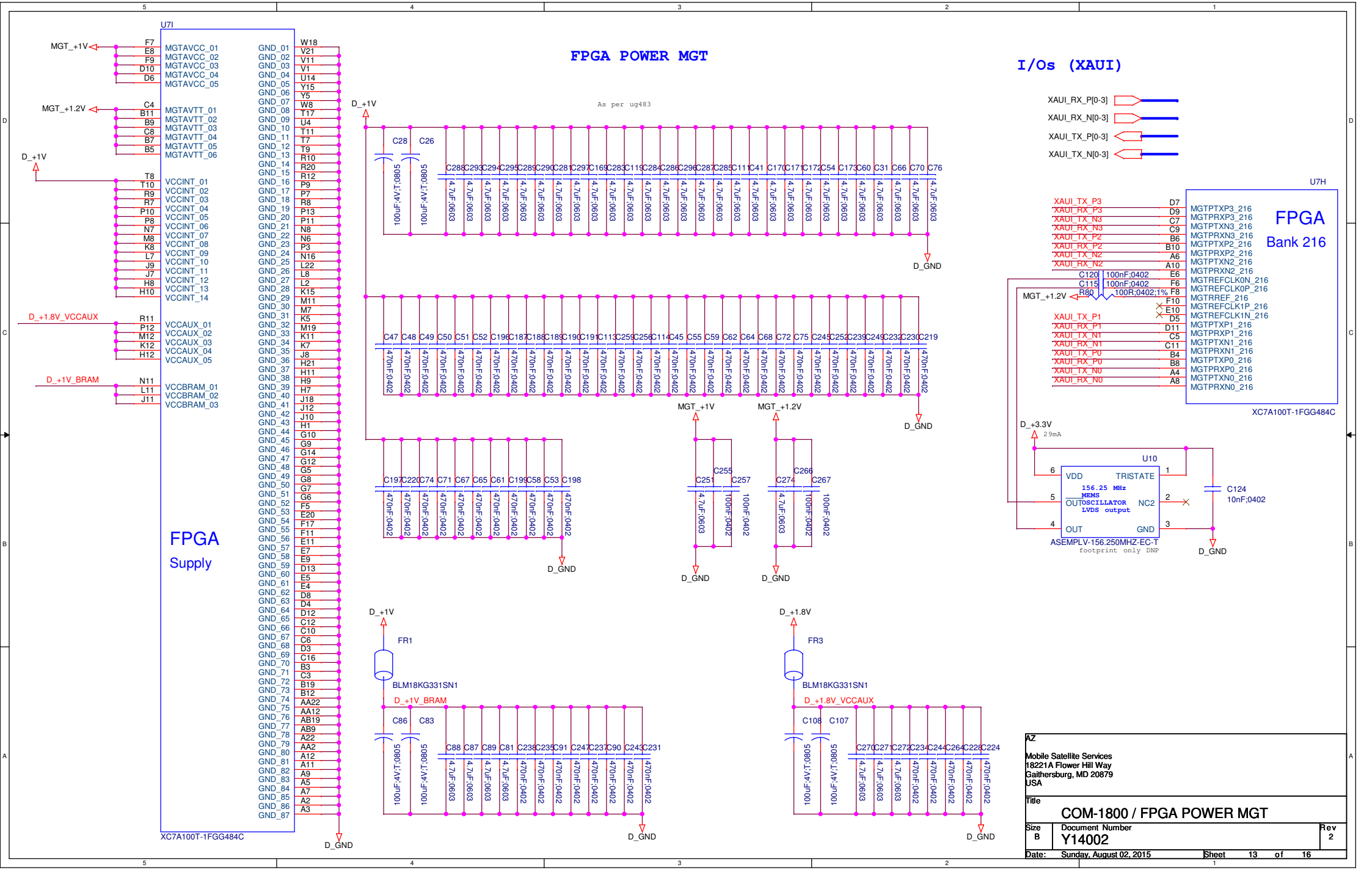
FPGA POWER MGT
I/Os (XAUI)
U7I
FPGA
Supply
XC7A100T-1FGG484C
MGT_+1V
MGT_+1.2V
D_+1V
D_+1.8V_VCCAUX
D_+1V_BRAM
D_+1.8V
D_GND
As per ug483
XAUI_RX_P[0-3]
XAUI_RX_N[0-3]
XAUI_TX_P[0-3]
XAUI_TX_N[0-3]
U7H
FPGA
Bank 216
XC7A100T-1FGG484C
D_+3.3V
29mA
U10
VDD
TRISTATE
OUT
GND
NC2
156.25 MHz
MEMS
OSCILLATOR
LVDS output
ASEMPLV-156.250MHZ-EC-T
footprint only DNP
C124
10nF;0402
FR1
FR3
BLM18KG331SN1
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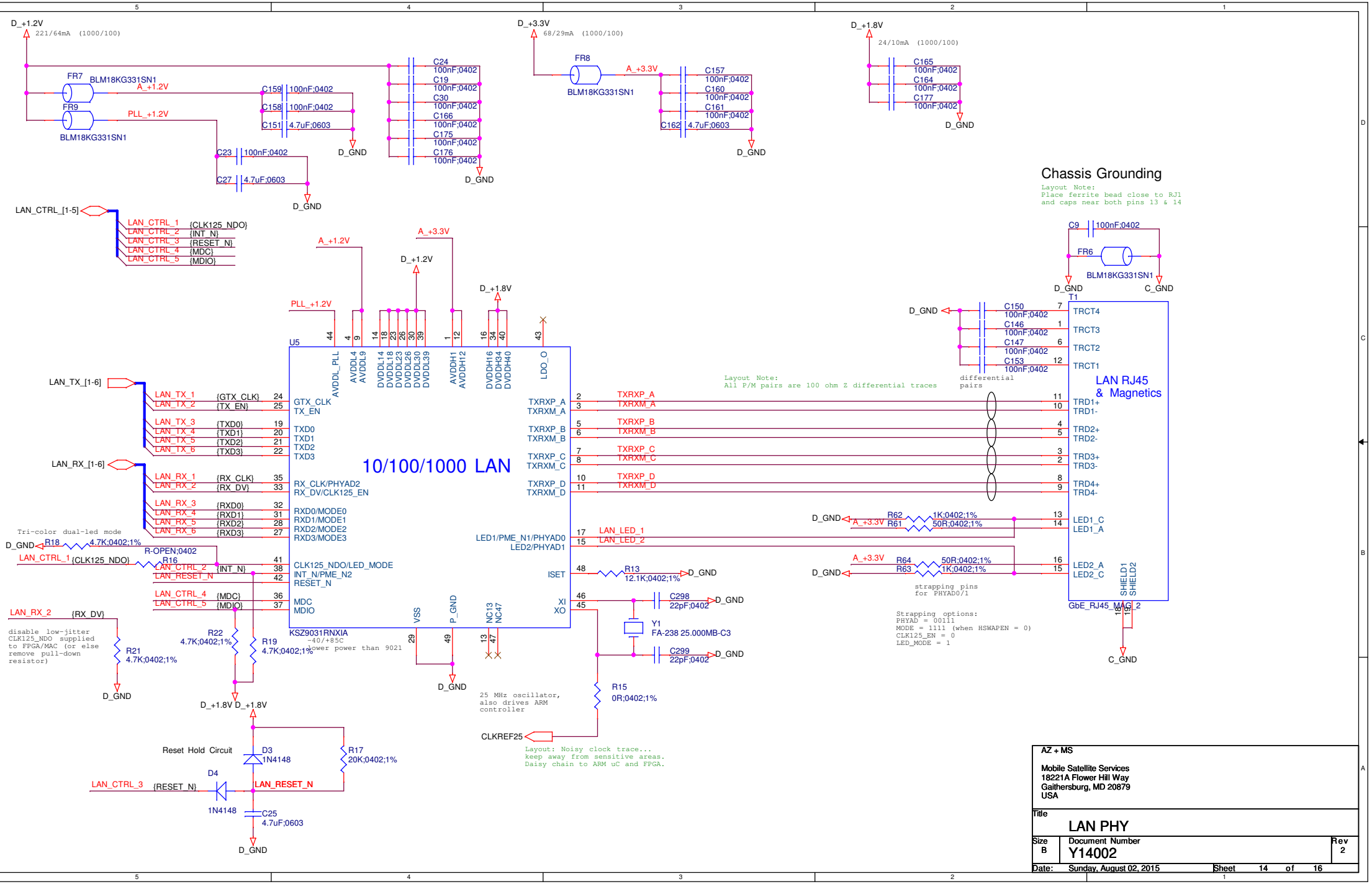
D_+1.2V
221/64mA (1000/100)
FR7
BLM18KG331SN1
A_+1.2V
FR9
BLM18KG331SN1
PLL_+1.2V
C159 100nF;0402
C158 100nF;0402
C151 4.7uF;0603
C23 100nF;0402
C27 4.7uF;0603
D_GND
C24 100nF;0402
C19 100nF;0402
C30 100nF;0402
C166 100nF;0402
C175 100nF;0402
C176 100nF;0402
D_+3.3V
68/29mA (1000/100)
FR8
BLM18KG331SN1
A_+3.3V
C157 100nF;0402
C160 100nF;0402
C161 100nF;0402
C162 4.7uF;0603
D_+1.8V
24/10mA (1000/100)
C165 100nF;0402
C164 100nF;0402
C177 100nF;0402
Chassis Grounding
Layout Note:
Place ferrite bead close to RJ1
and caps near both pins 13 & 14
C9 100nF;0402
FR6
BLM18KG331SN1
C_GND
LAN_CTRL_[1-5]
LAN_CTRL_1 {CLK125_NDO}
LAN_CTRL_2 {INT_N}
LAN_CTRL_3 {RESET_N}
LAN_CTRL_4 {MDC}
LAN_CTRL_5 {MDIO}
U5
10/100/1000 LAN
KSZ9031RNXIA
-40/+85C
lower power than 9021
AVDDL_PLL
AVDDL4
AVDDL9
DVDDL14
DVDDL18
DVDDL23
DVDDL26
DVDDL30
DVDDL39
AVDDH1
AVDDH12
DVDDH16
DVDDH34
DVDDH40
LDO_O
VSS
P_GND
NC13
NC47
LAN_TX_[1-6]
LAN_TX_1 {GTX_CLK} 24
LAN_TX_2 {TX_EN} 25
LAN_TX_3 {TXD0} 19
LAN_TX_4 {TXD1} 20
LAN_TX_5 {TXD2} 21
LAN_TX_6 {TXD3} 22
GTX_CLK
TX_EN
TXD0
TXD1
TXD2
TXD3
LAN_RX_[1-6]
LAN_RX_1 {RX_CLK} 35
LAN_RX_2 {RX_DV} 33
LAN_RX_3 {RXD0} 32
LAN_RX_4 {RXD1} 31
LAN_RX_5 {RXD2} 28
LAN_RX_6 {RXD3} 27
RX_CLK/PHYAD2
RX_DV/CLK125_EN
RXD0/MODE0
RXD1/MODE1
RXD2/MODE2
RXD3/MODE3
Tri-color dual-led mode
D_GND R18 4.7K;0402;1%
R-OPEN;0402
LAN_CTRL_1 {CLK125_NDO} R16
LAN_CTRL_2 {INT_N} 41
LAN_RESET_N 42
CLK125_NDO/LED_MODE
INT_N/PME_N2
RESET_N
LAN_CTRL_4 {MDC} 36
LAN_CTRL_5 {MDIO} 37
MDC
MDIO
LAN_RX_2 {RX_DV}
disable low-jitter CLK125_NDO supplied to FPGA/MAC (or else remove pull-down resistor)
R21 4.7K;0402;1%
D_GND
R22 4.7K;0402;1%
R19 4.7K;0402;1%
D_+1.8V D_+1.8V
Reset Hold Circuit
D3 1N4148
D4
1N4148
LAN_CTRL_3 {RESET_N}
LAN_RESET_N
R17 20K;0402;1%
C25 4.7uF;0603
D_GND
D_GND
D_GND
TXRXP_A
TXRXM_A
TXRXP_B
TXRXM_B
TXRXP_C
TXRXM_C
TXRXP_D
TXRXM_D
LED1/PME_N1/PHYAD0
LED2/PHYAD1
ISET
R13 12.1K;0402;1%
D_GND
XI
XO
C298 22pF;0402
D_GND
Y1
FA-238 25.000MB-C3
C299 22pF;0402
D_GND
25 MHz oscillator, also drives ARM controller
R15 0R;0402;1%
CLKREF25
Layout: Noisy clock trace... keep away from sensitive areas. Daisy chain to ARM uC and FPGA.
Layout Note:
All P/M pairs are 100 ohm Z differential traces
differential pairs
T1
LAN RJ45 & Magnetics
GbE_RJ45_MAG_2
TRCT4
TRCT3
TRCT2
TRCT1
TRD1+
TRD1-
TRD2+
TRD2-
TRD3+
TRD3-
TRD4+
TRD4-
C150 100nF;0402
C146 100nF;0402
C147 100nF;0402
C153 100nF;0402
D_GND
C_GND
LAN_LED_1
LAN_LED_2
LED1_C
LED1_A
LED2_A
LED2_C
R62 1K;0402;1%
R61 50R;0402;1%
R64 50R;0402;1%
R63 1K;0402;1%
A_+3.3V
D_GND
strapping pins for PHYAD0/1
Strapping options:
PHYAD = 00111
MODE = 1111 (when HSWAPEN = 0)
CLK125_EN = 0
LED_MODE = 1
SHIELD1
SHIELD2
C_GND
AZ + MS
Mobile Satellite Services
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USA
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+5V DC Supply

OPERATIONAL RANGE: 4.5 - 12V
No damage: 20V max

Filter

J2
BATT+ 1
BATT- 2
P02ECH381RH-E
low-profile 3.81mm terminal block
D_GND

FR5
BLM18KG121TN1

Reverse Voltage Protection

Q2
D5 D6 S
D2 D1 G
FDC658AP
-30V, -3.4A, 75mOhm
D_GND

Transient Voltage Suppression

Vin_prot
C
D2
12V TVS
A
D_GND

PCB Mounting Holes

H3 H4 H2 H1
D_GND D_GND D_GND D_GND

1V 3A

Vin_prot
PGOOD1 {+1V}
U6
NCP3170A 3A DC/DC Converter
PG VIN EN COMP VSW FB PGND AGND
VREF=0.8V
NCP3170ADR2G
C79 22uF;16V;T;1210
C44 15nF;0402
R23 1K;0402;1%
L3 3.3uH;4A
R28 24.9K;0402;1%
C57 150pF;0402
R27 100K;0402;1%
Ityp = TBDmA Vout = 1V
C63 C34 C32 C33 C69 C73 C77 100uF;4V;T;0805
C35 4.7uF;0603
C36 470nF;0402
D_+1V
FR12 BLM18KG121TN1
MGT_+1V
D_GND

FPGA VCCINT 328mA quiescent
FPGA VCCBRAM 11mA quiescent

1.2V 3A

PGOOD2 {+1.2V}
U14
NCP3170A 3A DC/DC Converter
PG VIN EN COMP VSW FB PGND AGND
VREF=0.8V
NCP3170ADR2G
C14 22uF;16V;T;1210
C148 10nF;0402
R71 1K;0402;1%
L2 3.3uH;4A
R72 24.9K;0402;1%
C154 150pF;0402
R67 49.9K;0402;1%
Ityp = TBDmA Vout = 1.2V
C29 100uF;4V;T;0805
C155 4.7uF;0603
C156 470nF;0402
D_+1.2V
FR13 BLM18KG121TN1
MGT_+1.2V
D_GND

LAN 221mA

PGOOD[1-3]
Power Good Indicators
Must be pulled up by ARM processor
PGOOD1 {+1V}
PGOOD2 {+1.2V}
PGOOD3 {+1.5V}

1.5V 3A

PGOOD3 {+1.5V}
U13
NCP3170A 3A DC/DC Converter
PG VIN EN COMP VSW FB PGND AGND
VREF=0.8V
NCP3170ADR2G
C132 22uF;16V;T;1210
C131 10nF;0402
R60 1K;0402;1%
L5 3.3uH;4A
R54 24.9K;0402;1%
C122 150pF;0402
R44 28.7K;0402;1%
Ityp = TBDmA Vout = 1.49V
C127 100uF;4V;T;0805
C126 4.7uF;0603
C130 470nF;0402
D_+1.5V
D_GND

AZ

Mobile Satellite Services
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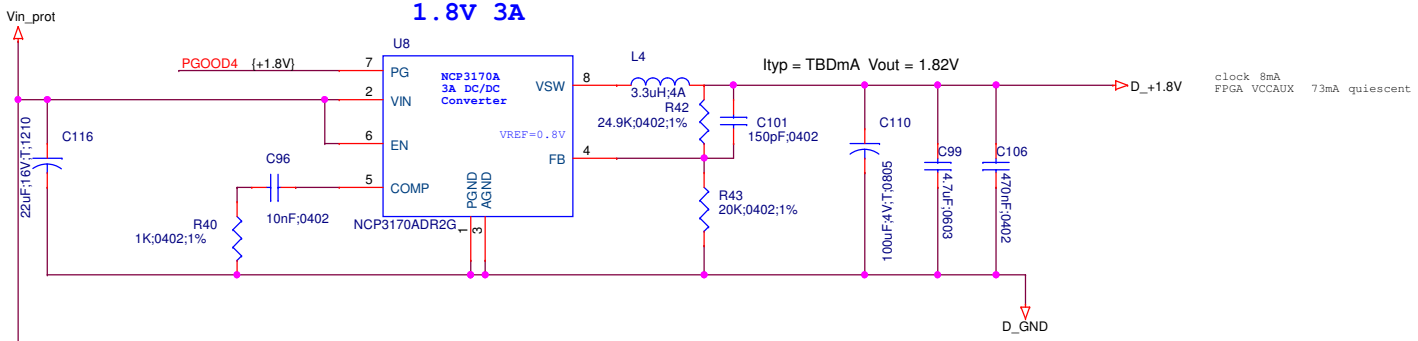
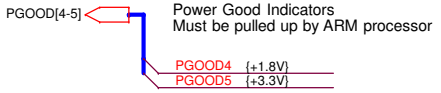
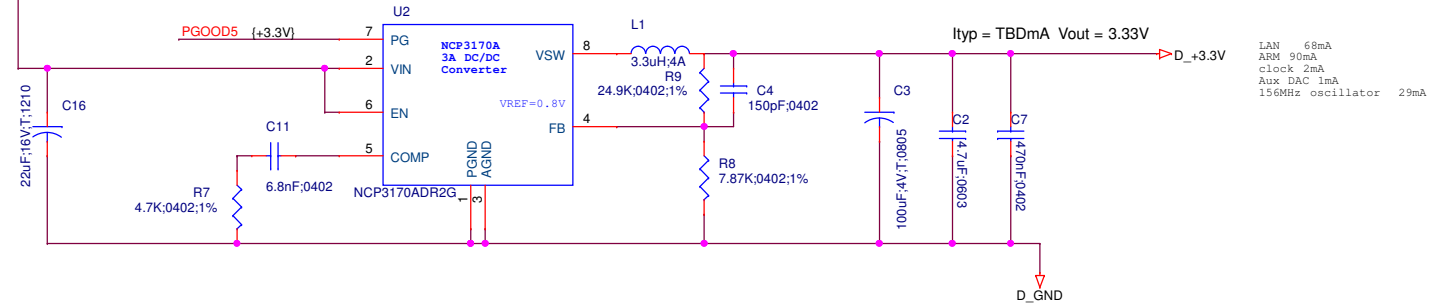
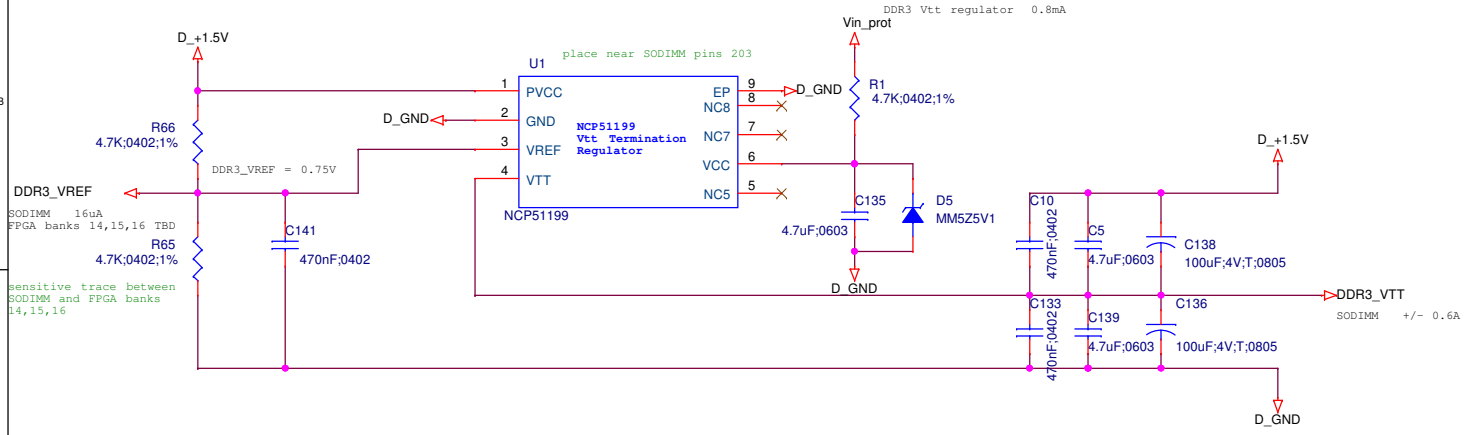
1.8V 3A





3.3V 3A





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Sensitive. 30mils trace between caps and pin.
shield with gnd. other trace > 15mils away.