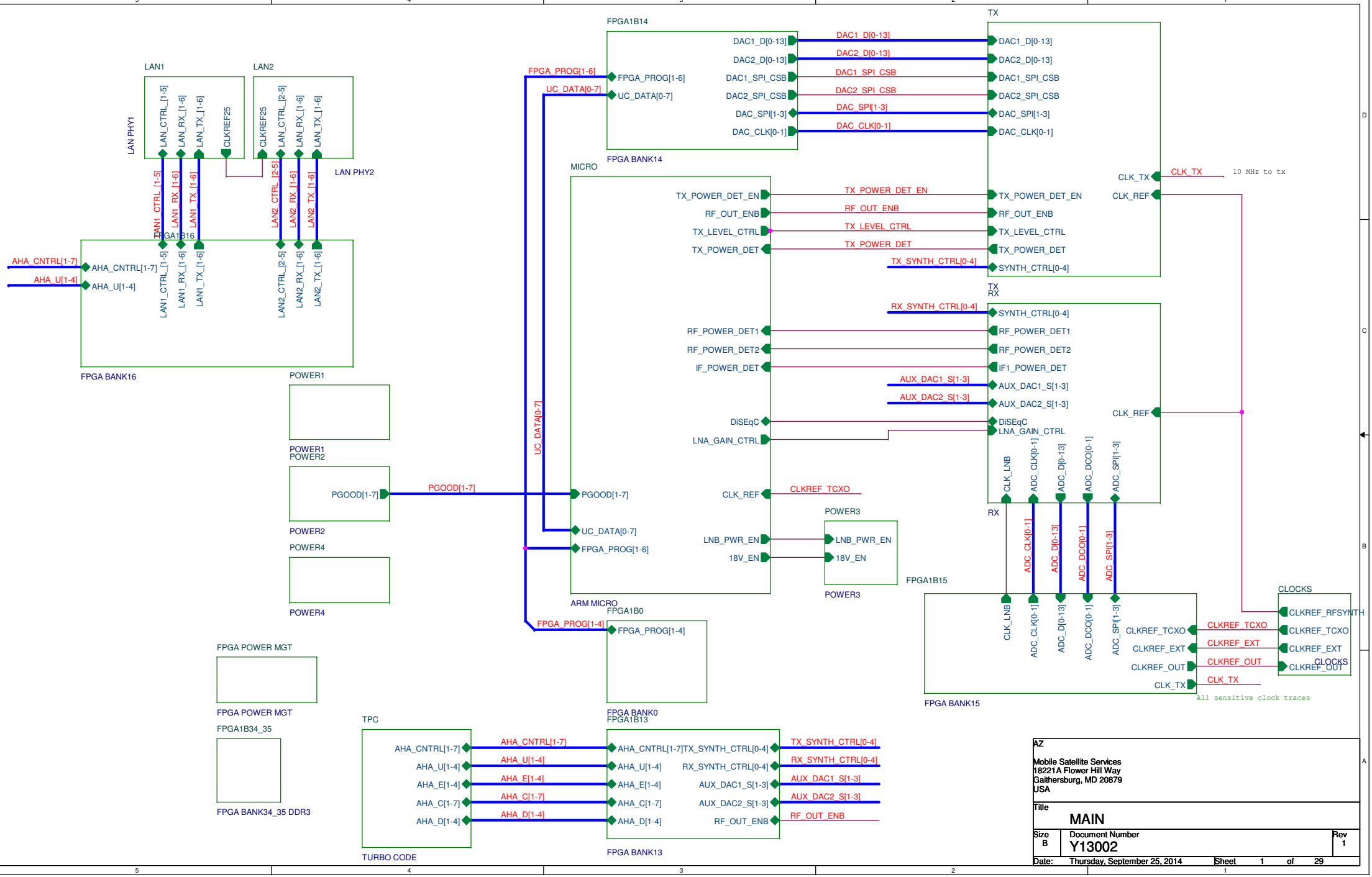
LAN1
LAN2
LAN PHY1
LAN PHY2
LAN_CTRL_[1-5]
LAN_RX_[1-6]
LAN_TX_[1-6]
CLKREF25
LAN2_CTRL_[2-5]
LAN2_RX_[1-6]
LAN2_TX_[1-6]
FPGA1B16
FPGA BANK16
AHA_CNTRL[1-7]
AHA_U[1-4]
POWER1
POWER2
POWER4
PGOOD[1-7]
FPGA_PROG[1-6]
UC_DATA[0-7]
FPGA1B14
FPGA BANK14
DAC1_D[0-13]
DAC2_D[0-13]
DAC1_SPI_CSB
DAC2_SPI_CSB
DAC_SPI[1-3]
DAC_CLK[0-1]
MICRO
ARM MICRO
TX_POWER_DET_EN
RF_OUT_ENB
TX_LEVEL_CTRL
TX_POWER_DET
TX_SYNTH_CTRL[0-4]
RX_SYNTH_CTRL[0-4]
RF_POWER_DET1
RF_POWER_DET2
IF_POWER_DET
AUX_DAC1_S[1-3]
AUX_DAC2_S[1-3]
DiSEqC
LNA_GAIN_CTRL
CLK_REF
CLKREF_TCXO
POWER3
LNB_PWR_EN
18V_EN
TX
RX
CLK_TX
10 MHz to tx
CLK_LNB
ADC_CLK[0-1]
ADC_D[0-13]
ADC_DCO[0-1]
ADC_SPI[1-3]
FPGA1B15
FPGA BANK15
CLOCKS
CLKREF_RFSYNTH
CLKREF_EXT
CLKREF_OUT
All sensitive clock traces
FPGA1B0
FPGA BANK0
FPGA POWER MGT
FPGA1B34_35
FPGA BANK34_35 DDR3
TPC
TURBO CODE
AHA_E[1-4]
AHA_C[1-7]
AHA_D[1-4]
FPGA1B13
FPGA BANK13
AZ
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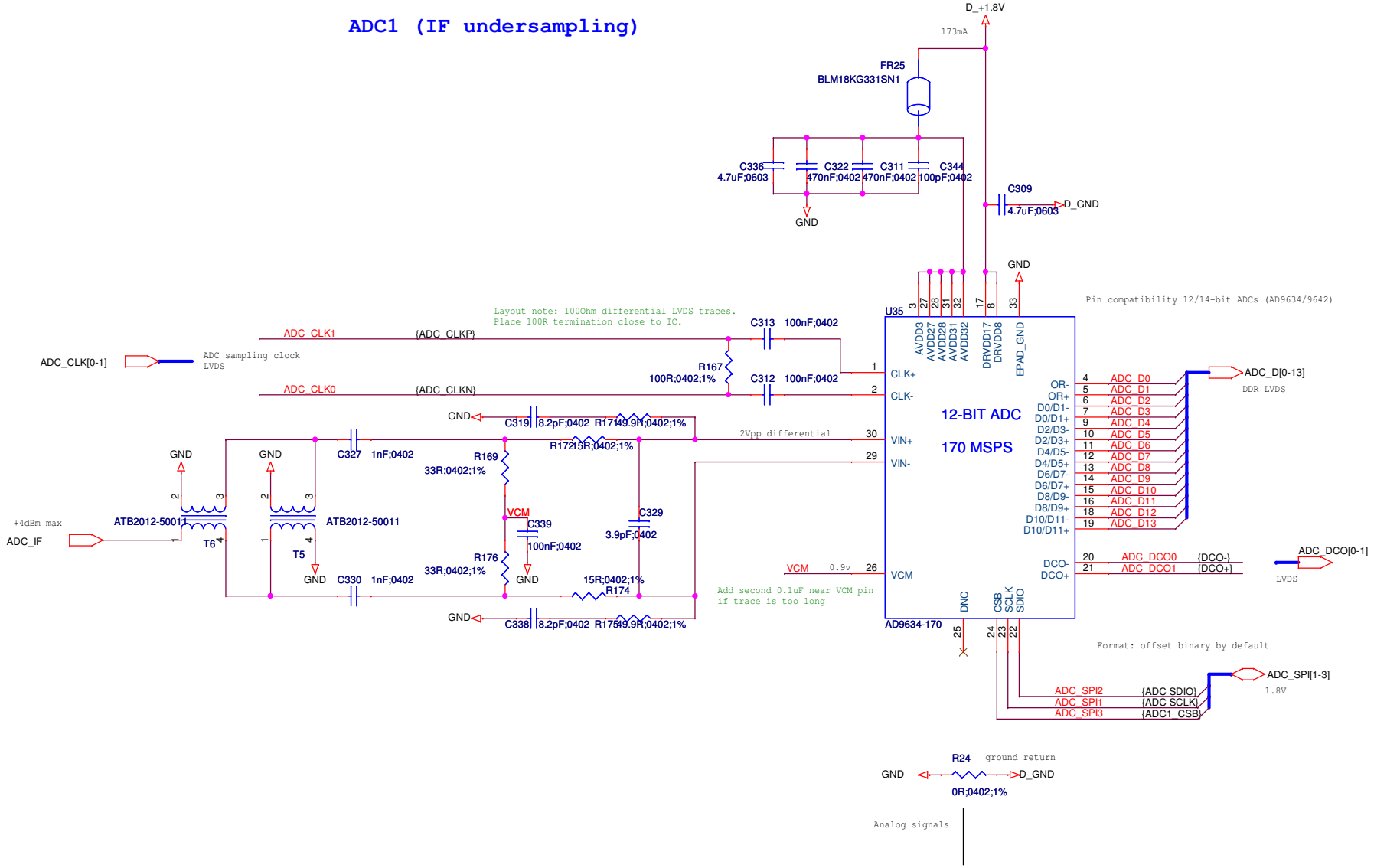
Title
MAIN
Size
B
Document Number
Y13002
Rev
1
Date:
Thursday, September 25, 2014
Sheet
1
of
29

ADC1 (IF undersampling)



AZ		
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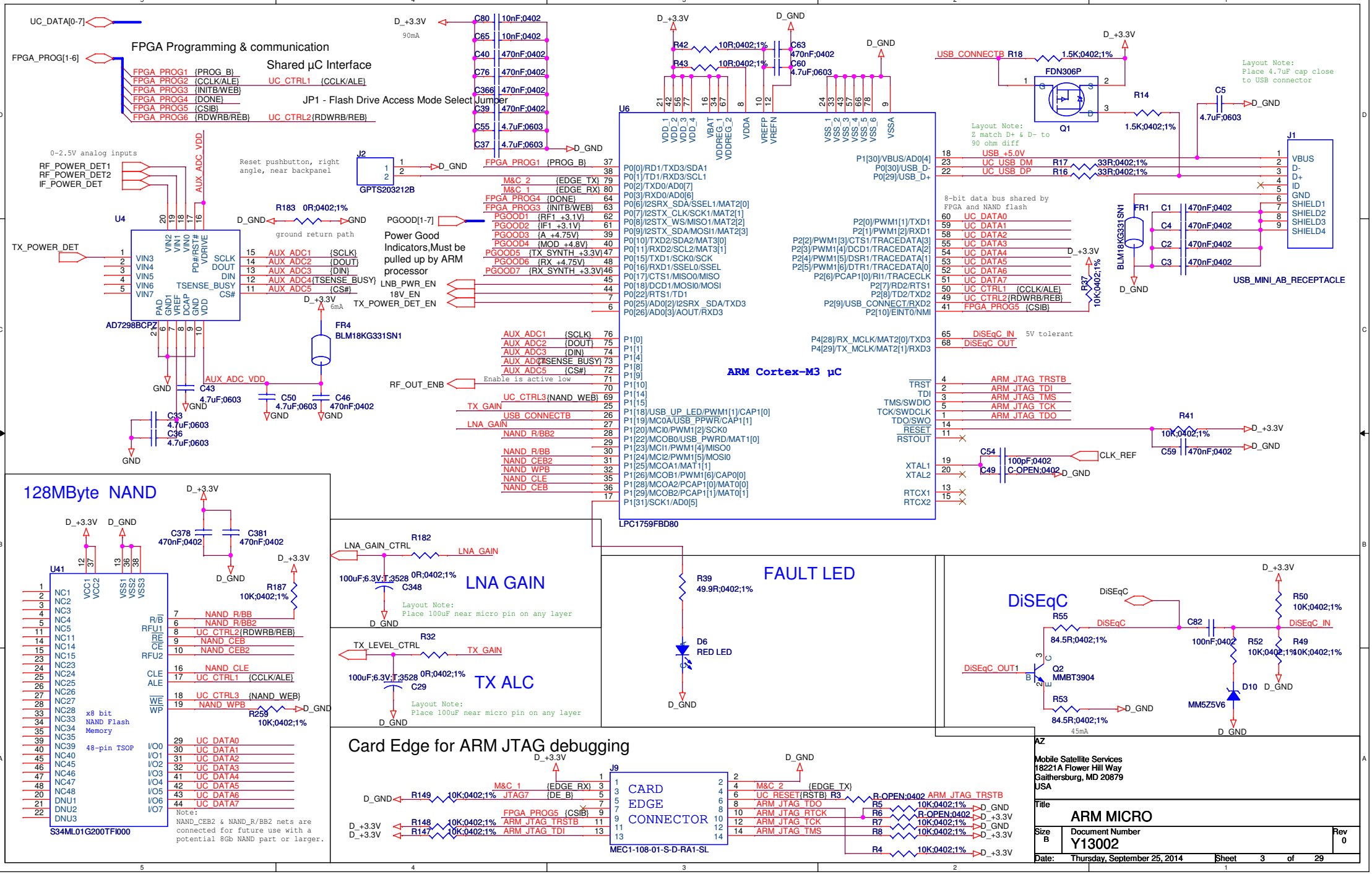
Title: ADC1		
Size: B	Document Number: Y13002	Rev: 1
Date: Thursday, September 25, 2014	Sheet 2 of 29	


FPGA Programming & communication
Shared µC Interface
JP1 - Flash Drive Access Mode Select Jumper
ARM Cortex-M3 µC
LPC1759FBD80
U6
U4
AD7298BCPZ
GPTS203212B
J2
J1
USB_MINI_AB_RECEPTACLE
FDN306P
Q1
BLM18KG331SN1
128MByte NAND
S34ML01G200TFI000
U41
LNA GAIN
TX ALC
FAULT LED
D6
RED LED
DiSEqC
Q2
MMBT3904
MM5Z5V6
Card Edge for ARM JTAG debugging
J9
CARD EDGE CONNECTOR
MEC1-108-01-S-D-RA1-SL
Reset pushbutton, right angle, near backpanel
Power Good Indicators,Must be pulled up by ARM processor
Layout Note: Place 4.7uF cap close to USB connector
Layout Note: 2 match D+ & D- to 90 ohm diff
Layout Note: Place 100uF near micro pin on any layer
Note: NAND_CEB2 & NAND_R/BB2 nets are connected for future use with a potential 8Gb NAND part or larger.
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Title
ARM MICRO
Size B
Document Number Y13002
Rev 0
Date: Thursday, September 25, 2014
Sheet 3 of 29

Design note1: use 1.8V drivers to minimize noise
Design note2: place 33R at source to dampen waveform/reduce overshoot/clock harmonics
Design note3: NC7SZ04 is 5.5V tolerant

(19.2MHz) VC-TCXO

2.5ppm over -30/+75C, 1ppm/year aging
Calibrate at manufacturing

D_+3.3V
R262 TC33X-2-103E
D_+3.3V D_GND
2mA
R263 100R;0402;1%
U56
VCTR VDD
GND2 OUT
C595 470nF;0402
C596 470nF;0402
D_GND
D_GND
VC-TCXO 19.2MHz

Need amplification because amplitude is 800mVpp typ

C188 470nF;0402

D_+1.8V
R89 10K;0402;1%
R93 12K;0402;1%
D_GND

U57 NC VCC GND A Y NC7SZ04P5X
D_+1.8V D_GND D_+1.8V
C597 470nF;0402
D_GND
R266 33R;0402;1%
CLKREF_RFSYNTH
To RF frequency synthesizers

U15 NC VCC GND A Y NC7SZ04P5X
D_+1.8V D_GND D_+1.8V
C165 470nF;0402
D_GND
R84 33R;0402;1%
CLKREF_TCXO
To FPGA (1.8V bank)

Layout note:
Noise sources should be routed away from reference clock circuitry.

EXTERNAL FREQUENCY REFERENCE (INPUT)
10 MHz or 1PPS

J6
UMCC
GND2
D_GND

Ultra-minature coaxial connector on PCB. Connected to IP67 SMA on front-panel through cabling.

C274 470nF;0402

D_+1.8V
R137 10K;0402;1%
R136 12K;0402;1%
D_GND

U26 NC VCC GND A Y NC7SZ04P5X
D_+1.8V D_GND D_+1.8V
C270 470nF;0402
D_GND
R131 33R;0402;1%
CLKREF_EXT
To FPGA (1.8V bank)

Layout note:
Noise sources should be routed away from reference clock circuitry.

5.6V Zener: Prevent over/under-voltage damage to NC7SZ04 at analog inputs.

INTERNAL FREQUENCY REFERENCE (OUTPUT)
10 MHz

J7
UMCC
GND2
D_GND

C273 24pF;0402
L31 10uH;0603;SRF > 50MHz
tuned to 10 MHz

R132 33R;0402;1%
R134 R-OPEN;0402
D_GND

D_+1.8V D_+1.8V
C266 470nF;0402
D_GND D_GND
U25 GND VCC NC Y A NC7SZ04P5X
CLKREF_OUT

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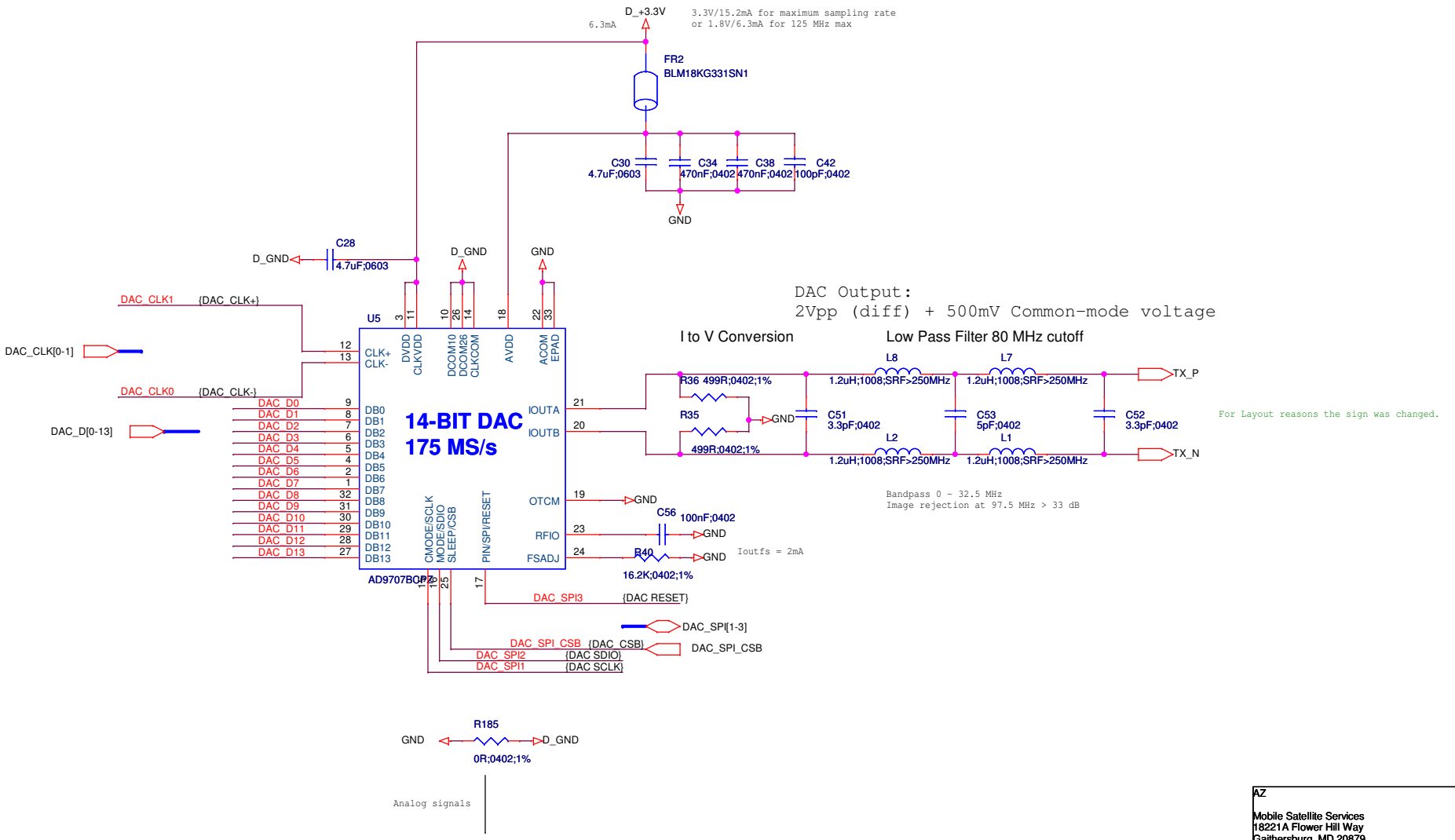
Title: CLOCKS			
Size: B	Document Number: Y13002		Rev: 0
Date: Thursday, September 25, 2014	Sheet 4 of 29		

DAC (1 baseband channel)



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Title: DAC		
Size: B	Document Number: Y13002	Rev: 0
Date: Friday, October 25, 2013	Sheet 5 of 29	

AHA_CNTRL[1-7]
{RESET_N} AHA_CNTRL1
{PLL_SYSCLK} AHA_CNTRL2
{E_CS_N} AHA_CNTRL3
{D_CS_N} AHA_CNTRL4
{E_GOUT} AHA_CNTRL5
{D_GOUT} AHA_CNTRL6
{PLL_BYPASS} AHA_CNTRL7

AHA_U[1-4]
{U_CLK} AHA_U1
{U_DATA} AHA_U2
{U_FS} AHA_U3
{U_ACPT} AHA_U4

AHA_E[1-4]
{E_CLK} AHA_E1
{E_DATA} AHA_E2
{E_FS} AHA_E3
{E_RDY} AHA_E4

AHA_C[1-7]
{C_CLK} AHA_C1
{C_DATA3} AHA_C2
{C_DATA2} AHA_C3
{C_DATA1} AHA_C4
{C_DATA0} AHA_C5
{C_FS} AHA_C6
{C_ACPT} AHA_C7

AHA_D[1-4]
{D_CLK} AHA_D1
{D_DATA} AHA_D2
{D_FS} AHA_D3
{D_RDY} AHA_D4

This (old) TPC codec is only used as temporary/contingency until a Turbo code or LDPC codec is implemented within the FPGA. It may not be populated.

D_+1.8V
D_+3.3V
C586 470nF;0402
C581 100uF;4V;T;1411
FR46 BLM18KG331SN1
D_+1.8V

U54 AHA4524

VDD1 7, VDD2 13, VDD3 19, VDD4 26, VDD5 31, VDD6 39, VDD7 45, VDD8 49, VDD9 53, VDD10 60
VDDIO_1 3, VDDIO_2 24, VDDIO_3 35, VDDIO_4 58
VAD 43, AGND 42

AHA_CNTRL1 {RESET_N} 51 RESET_N
D_+3.3V 47 TRISTATE_N
D_GND 48 TESTMODE
D_GND 17 SCANMODE
D_+3.3V 4 DPARINPUT
AHA_CNTRL7 {PLL_BYPASS} 44 PLL_BYPASS
D_GND 32 E_MODE
D_GND 64 D_MODE
AHA_CNTRL3 {E_CS_N} 18 E_CS_N
AHA_CNTRL4 {D_CS_N} 52 D_CS_N
AHA_CNTRL2 {PLL_SYSCLK} 41 SYSCLK
AHA_CNTRL5 {E_GOUT} 30 E_GOUT
AHA_CNTRL6 {D_GOUT} 63 D_GOUT
D_+3.3V 9 RDYPOLARITY
D_+3.3V 10 ACPTPOLARITY

UNENCODED DATA
U_CLK 36 {U_CLK} AHA_U1
U_DATA 40 {U_DATA} AHA_U2
U_FS 37 {U_FS} AHA_U3
U_ACPT 33 {U_ACPT} AHA_U4

ENCODED DATA
E_CLK 25 {E_CLK} AHA_E1
E_DATA 22 {E_DATA} AHA_E2
E_FS 21 {E_FS} AHA_E3
E_RDY 28 {E_RDY} AHA_E4

CHANNEL DATA
C_CLK 6 {C_CLK} AHA_C1
C_DATA[3] 11 {C_DATA3} AHA_C2
C_DATA[2] 12 {C_DATA2} AHA_C3
C_DATA[1] 15 {C_DATA1} AHA_C4
C_DATA[0] 16 {C_DATA0} AHA_C5
C_FS 8 {C_FS} AHA_C6
C_ACPT 1 {C_ACPT} AHA_C7

DECODED DATA
D_CLK 59 {D_CLK} AHA_D1
D_DATA 56 {D_DATA} AHA_D2
D_FS 54 {D_FS} AHA_D3
D_RDY 62 {D_RDY} AHA_D4

GND1 5, GND2 14, GND3 20, GND4 27, GND5 29, GND6 38, GND7 46, GND8 50, GND9 55, GND10 61
GNDIO_1 2, GNDIO_2 23, GNDIO_3 34, GNDIO_4 57
D_GND

AHA_CNTRL5 {E_GOUT} 1 TP5
AHA_CNTRL6 {D_GOUT} 1 TP6

D_+3.3V
D_GND C584 470nF;0402
D_GND C588 470nF;0402

D_+1.8V
D_GND C589 470nF;0402
D_GND C583 470nF;0402
D_GND C587 470nF;0402
D_GND C582 470nF;0402
D_GND C585 470nF;0402

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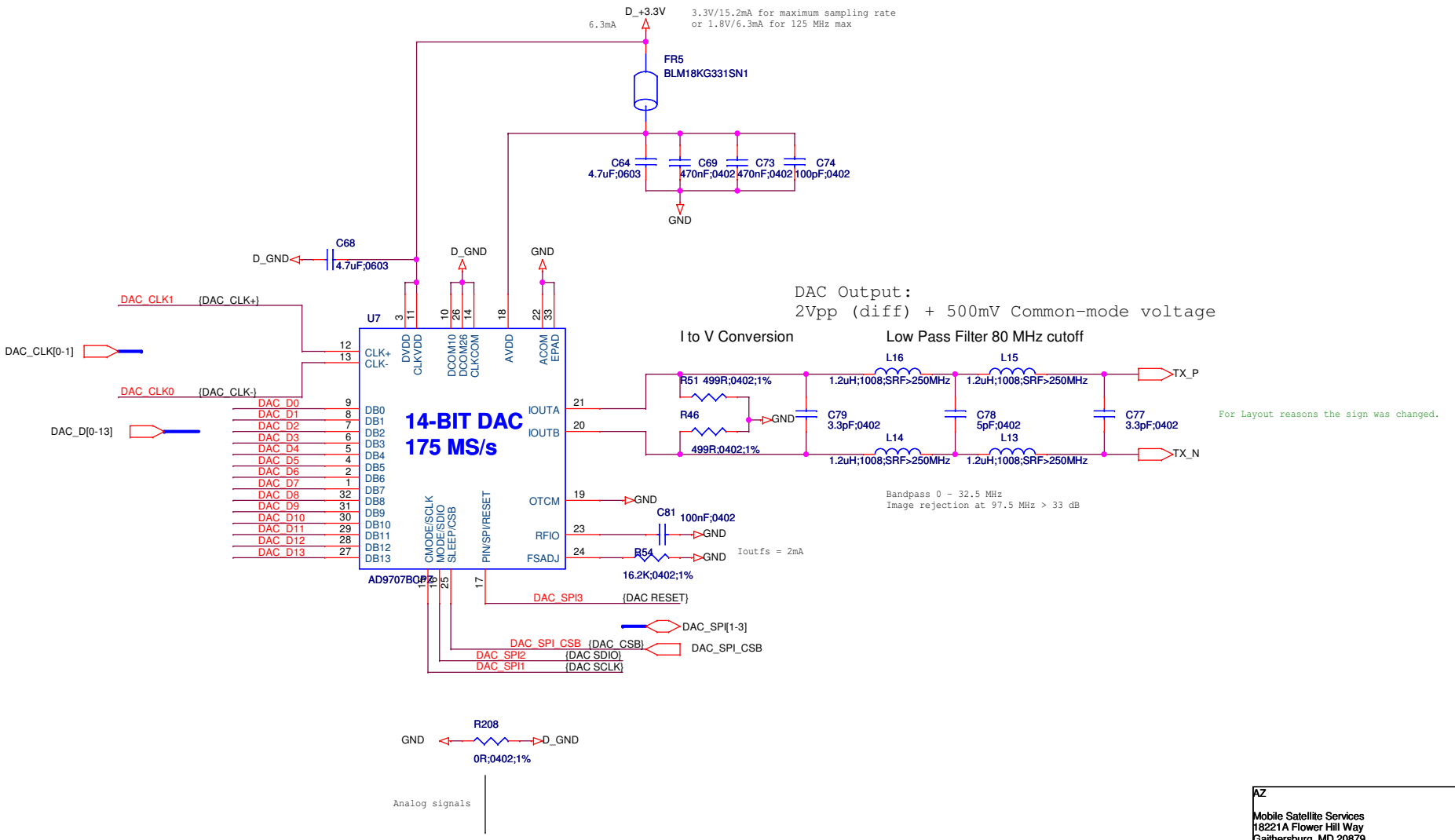
18221A Flower Hill Way
Gaithersburg, MD 20879
USA

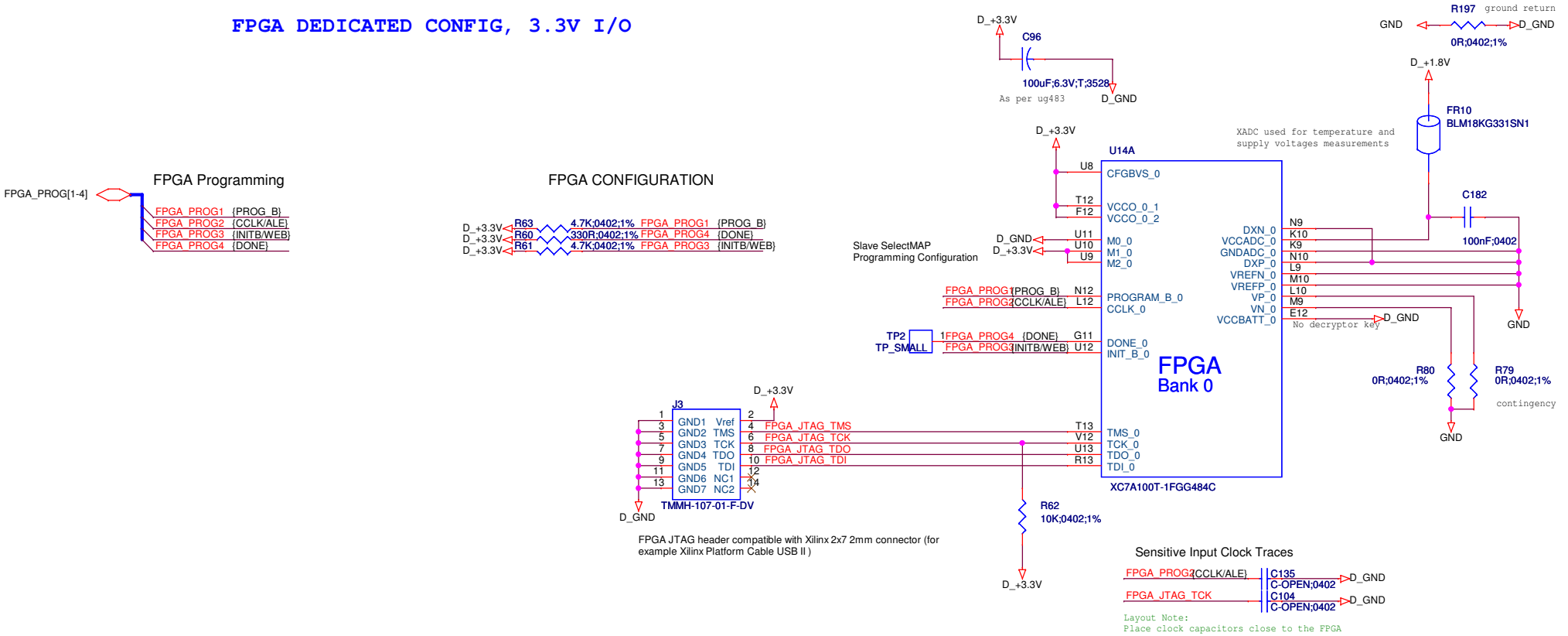
Title: TURBO CODE
Size: B
Document Number: Y13002
Rev: 0
Date: Thursday, September 25, 2014
Sheet 6 of 6

DAC (1 baseband channel)



AZ Mobile Satellite Services 18221A Flower Hill Way Gaithersburg, MD 20879 USA		
Title: DAC		
Size: B	Document Number: Y13002	Rev: 0
Date: Friday, October 25, 2013	Sheet 6 of 29	

FPGA DEDICATED CONFIG, 3.3V I/O



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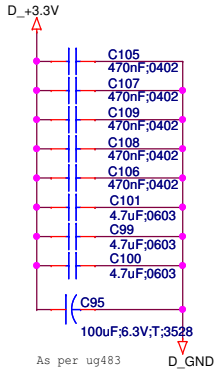
Title: FPGA BANK0

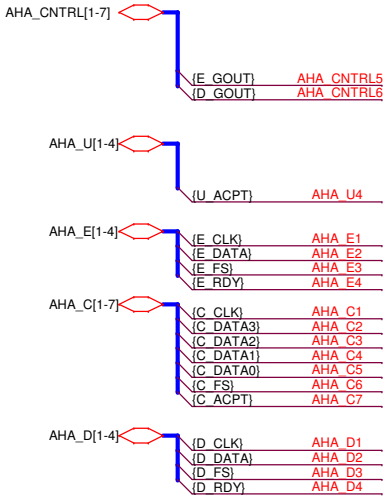
Size	Document Number	Rev
B	Y13002	1

Date: Thursday, September 25, 2014 Sheet 7 of 29

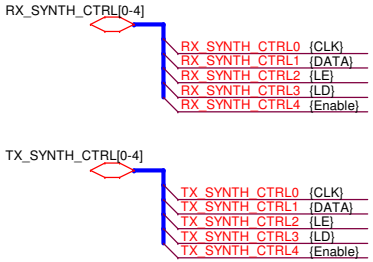
FPGA BANK 13, 3.3V I/O



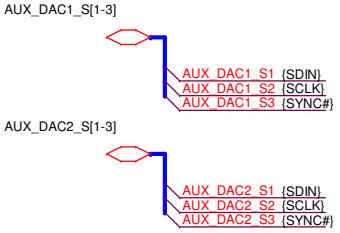
TPC CODEC (TEMP)



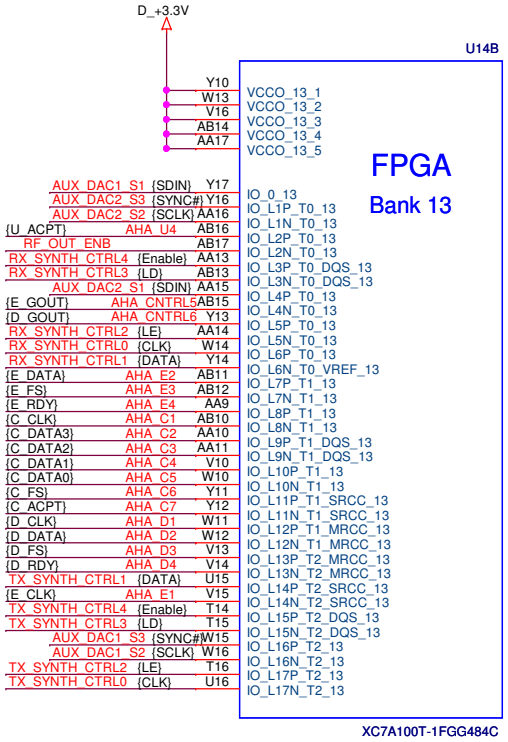
RF frequency synthesizers



RX RF and IF gain controls



TX control



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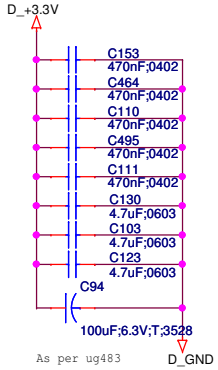
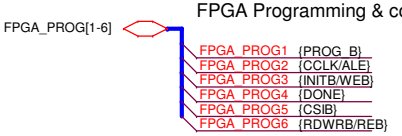
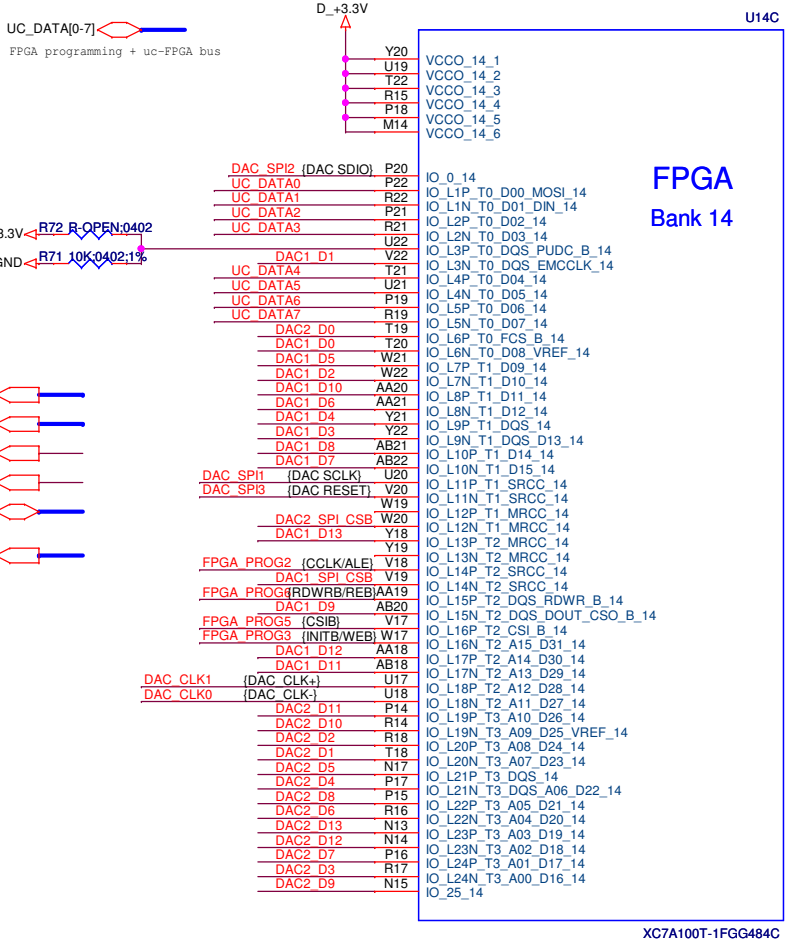
Title	FPGA BANK13	
Size B	Document Number Y13002	Rev 1
Date: Thursday, September 25, 2014	Sheet 8 of 29	

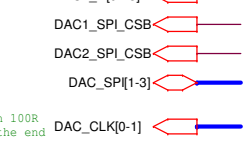
FPGA BANK 14, 3.3V I/O



FPGA Programming & communication







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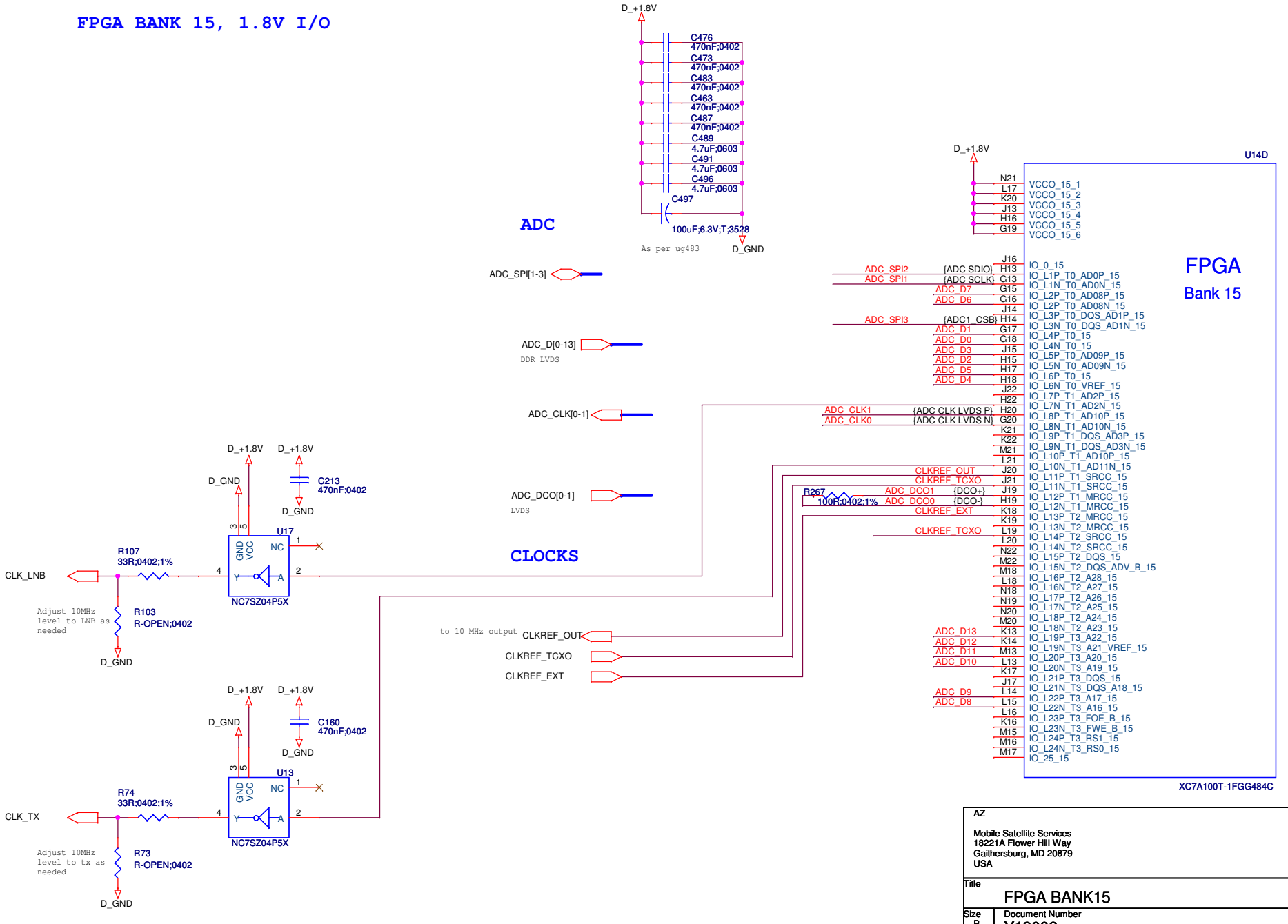
Title	FPGA BANK14	
Size B	Document Number Y13002	Rev 1
Date: Thursday, September 25, 2014	Sheet 9 of 29	

FPGA BANK 15, 1.8V I/O



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Title	FPGA BANK15
Size B	Document Number Y13002 Rev 1
Date: Wednesday, October 01, 2014	Sheet 10 of 29

FPGA BANK 16, 2.5V I/O

TPC CODEC (TEMP)

AHA_CNTRL[1-7]
- {RESET_N} AHA_CNTRL1
- {PLL_SYSCLK} AHA_CNTRL2
- {E_CS_N} AHA_CNTRL3
- {D_CS_N} AHA_CNTRL4
- {PLL_BYPASS} AHA_CNTRL7

AHA_U[1-4]
- {U_CLK} AHA_U1
- {U_DATA} AHA_U2
- {U_FS} AHA_U3

D_+2.5V

C186 470nF;0402
C192 470nF;0402
C195 470nF;0402
C207 470nF;0402
C208 470nF;0402
C211 4.7uF;0603
C210 4.7uF;0603
C209 4.7uF;0603
C218 100uF;6.3V;T;3528

As per ug483

D_GND

LAN PHY #1

LAN1_CTRL_[1-5]
- LAN1_CTRL_1 {CLK125_NDO}
- LAN1_CTRL_2 {INT_N}
- LAN1_CTRL_3 {RESET_N}
- LAN1_CTRL_4 {MDC}
- LAN1_CTRL_5 {MDIO}

LAN1_TX_[1-6]
- LAN1_TX_1 {GTX_CLK}
- LAN1_TX_2 {TX_EN}
- LAN1_TX_3 {TXD0}
- LAN1_TX_4 {TXD1}
- LAN1_TX_5 {TXD2}
- LAN1_TX_6 {TXD3}

LAN1_RX_[1-6]
- LAN1_RX_1 {RX_CLK}
- LAN1_RX_2 {RX_DV}
- LAN1_RX_3 {RXD0}
- LAN1_RX_4 {RXD1}
- LAN1_RX_5 {RXD2}
- LAN1_RX_6 {RXD3}

LAN PHY #2

LAN2_CTRL_[2-5]
- LAN2_CTRL_2 {INT_N}
- LAN2_CTRL_3 {RESET_N}
- LAN2_CTRL_4 {MDC}
- LAN2_CTRL_5 {MDIO}

LAN2_TX_[1-6]
- LAN2_TX_1 {GTX_CLK}
- LAN2_TX_2 {TX_EN}
- LAN2_TX_3 {TXD0}
- LAN2_TX_4 {TXD1}
- LAN2_TX_5 {TXD2}
- LAN2_TX_6 {TXD3}

LAN2_RX_[1-6]
- LAN2_RX_1 {RX_CLK}
- LAN2_RX_2 {RX_DV}
- LAN2_RX_3 {RXD0}
- LAN2_RX_4 {RXD1}
- LAN2_RX_5 {RXD2}
- LAN2_RX_6 {RXD3}

LED PIPES

D1
LED PIPE
D2
LED PIPE
D3
LED PIPE

front-panel LEDs layout:
- LIGHT PIPE 3MM 2POS RA BEND SMD Lumex P/N LPF-C012303S
- LED: 0603, <90deg viewing angle, 10mA

D9 R11 LED2 GREEN LED 49.9R;0402;1%
D4 R1 LED3 GREEN LED 49.9R;0402;1%
D8 R10 LED4 GREEN LED 49.9R;0402;1%
D5 R2 LED5 YELLOW LED 49.9R;0402;1%
D7 R9 LED6 YELLOW LED 49.9R;0402;1%

D_GND

D_+2.5V

U14E

VCCO_16_1 F22
VCCO_16_2 E15
VCCO_16_3 D18
VCCO_16_4 C21
VCCO_16_5 B14
VCCO_16_6 A17

FPGA
Bank 16

LAN1_TX_2	{TX_EN}	F15
LAN1_TX_6	{TXD3}	F13
LAN1_RX_3	{RXD0}	F14
LAN1_CTRL_3	{RESET_N}	F16
LAN2_TX_1	{GTX_CLK}	E17
LAN1_RX_6	{RXD3}	C14
LAN1_CTRL_4	{MDC}	C15
LAN1_TX_5	{TXD2}	E13
LAN1_RX_4	{RXD1}	E14
LAN2_TX_6	{TXD3}	E16
LAN2_TX_5	{TXD2}	D16
LAN1_RX_5	{RXD2}	D14
{RESET_N}	AHA_CNTRL1	D15
LAN1_CTRL_5	{MDIO}	B15
LAN2_TX_4	{TXD1}	B16
LAN1_TX_4	{TXD1}	C13
LAN1_TX_3	{TXD0}	B13
LAN1_CTRL_2	{INT_N}	A15
LAN2_TX_3	{TXD0}	A16
LAN1_TX_1	{GTX_CLK}	A13
LAN1_RX_2	{RX_DV}	A14
{PLL_BYPASS}	AHA_CNTRL7	B17
{E_CS_N}	AHA_CNTRL3	B18
LAN1_CTRL_1	{CLK125_NDO}	D17
LAN1_RX_1	{RX_CLK}	C17
{D_CS_N}	AHA_CNTRL4	C18
LAN2_RX_1	{RX_CLK}	C19
{PLL_SYSCLK}	AHA_CNTRL2	E19
{U_CLK}	AHA_U1	D19
LAN2_TX_2	{TX_EN}	F18
LAN2_RX_6	{RXD3}	E18
{U_DATA}	AHA_U2	B20
LAN2_CTRL_2	{INT_N}	A20
LAN2_CTRL_4	{MDC}	A18
LAN2_CTRL_5	{MDIO}	A19
LAN2_RX_5	{RXD2}	F19
LAN2_RX_4	{RXD1}	F20
{U_FS}	AHA_U3	D20
	LED2	C20
	LED3	C22
	LED4	B22
	LED5	B21
LAN2_CTRL_3	{RESET_N}	A21
		E22
		D22
		E21
		D21
LAN2_RX_2	{RX_DV}	G21
	LED6	G22
LAN2_RX_3	{RXD0}	F21

IO_0_16
IO_L1P_T0_16
IO_L1N_T0_16
IO_L2P_T0_16
IO_L2N_T0_16
IO_L3P_T0_DQS_16
IO_L3N_T0_DQS_16
IO_L4P_T0_16
IO_L4N_T0_16
IO_L5P_T0_16
IO_L5N_T0_16
IO_L6P_T0_16
IO_L6N_T0_VREF_16
IO_L7P_T1_16
IO_L7N_T1_16
IO_L8P_T1_16
IO_L8N_T1_16
IO_L9P_T1_DQS_16
IO_L9N_T1_DQS_16
IO_L10P_T1_16
IO_L10N_T1_16
IO_L11P_T1_SRCC_16
IO_L11N_T1_SRCC_16
IO_L12P_T1_MRCC_16
IO_L12N_T1_MRCC_16
IO_L13P_T2_MRCC_16
IO_L13N_T2_MRCC_16
IO_L14P_T2_SRCC_16
IO_L14N_T2_SRCC_16
IO_L15P_T2_DQS_16
IO_L15N_T2_DQS_16
IO_L16P_T2_16
IO_L16N_T2_16
IO_L17P_T2_16
IO_L17N_T2_16
IO_L18P_T2_16
IO_L18N_T2_16
IO_L19P_T3_16
IO_L19N_T3_VREF_16
IO_L20P_T3_16
IO_L20N_T3_16
IO_L21P_T3_DQS_16
IO_L21N_T3_DQS_16
IO_L22P_T3_16
IO_L22N_T3_16
IO_L23P_T3_16
IO_L23N_T3_16
IO_L24P_T3_16
IO_L24N_T3_16
IO_25_16

XC7A100T-1FGG484C

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Title: FPGA BANK16

Size	Document Number	Rev
B	Y13002	1

Date: Thursday, September 25, 2014 Sheet 11 of 29

FPGA BANKS 34/35, 1.5V I/O

Contingency if more memory is needed for LDPC

U14F

FPGA
Bank 34

XC7A100T-1FGG484C

U14G

FPGA
Bank 35

XC7A100T-1FGG484C

U10

16-Bit
DDR3
SDRAM

MT41J64M16

40 Ohm (single-ended) traces
80 Ohm differential traces

Sensitive. 30mils trace between caps and pin.
shield with gnd. other trace > 15mils away.

Place near SDRAM

DDR3_VREF = 0.75V

Test points

J4

TMMH-107-01-F-DV

Title	
	FPGA BANK34_35 DDR3
Size: C	Document Number: Y13002
Rev: 1	
Date: Wednesday, October 01, 2014	Sheet 12 of 29

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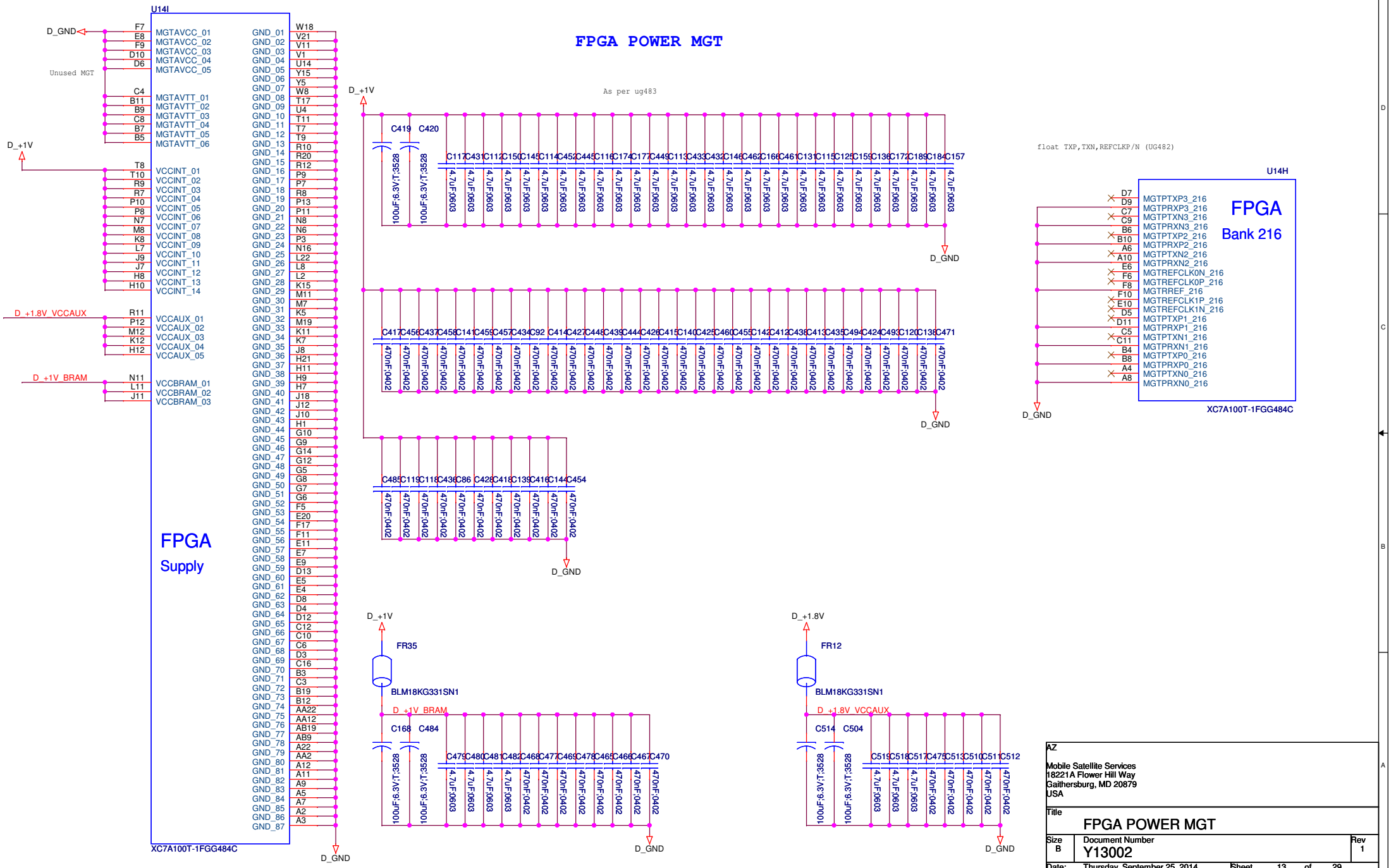
FPGA POWER MGT



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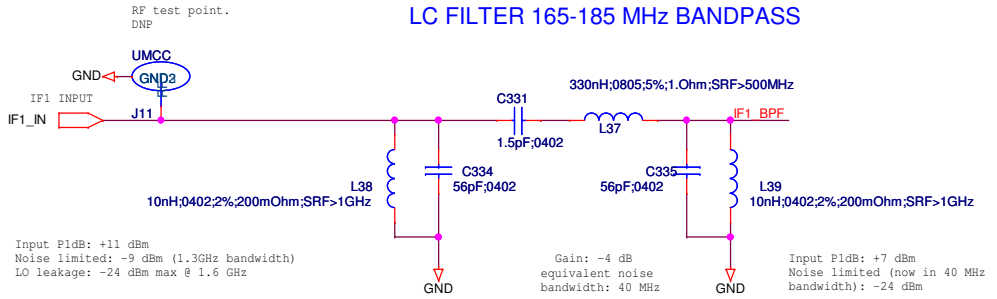
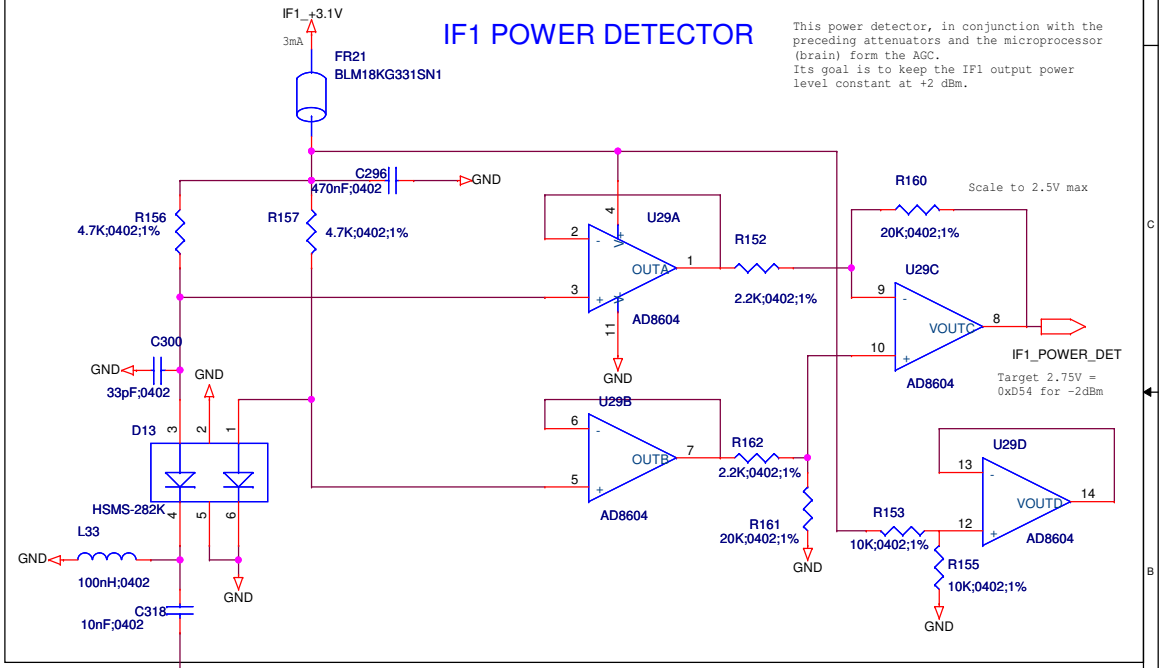
Title	FPGA POWER MGT	
Size B	Document Number Y13002	Rev 1
Date: Thursday, September 25, 2014	Sheet 13 of 29	

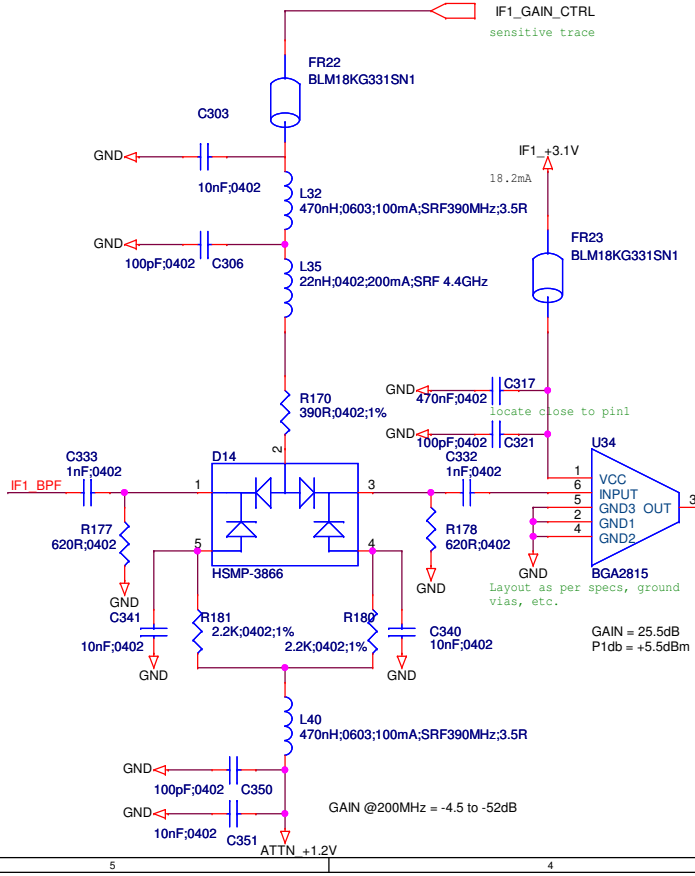
LC FILTER 165-185 MHz BANDPASS

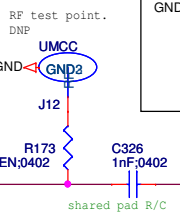


IF1 POWER DETECTOR

This power detector, in conjunction with the preceding attenuators and the microprocessor (brain) form the AGC.
Its goal is to keep the IF1 output power level constant at +2 dBm.







IF1_OUT

DSP module expects a maximum level of 2Vpp differential (1Vpp single-ended)

Signal (agc stable): 2dBm (3.5 dB below P1dB)
= 0.8 Vpp
Worst-case noise power: -3dBm when AGC tracks the noise.

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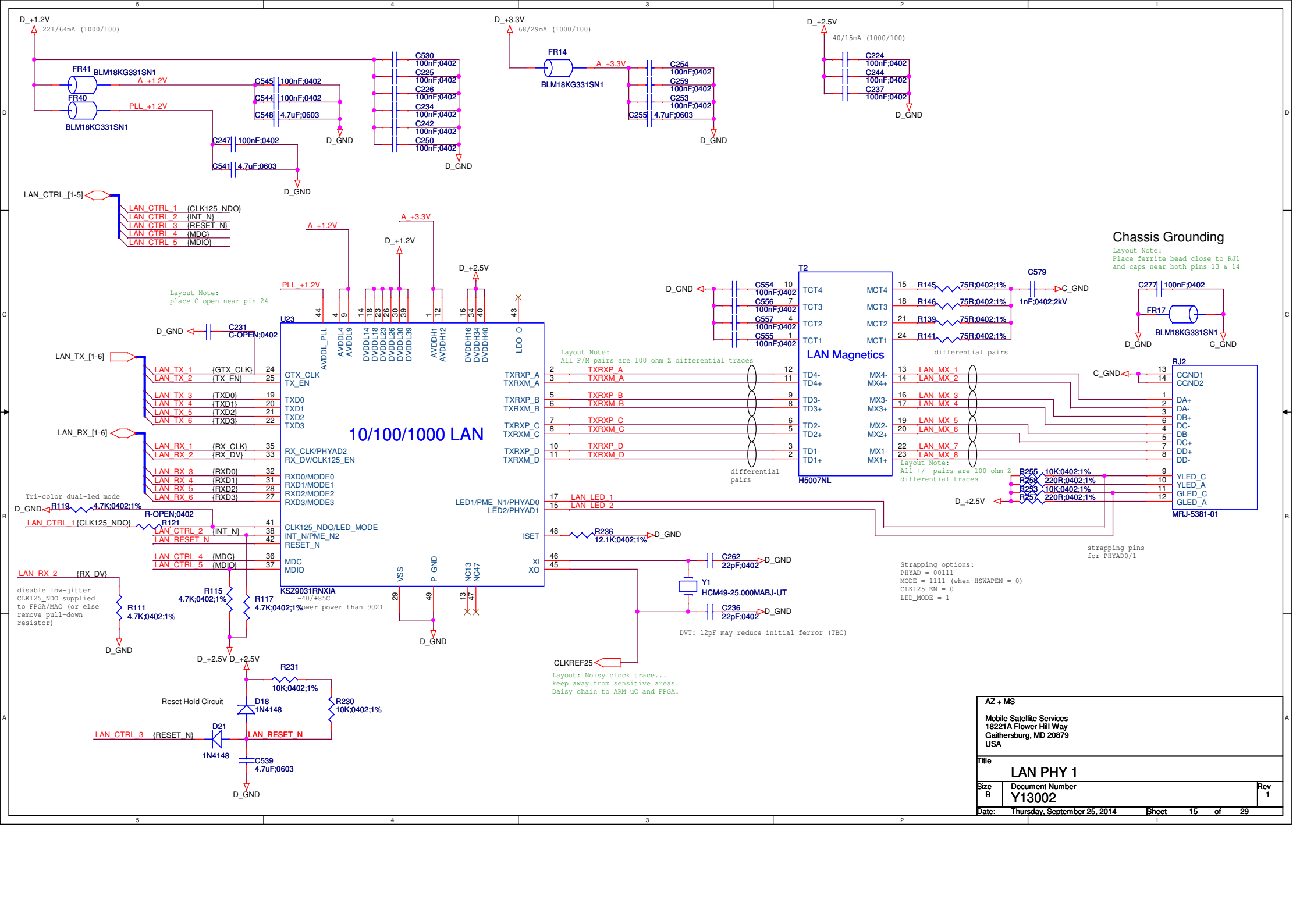
Title	IF1	
Size B	Document Number Y13002	Rev 0
Date: Thursday, September 25, 2014	Sheet 14 of 29	



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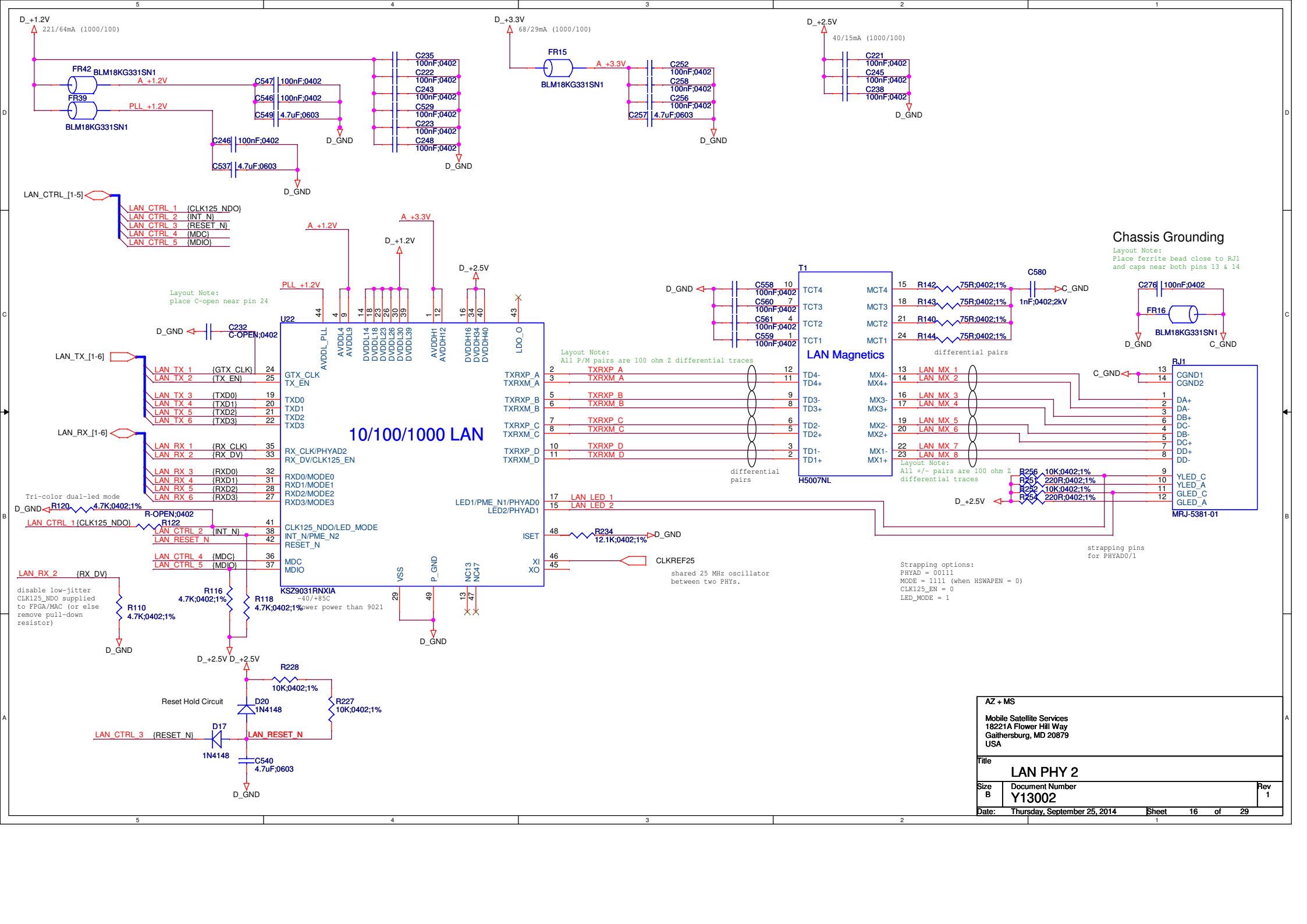
Title: LAN PHY 1

Size: B | Document Number: Y13002 | Rev: 1

Date: Thursday, September 25, 2014 | Sheet 15 of 29



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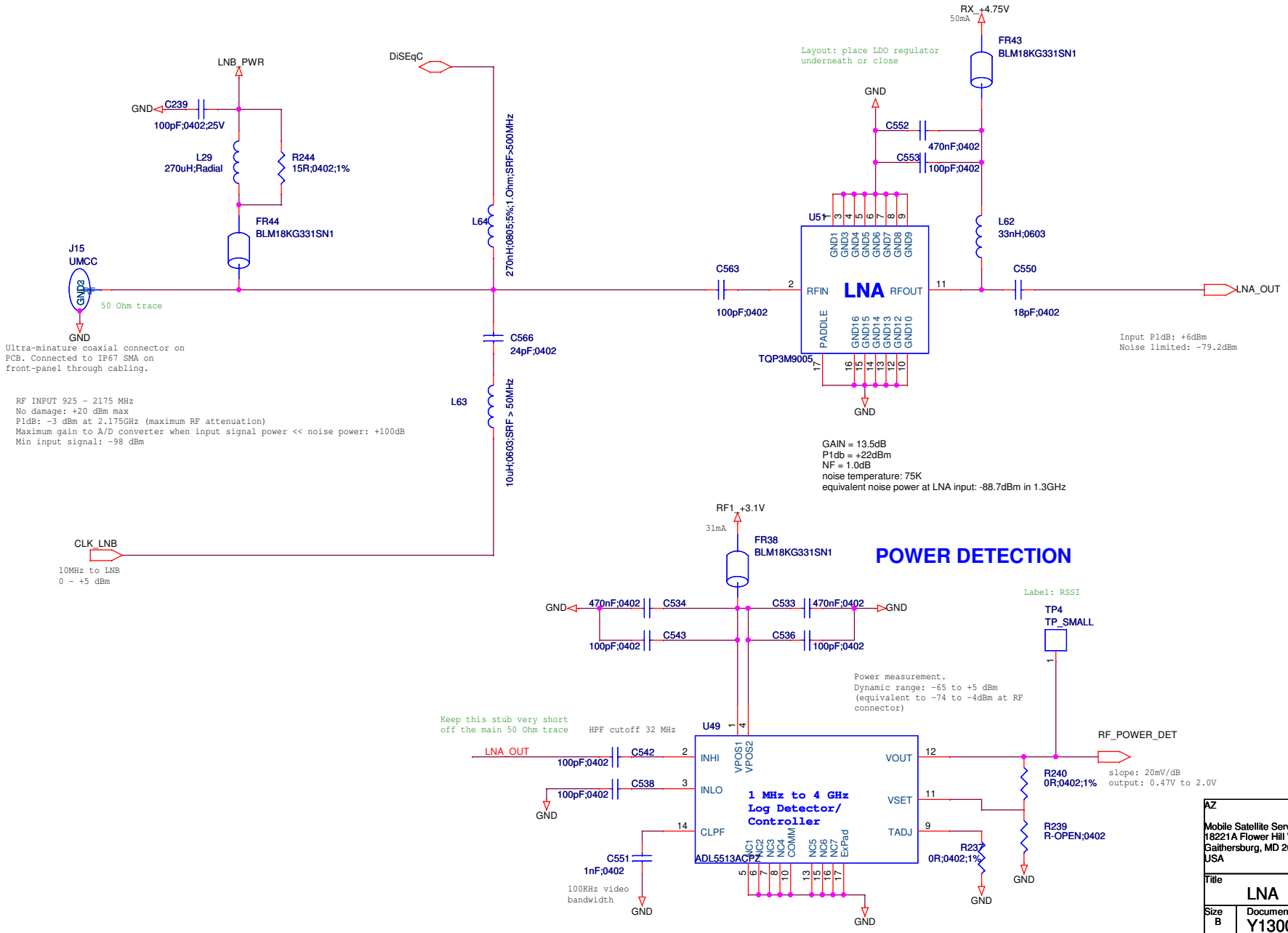
Title: LAN PHY 2

Size	Document Number	Rev
B	Y13002	1

Date: Thursday, September 25, 2014 Sheet 16 of 29



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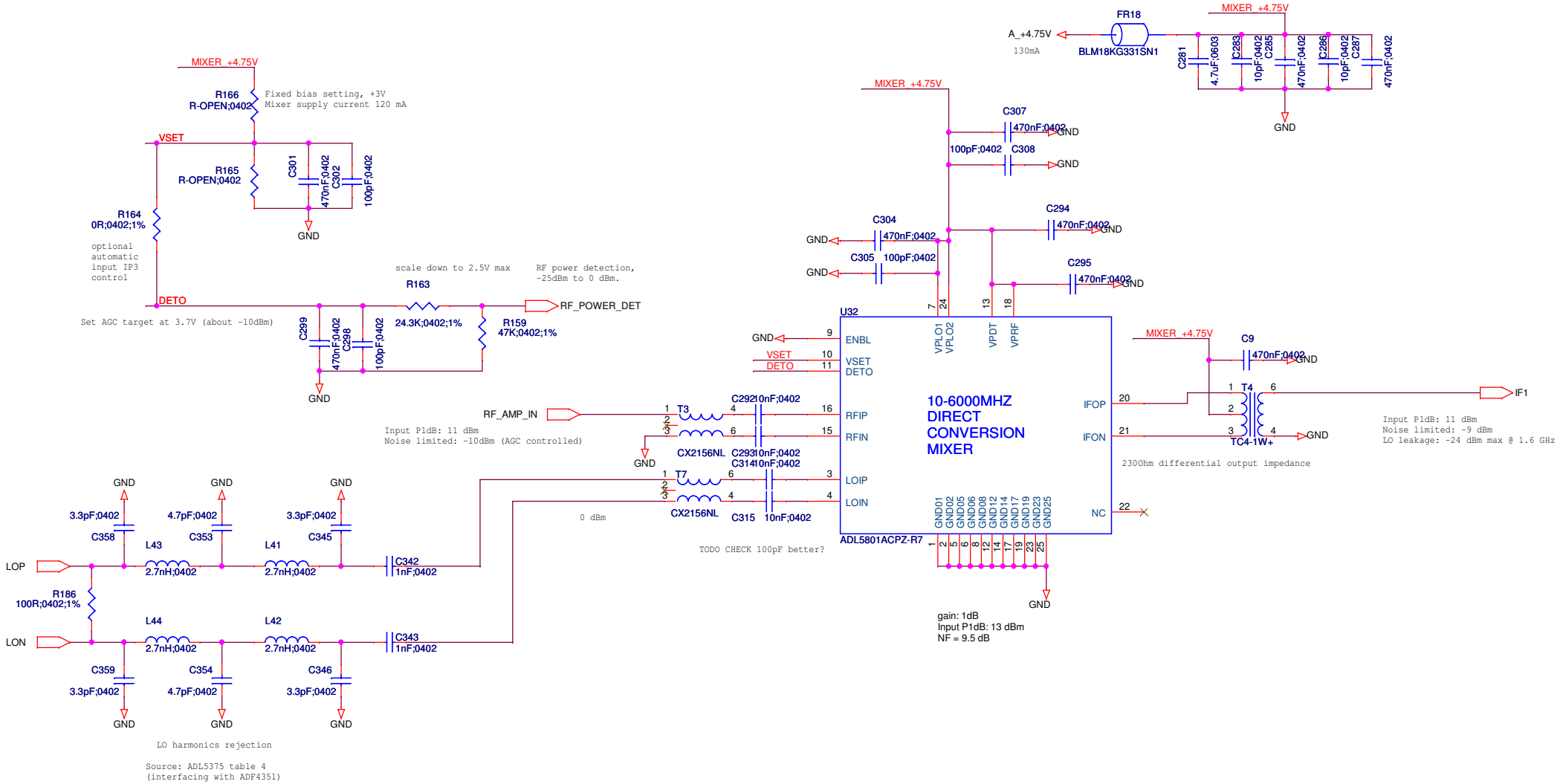
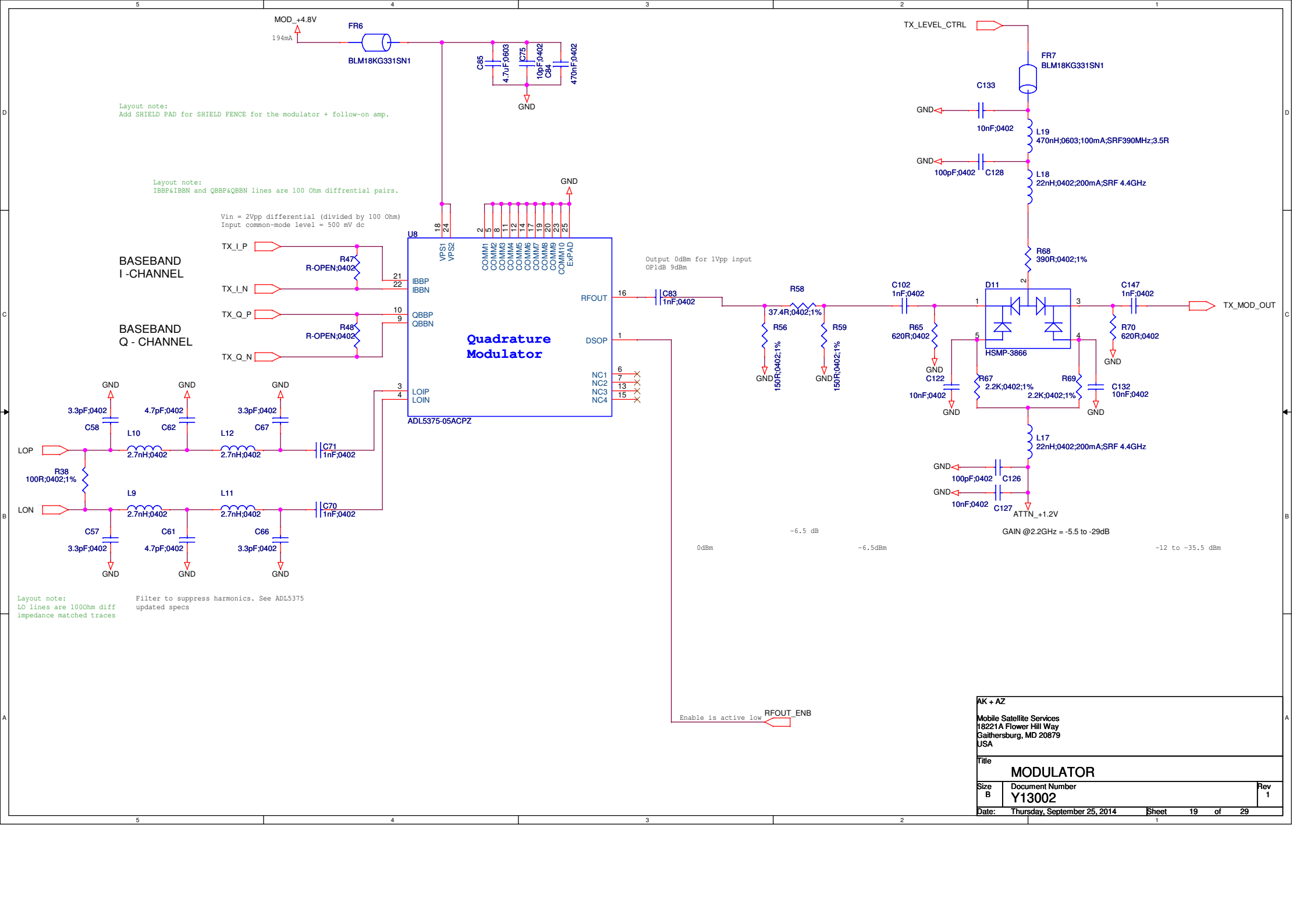
Title	LNA
Size B	Document Number Y13002 Rev 0
Date: Thursday, September 25, 2014	Sheet 17 of 29



AZ Mobile Satellite Services 18221A Flower Hill Way Gaithersburg, MD 20879 USA		
Title: MIXER		
Size: B	Document Number: Y13002	Rev: 0
Date: Friday, October 25, 2013	Sheet 18 of 29	



AK + AZ

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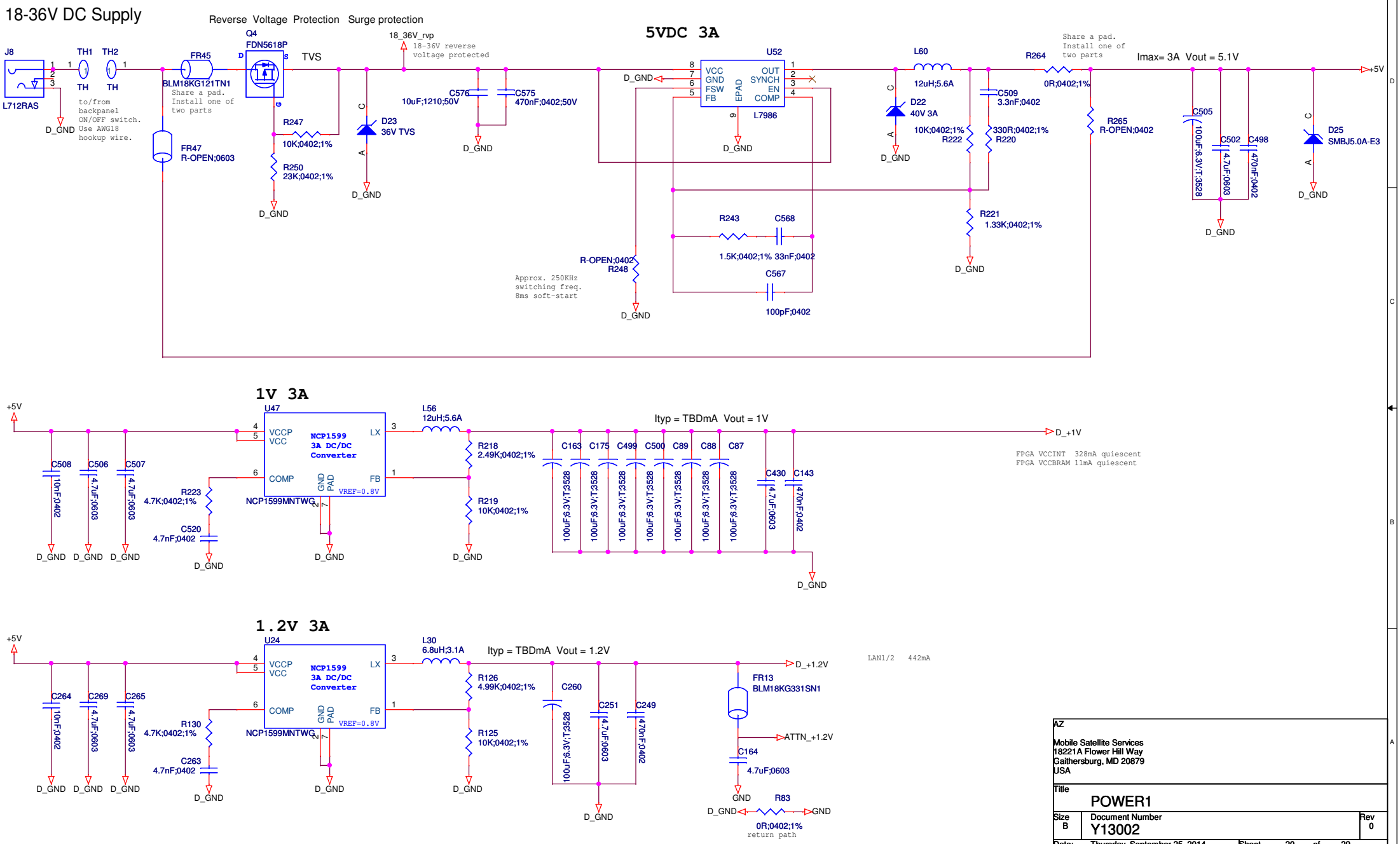
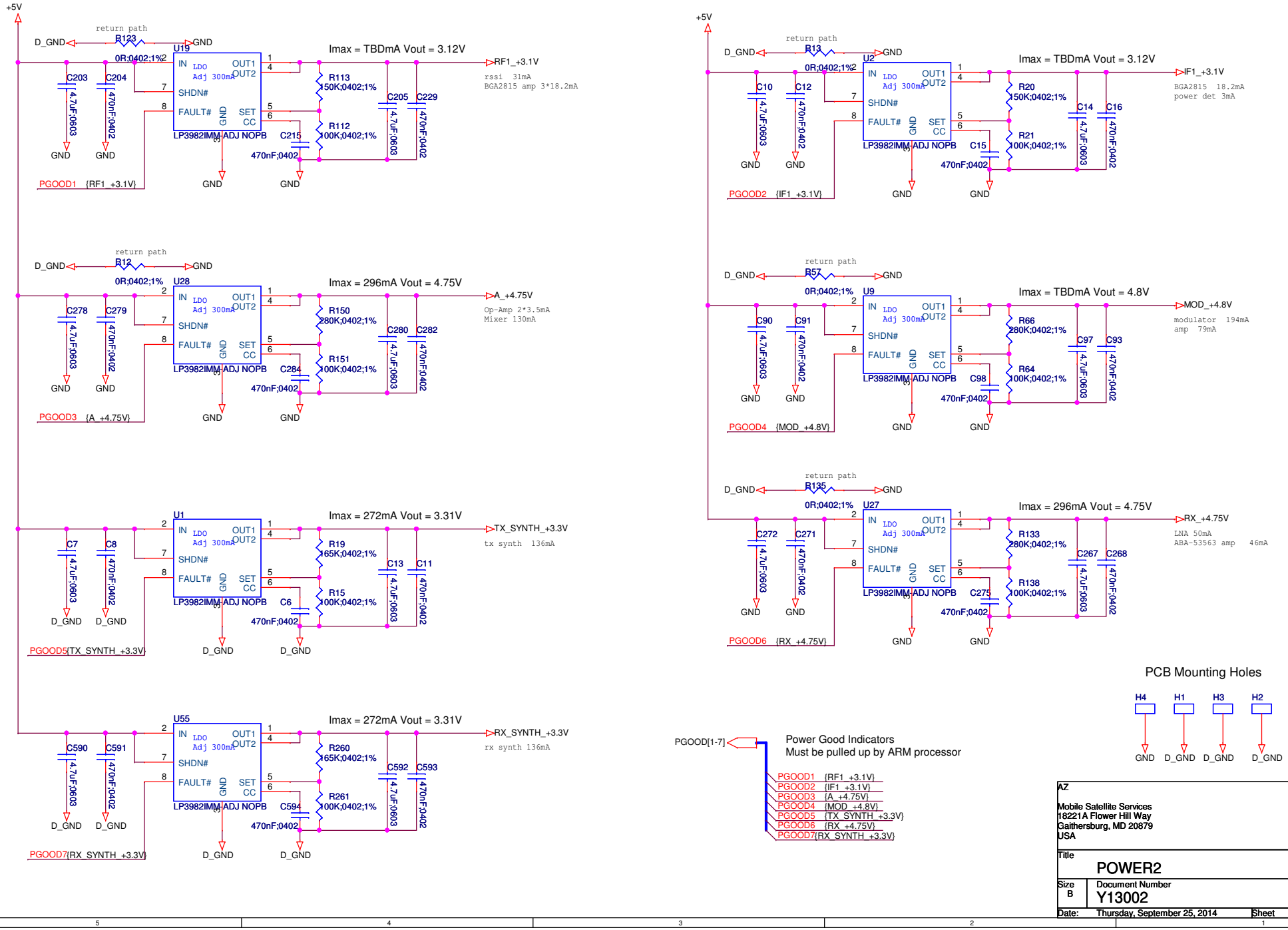
Title: MODULATOR

Size	Document Number	Rev
B	Y13002	1

Date: Thursday, September 25, 2014 Sheet 19 of 29



AZ		
Mobile Satellite Services 18221A Flower Hill Way Gaithersburg, MD 20879 USA		
Title	POWER1	
Size B	Document Number Y13002	Rev 0
Date: Thursday, September 25, 2014	Sheet 20 of 29	


+5V
return path
D_GND
R123
0R;0402;1%
GND
U19
LP3982IMM-ADJ NOPB
IN
OUT1
OUT2
LDO
Adj 300mA
SHDN#
FAULT#
GND
SET
CC
Imax = TBDmA Vout = 3.12V
RF1_+3.1V
rssi 31mA
BGA2815 amp 3*18.2mA
C203
C204
4.7uF;0603
470nF;0402
R113
150K;0402;1%
R112
100K;0402;1%
C205
C229
C215
PGOOD1 {RF1_+3.1V}
R12
U28
Imax = 296mA Vout = 4.75V
A_+4.75V
Op-Amp 2*3.5mA
Mixer 130mA
C278
C279
R150
280K;0402;1%
R151
C280
C282
C284
PGOOD3 {A_+4.75V}
U1
Imax = 272mA Vout = 3.31V
TX_SYNTH_+3.3V
tx synth 136mA
C7
C8
R19
165K;0402;1%
R15
C13
C11
C6
PGOOD5{TX_SYNTH_+3.3V}
U55
Imax = 272mA Vout = 3.31V
RX_SYNTH_+3.3V
rx synth 136mA
C590
C591
R260
165K;0402;1%
R261
C592
C593
C594
PGOOD7{RX_SYNTH_+3.3V}
R13
U2
Imax = TBDmA Vout = 3.12V
IF1_+3.1V
BGA2815 18.2mA
power det 3mA
C10
C12
R20
150K;0402;1%
R21
C14
C16
C15
PGOOD2 {IF1_+3.1V}
R57
U9
Imax = TBDmA Vout = 4.8V
MOD_+4.8V
modulator 194mA
amp 79mA
C90
C91
R66
280K;0402;1%
R64
C97
C93
C98
PGOOD4 {MOD_+4.8V}
R135
U27
Imax = 296mA Vout = 4.75V
RX_+4.75V
LNA 50mA
ABA-53563 amp 46mA
C272
C271
R133
280K;0402;1%
R138
C267
C268
C275
PGOOD6 {RX_+4.75V}
PGOOD[1-7]
Power Good Indicators
Must be pulled up by ARM processor
PGOOD1 {RF1_+3.1V}
PGOOD2 {IF1_+3.1V}
PGOOD3 {A_+4.75V}
PGOOD4 {MOD_+4.8V}
PGOOD5 {TX_SYNTH_+3.3V}
PGOOD6 {RX_+4.75V}
PGOOD7{RX_SYNTH_+3.3V}
PCB Mounting Holes
H4
H1
H3
H2
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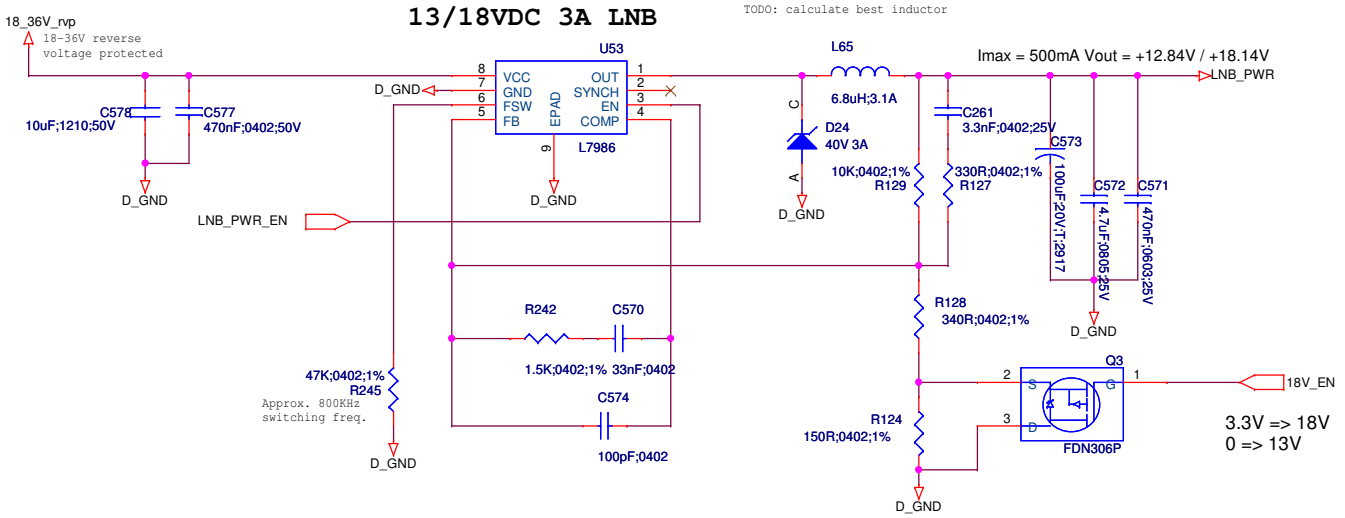
USA
Title
POWER2
Size
B
Document Number
Y13002
Rev
0
Date: Thursday, September 25, 2014
Sheet 21 of 29



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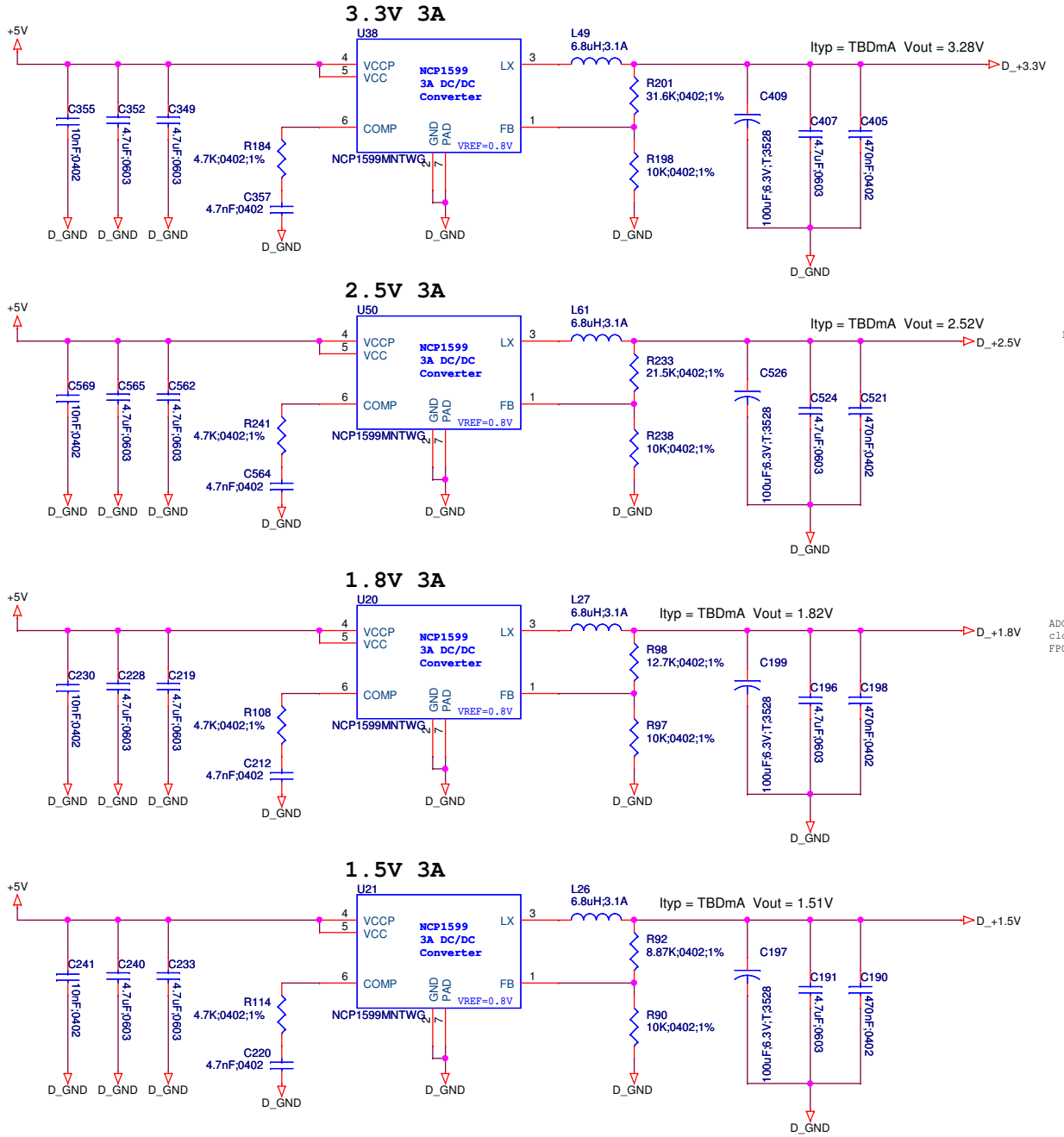
Title: POWER3		
Size: B	Document Number: Y13002	Rev: 0
Date: Thursday, September 25, 2014	Sheet 22 of 29	



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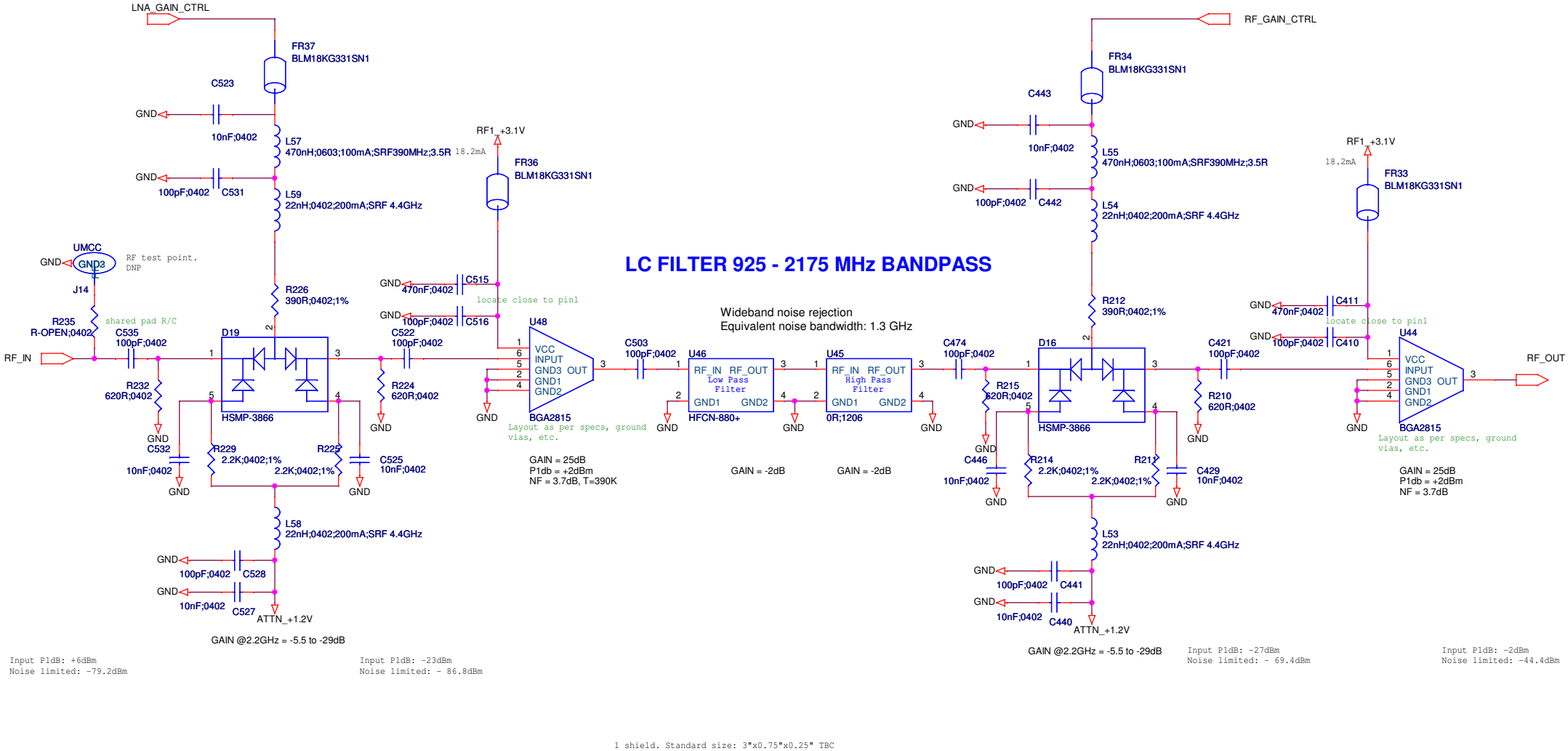
Title: POWER4

Size	Document Number	Rev
B	Y13002	0

Date: Thursday, September 25, 2014 Sheet 23 of 29



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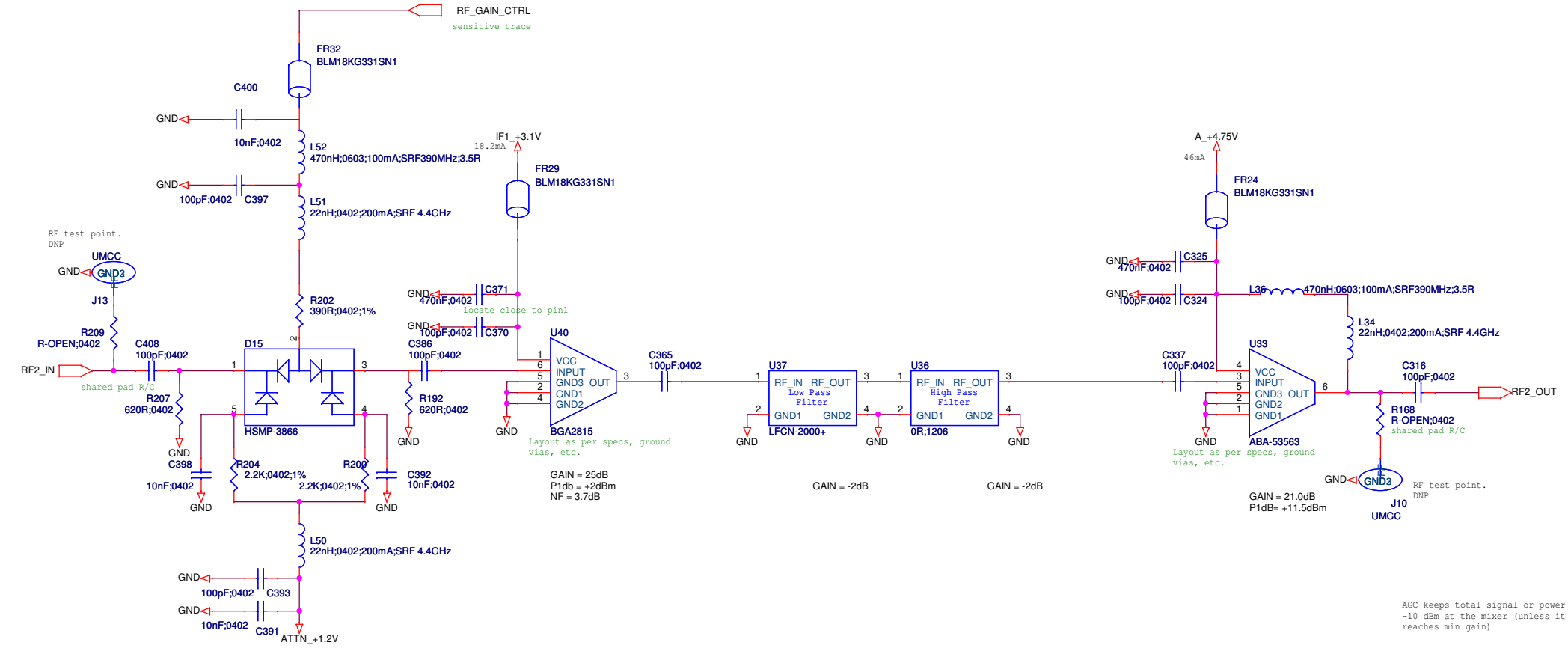
Title	RF1	
Size B	Document Number Y13002	Rev 0
Date: Friday, September 26, 2014	Sheet 24 of 29	



1 shield. Standard size: 1.125"x0.75"x0.25" (TBC)

AZ

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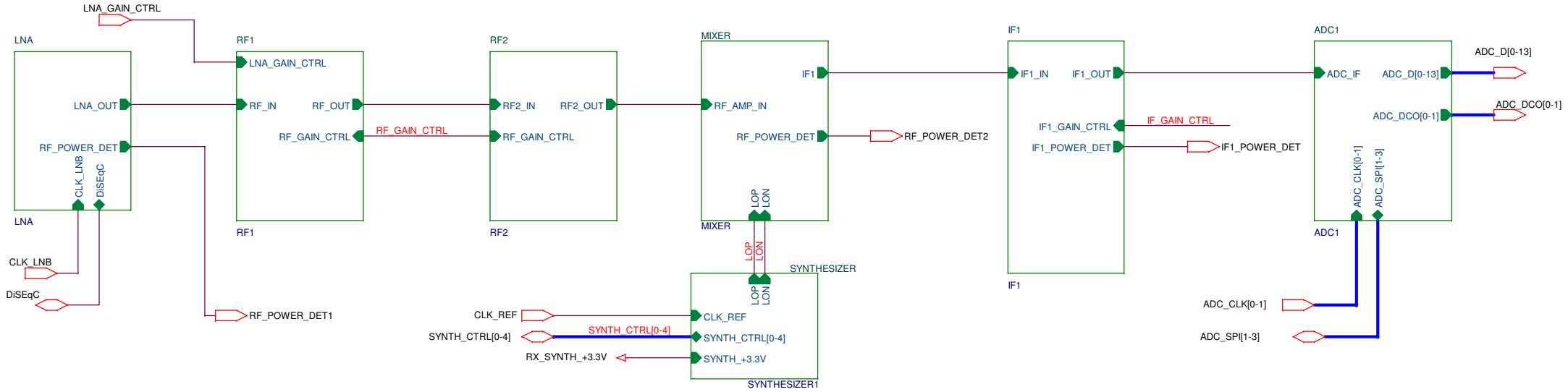
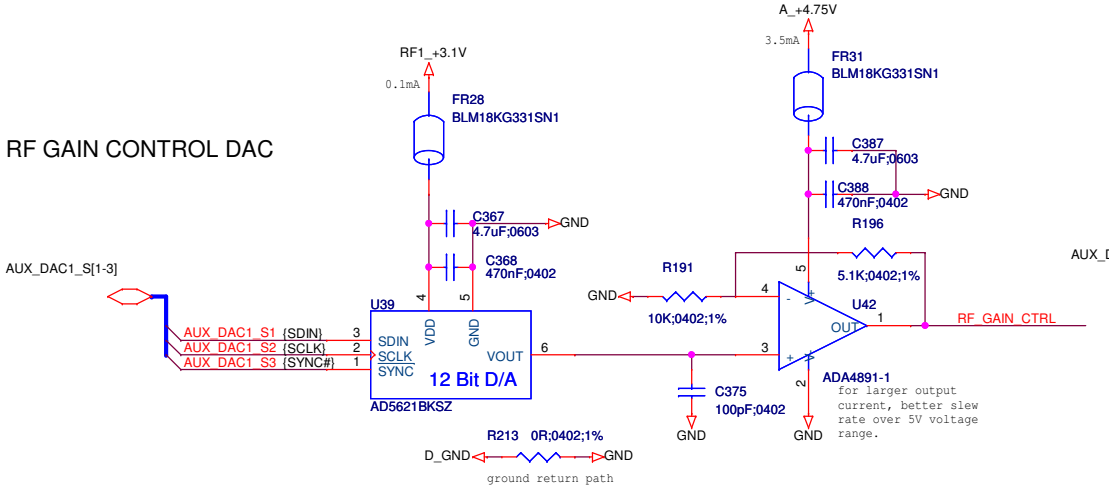
Title: RF2

Size	Document Number	Rev
B	Y13002	0

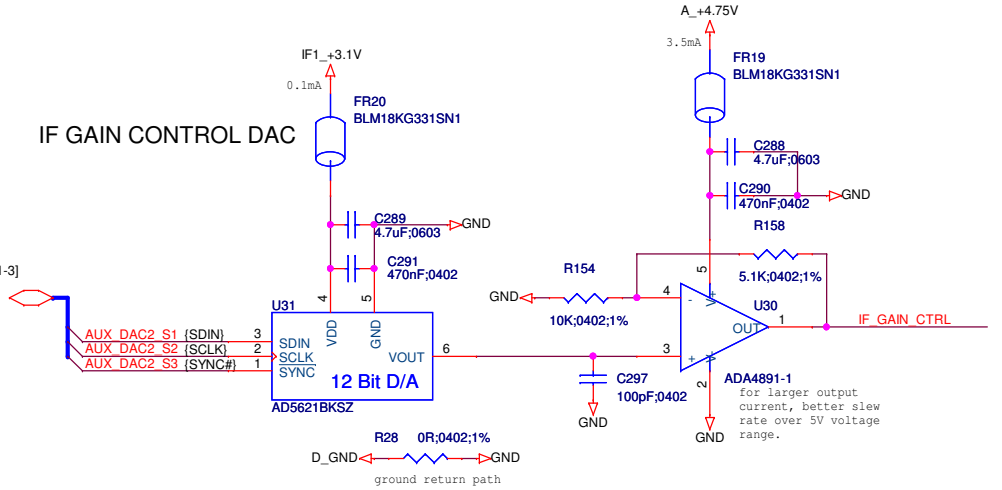
Date: Friday, September 26, 2014 Sheet 25 of 29



RF GAIN CONTROL DAC



IF GAIN CONTROL DAC



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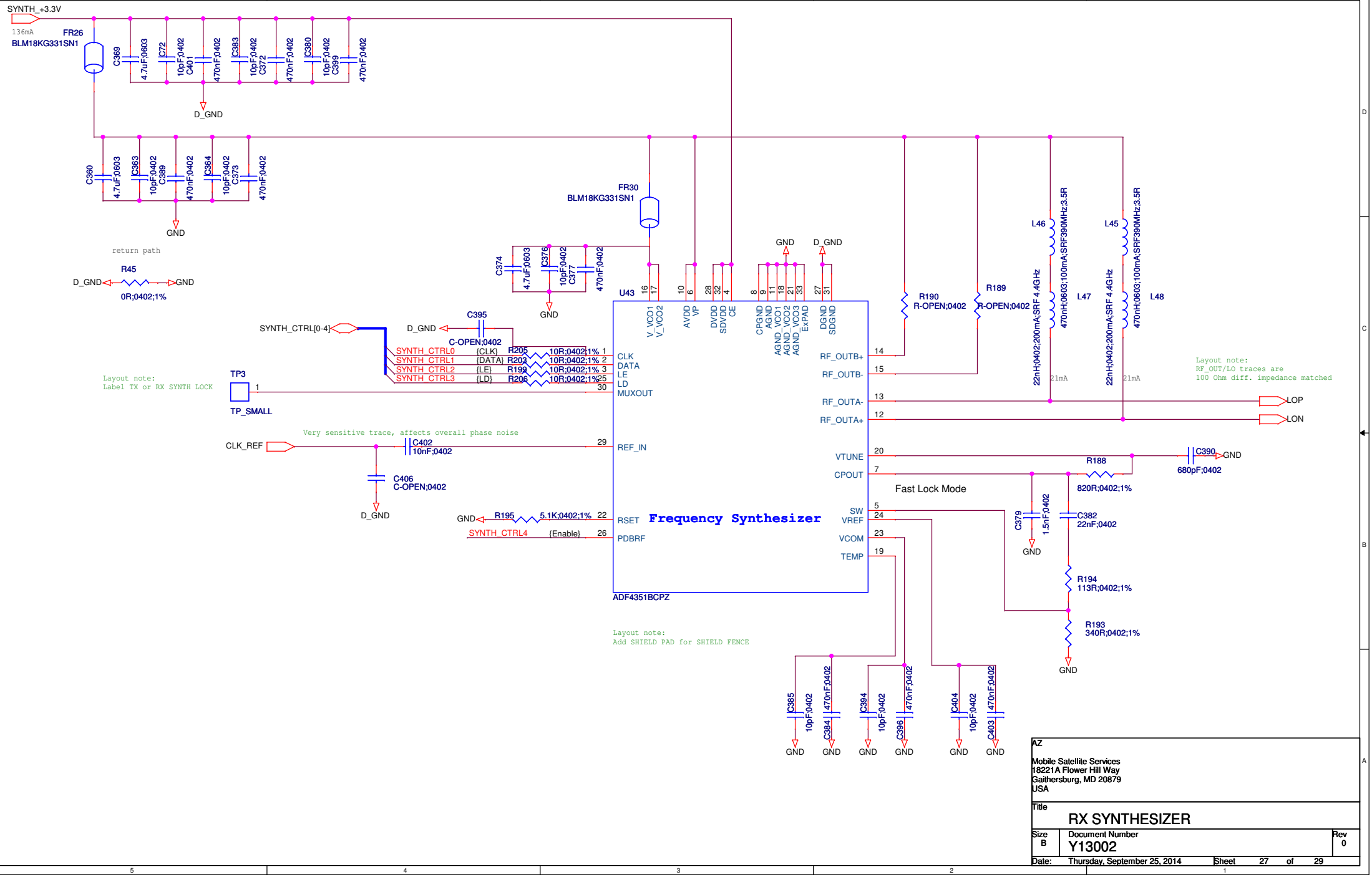
Title: RX		
Size: B	Document Number: Y13001	Rev: 0
Date: Thursday, September 25, 2014	Sheet 26 of 29	



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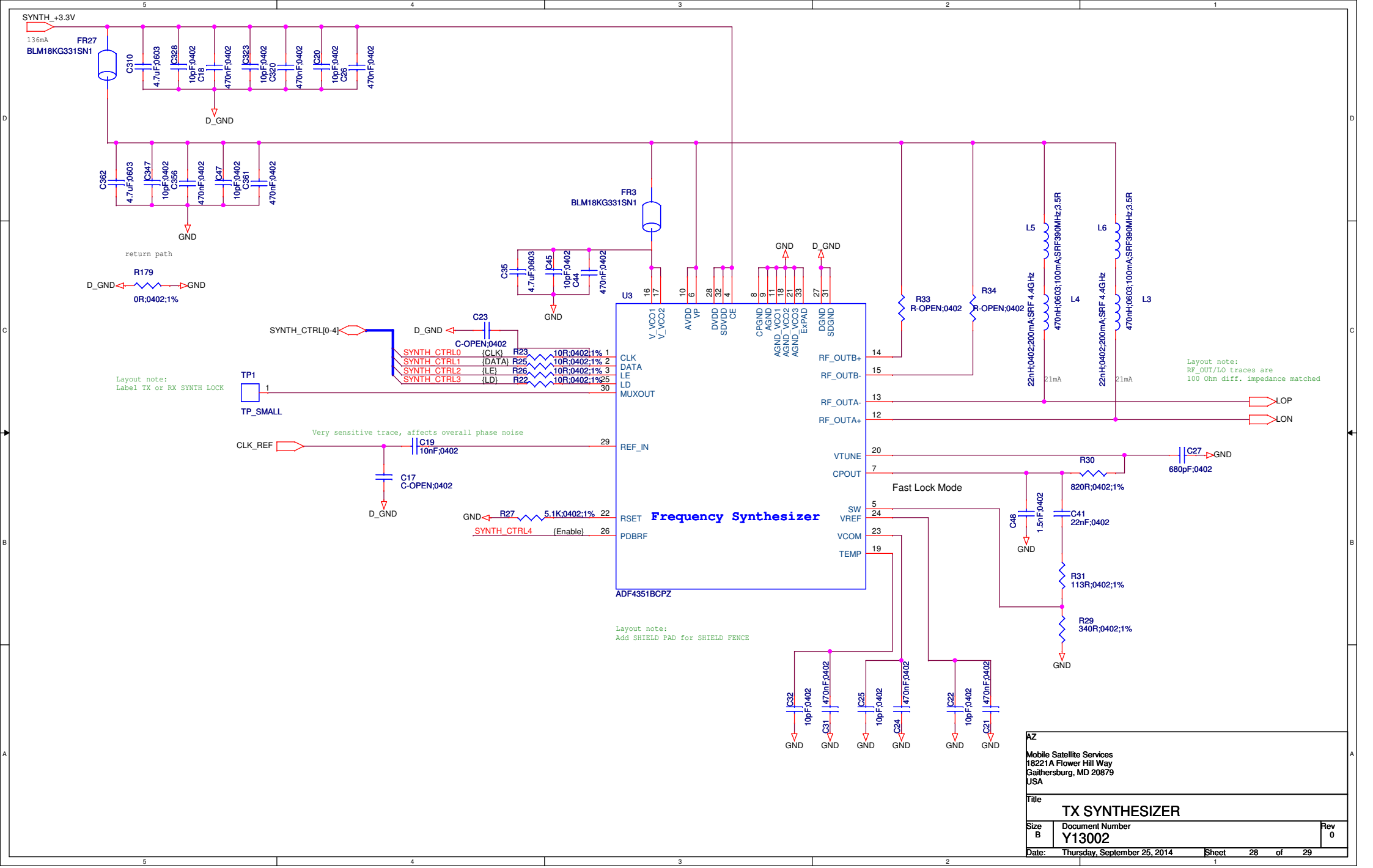
Title: RX SYNTHESIZER

Size	Document Number	Rev
B	Y13002	0

Date: Thursday, September 25, 2014 Sheet 27 of 29



AZ	
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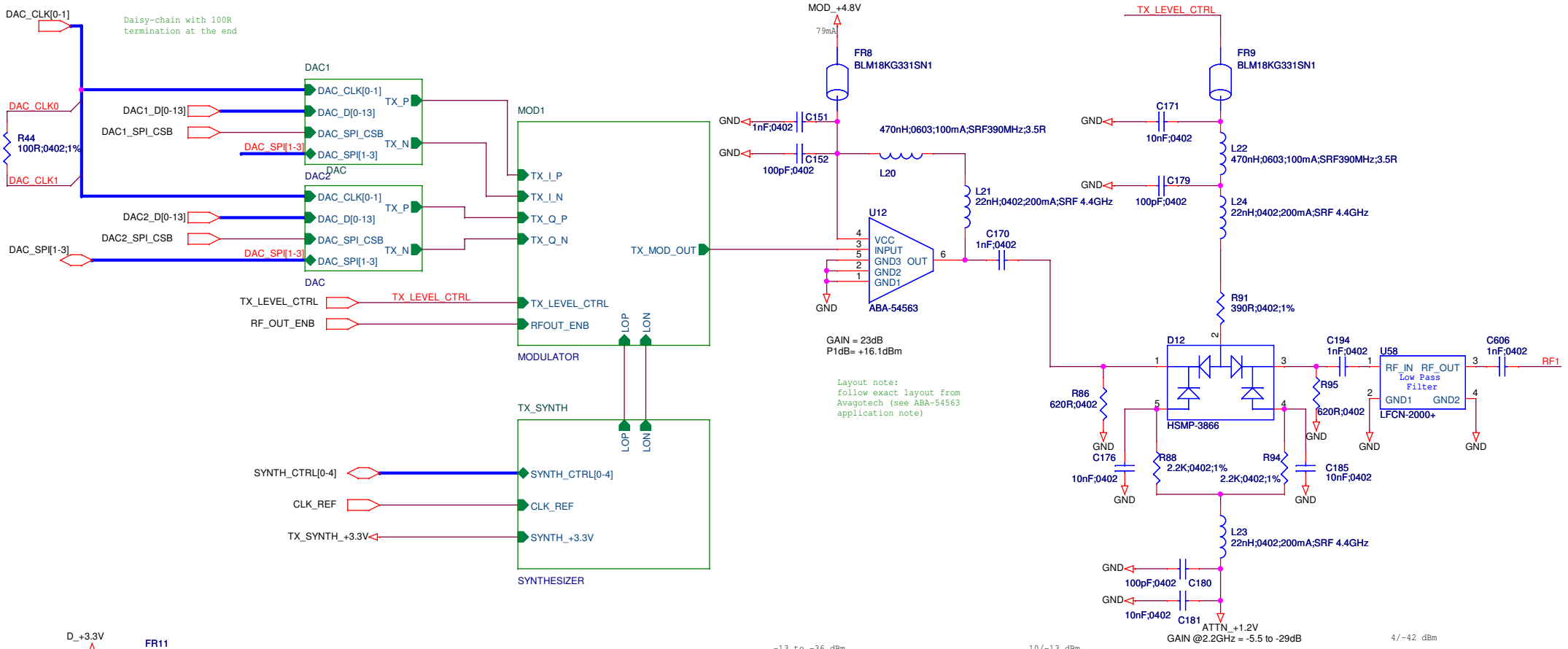
Title	TX SYNTHESIZER
Size B	Document Number Y13002 Rev 0
Date: Thursday, September 25, 2014	Sheet 28 of 29



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Title	TX	
Size B	Document Number Y13002	Rev 1
Date: Friday, September 26, 2014	Sheet 29 of 29	