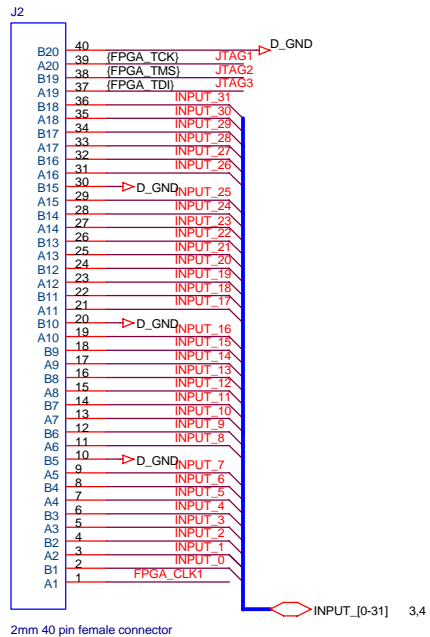


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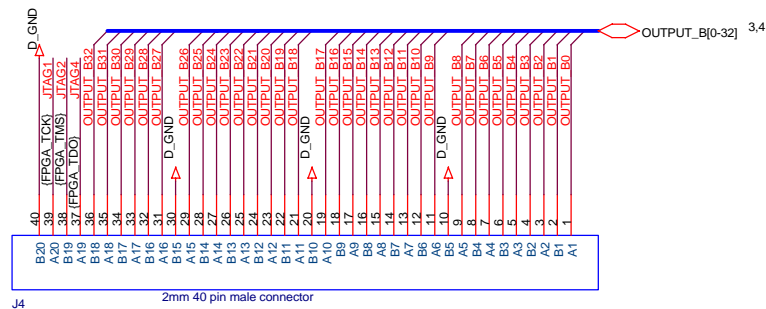
MAIN.....1	MICRO.....4
CONNECTOR.....2	POWER.....5
FPGA.....3	TURBO CODE.....6

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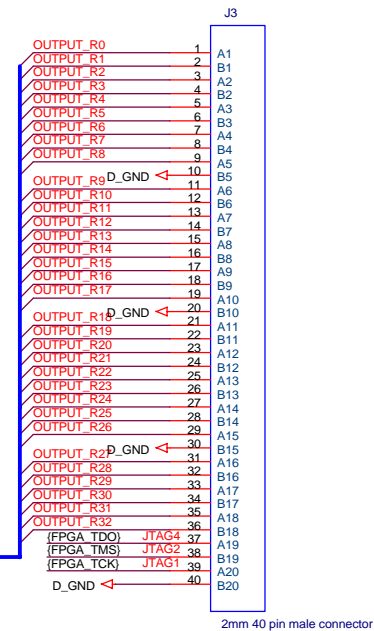
40 Pin INPUT - Left



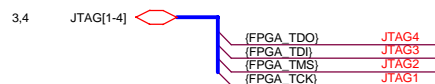
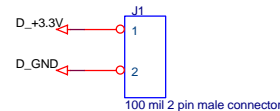
40 Pin OUTPUT - Bottom



40 Pin OUTPUT - Right

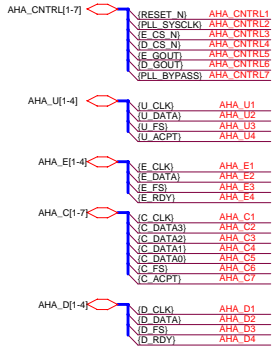


FPGA_CLK1

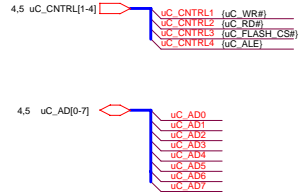


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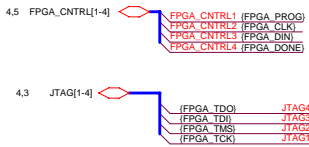
AHA INTERFACE



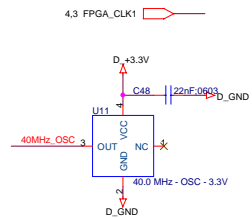
uC INTERFACE



FPGA CONFIGURATION



FPGA CLOCKS



40 PIN INPUT - RIGHT



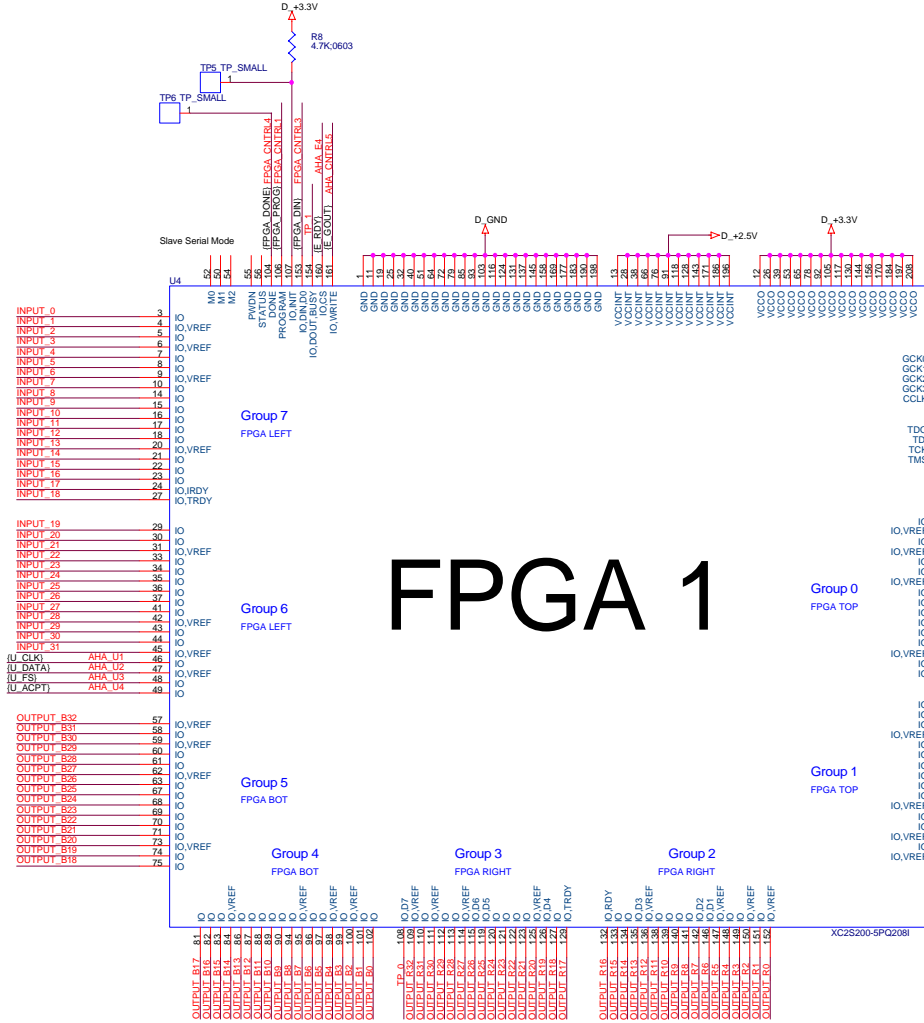
40 PIN OUTPUT - BOTTOM



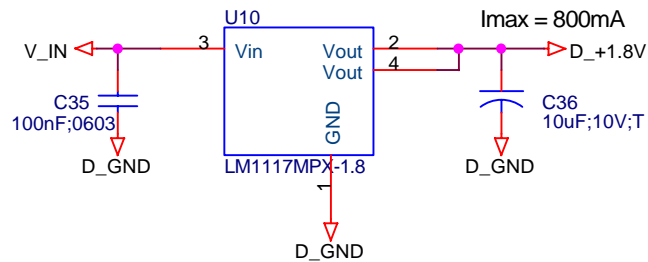
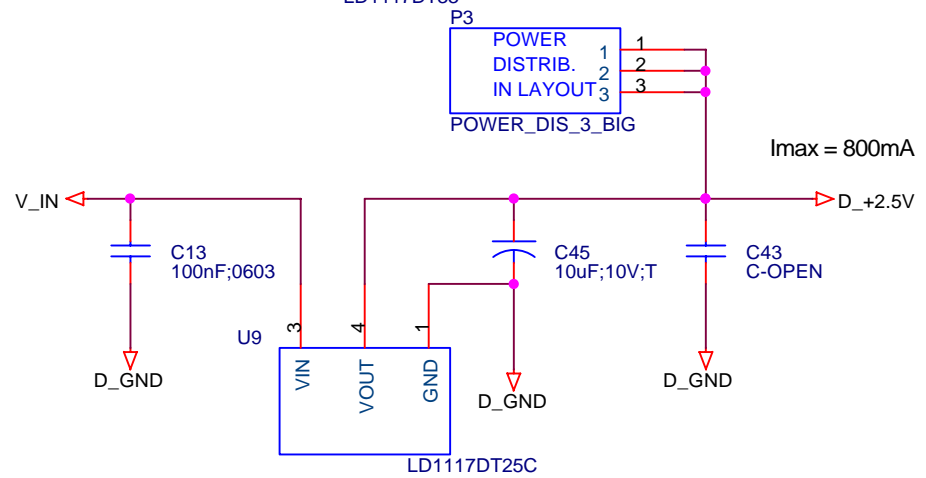
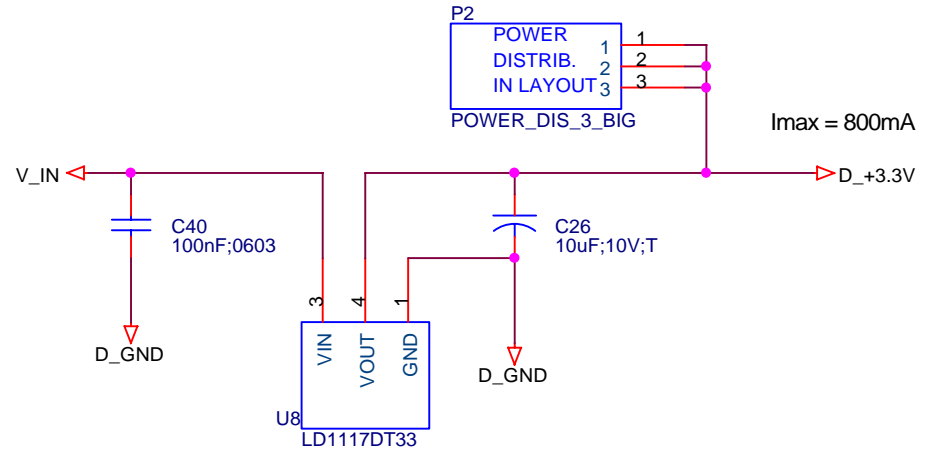
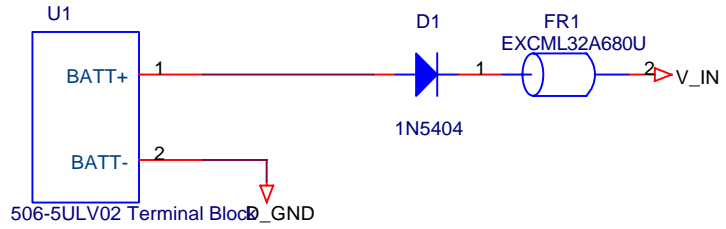
40 PIN OUTPUT - LEFT



FPGA 1



+5 V Supply



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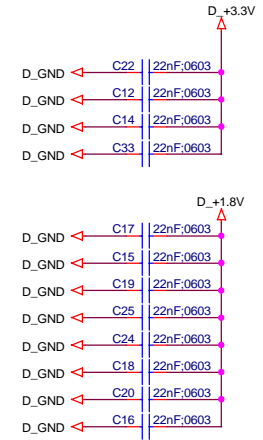
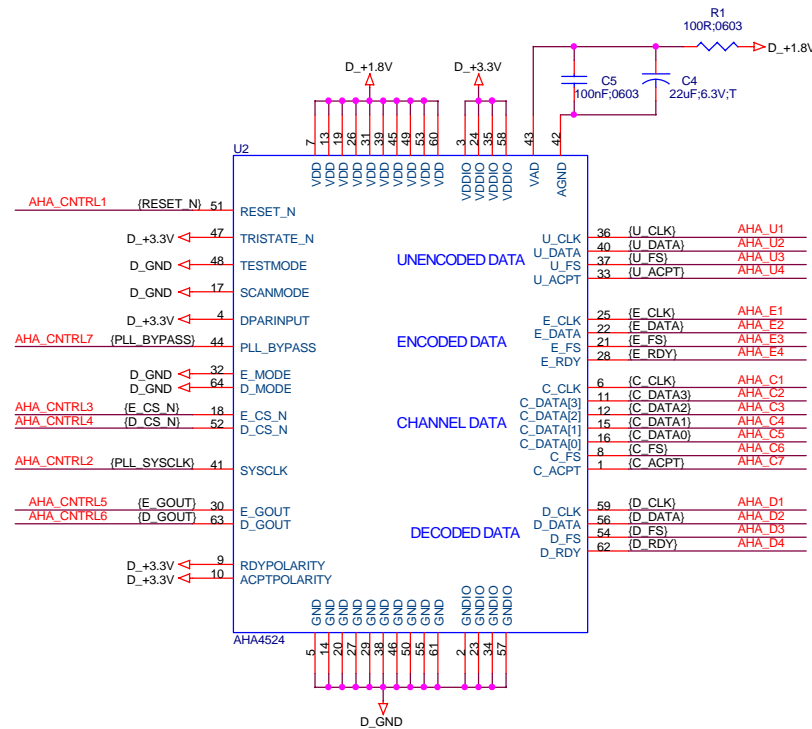
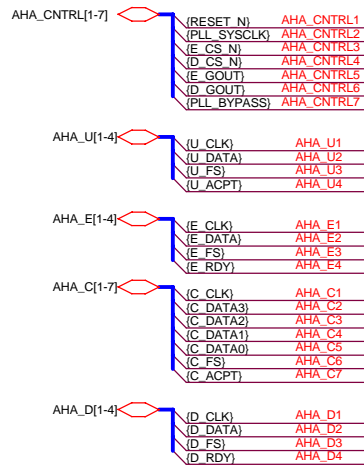
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