TROUBLESHOOTING MONITORING AND CONTROL (M&C) CONNECTIONS

Objective

The purpose of this document is to help debug ComBlock assemblies when the primary symptom is 'lack of communication with the ComBlock Control Center'.

Low supply voltage

The most common cause of bad or unreliable communication between a ComBlock assembly and the ComBlock Control Center is too low a power supply voltage.

Many ComBlocks exhibit communication problems when the supply voltage falls below 4.9V. Please measure the supply voltage at the green terminal block, as a voltage drop can occur between the power supply and the ComBlock assembly when the hookup wire is too thin or when the ComBlock power consumption is large (for example COM-3004 or COM-4004).

Recommendation:

a) supply voltage 5.0V – 5.1V is best when measured at the green terminal block.

b) hookup wires gauge AWG 18 for low voltage drop between the power supply and the ComBlock assembly.

FPGA is not configured

If the ComBlock assembly includes FPGAs, communications could be impeded if the FPGA is not configured or is configured with a flawed configuration.

To verify that the FPGA is configured, please check the 'DONE' test point with an oscilloscope or voltmeter. The DONE test point should go high (2.5V or 3.3V) within a few seconds after power up.

If the DONE test point is low, the FPGA must be reprogrammed.

To reprogram the FPGA, it is best to disconnect the board from the other ComBlocks.

Bad FPGA configuration

On ComBlock FPGA development boards, developers can accidentally load FPGA code which is syntaxically correct (DONE test point goes high, FPGA is happy) but which interferes with the serial communication or the Atmel microcontroller.

If so, the method to recover communications is either

a) to block the FPGA from configuring at power up (using a short wire, hold the INIT# test point to ground while powering up the ComBlock). Works for COM-1000, COM-1100 and COM-8000 platforms.

b) to force the FPGA to load the default configuration. See the COM-1200, -1300, -1400 specifications.

Missing .ucf constraint file in the Xilinx ISE project is the most common cause for a bad FPGA. In this case, pins are not connected to the internal nets as expected.

Tracing the problem

In large ComBlock assemblies, it can be difficult to trace the origin of the communication problem. The easiest method to identify where the problem is is to use an oscilloscope to track messages exchanged between the ComBlock control center and the ComBlock assembly.

It is important to know that all messages go through pins A18 and B18 of each 40-pin connector.

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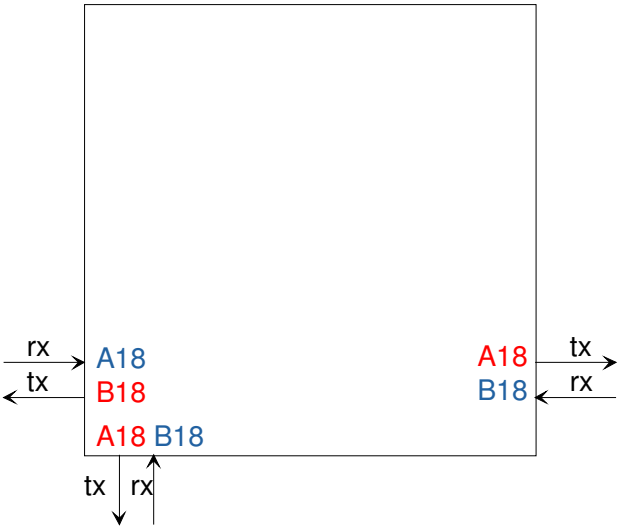
 Issued 11/27/2008

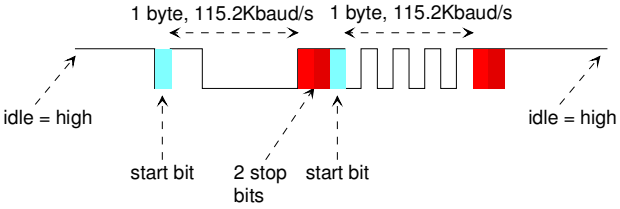


The procedure to pinpoint problems is as follows:

a) from the ComBlock Control Center, click on the enumeration button (2nd from the left) to trigger messages.

b) Using an oscilloscope, probe on the A18 or B18 pins to detect activity.

The messages are transmitted as 115.2 Kbaud asynchronous serial signals.

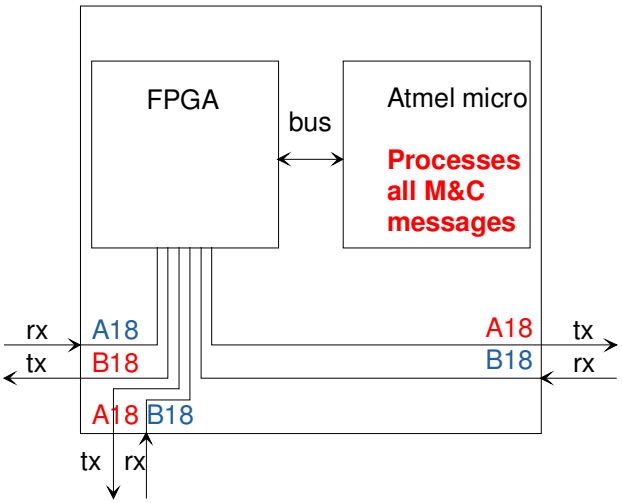


Please check that, when idle, the A18/B18 serial lines should be pulled high to 3.3V

When clicking on the enumerate button, the ComBlock Control Center shall ask each module to identify itself. Questions and Answers should be clearly visible using an oscilloscope probe on pins A18 and B18.

Don't forget the microprocessor

Nearly every ComBlock has a built-in microprocessor (Atmel AVR ATMega) which processes all M&C messages, whether the message is destined to this ComBlock, or the message is only in transit.



In ComBlock FPGA development platforms, messages also go through the FPGA. It is thus mandatory to follow two rules when writing custom code for the FPGA:

1) connect the M&C pins A18 and B18 to the FPGA
2) connect the FPGA to the Atmel microprocessor 8-bit address/data bus.

Failure to do will cause a break in M&C communication.

To help with this process, please start any custom FPGA code with the full supplied code template.